Committed to Innovation, Leti Creates Differentiating Solutions for its Industrial Partners.

Leti is a research institute of CEA Tech and a recognized global leader in miniaturization technologies. Leti’s teams are focused on developing solutions that will enable future information and communication technologies, health and wellness approaches, clean and safe energy production and recovery, sustainable transport, space exploration and cybersecurity.

For 50 years, the institute has built long-term relationships with its industrial partners, tailoring innovative and differentiating solutions to their needs. Its entrepreneurship programs have sparked the creation of 64 start-ups. Leti and its industrial partners work together through bilateral projects, joint laboratories and collaborative research programs.

Leti maintains an excellent scientific level by working with the best research teams worldwide, establishing partnerships with major research technology organizations and academic institutions. Leti is also a member of the Carnot Institutes network*.

*Caron Institutes network: French network of 34 institutes serving innovation in industry.

CEA Tech is the technology research branch of the French Alternative Energies and Atomic Energy Commission (CEA), a key player in research, development and innovation in defense & security, nuclear energy, technological research for industry and fundamental physical and life sciences.

www.cea.fr/english

Leti at a glance

€315 million budget
800 publications per year
ISO 9001 certified since 2000

Founded in 1967
Based in France (Grenoble) with offices in the USA (Silicon Valley) and Japan (Tokyo)

1,900 researchers
2,760 patents in portfolio
91,500 sq. ft. cleanroom space, 8” & 12” wafers

350 industrial partners
64 startups created
Within CEA Tech and Leti, Optics and Photonics activities are focused principally on big industrial markets of photonics: all-wavelength imaging (visible, infrared, THz), information displays, solid-state lighting, optical data communications, optical environmental sensors.

The R&D projects are performed with industrial and academic partners. The industrial partners of the Optics and Photonics division range from SME to large international companies. The projects are merging fundamental aspects with advanced technological and industrial developments; nano-sciences are interwoven with material sciences, optics, electronics and micro & nano-fabrication.
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Optics and Photonics Division (DOPT) of Leti fosters employment in France and Europe by developing innovative photonic components. We see miniaturization and integration as the main driving factors to reach this target. We help our industrial partners to decrease the cost, to improve the performances and to diversify the functionalities of their products.

DOPT is focused on various topics such as visible, infrared and THz imaging sensors as well as integrated photonic components, optical gas sensors and light emitting arrays, displays and smart lighting. In each area, DOPT, with its 300 staff members, concentrates long-term expertise, up-to-date clean rooms and equipment and dedicated characterization benches. 90% of our funding is obtained through one-to-one or collaborative projects, both with academic and industrial partners. The high quality of our partners is also our strength.

Staying at the leading edge of applied photonic research requires a deep understanding of product and application needs in terms of performance, cost and functions, as well as an ability to introduce new concepts in our process flows. It also relies on our ability to set-up new optical benches for in depth characterization or for proof of concepts validation.

I hope that reading this report will make you want to know more about us, meet us at conferences, forums or Leti events, join us as a researcher or PhD student or, of course, build fruitful collaborations on research topics tackling the microscopic behavior of photons using state-of-the-art industry compatible facilities.

Have a nice reading!
Key figures

- **215** permanent researchers
- **40** PhD students and Post-docs
- **50** CEA experts: with **4** directors of research and **2** international experts

- **150** publications in 2017 including **65** papers in peer reviewed journals

- **90** patents filed in 2017
- **500** patents portfolio with about **20%** under licensing contract

Dedicated clean rooms for III-V and II-VI materials on versatile substrate geometries up to 150 mm

Access to Leti clean rooms through numerous photonic fab processing modules in 200 and 300 mm format

Optics and opto-electronics characterization facilities

Advanced means of modeling and simulation
Awards

François TEMPLIER received a “best paper award” of the Journal of the Society of Information Display (JSID) for “GaN-based emissive microdisplays: A very promising technology for compact, ultra-high brightness display systems”

Badhise BEN BAKIR and Thomas FERROTTI received a “best paper award” at the International Conference on Solid State Devices and Materials (SSDM), for the design and the tests of a 1,3µm hybrid III-V on Silicon Transmitter operating at 25Gb/s

Divya TANEJA received the “Student traveler award” at the Electronic Components and Technology Conference (ECTC 2017) for the paper « Cu-SnAg Interconnects Evaluation for the Assembly at 10µm and 5µm Pitch”

Conference and workshop organization

Tony MAINDRON: the RAFALD workshop on “Atomic Layer Deposition (ALD) techniques” (Montpellier, France)
Guy FEUILLET: at the “Int. Conference on Nitrides semiconductors” (ICNS, Strasbourg, France)

Book

• Internal strain in HgCdTe photodetectors
• Intensity-dependent photoluminescence decay in HgCdTe
• Dark current in HgCdTe photodetectors
Micro-laue investigation of internal strain in HgCdTe photodiodes

Authors: A. Tuaz, P. Ballet, X. Biquard and F. Rieutord (CEA INAC)

Abstract:

While beam micro-Laue has been used at ESRF to investigate bi-axial strain profiles in HgCdTe/CdZnTe structures, in particular the effect of alloy composition variation induced lattice mismatch in multilayer stacks or diffused interfaces has been studied. Through two different examples we show that micro-Laue can be used to very accurately track small diffraction peak displacements allowing for extracting strain profiles with a very good precision and a 200nm in-depth resolution.

Context and Challenges

Internal strain in HgCdTe photodiodes is generally considered as a prominent source of extended defects via lattice relaxation, and its origin can be multiple resulting from epitaxial misfit, annealing induced composition interdiffusion, or technological processing. While macroscopic manifestation of strain build-up can be related to device performance, its microscopic determination over the range of an interface and within large thickness layers or multilayer stacks requires the sub-micronic resolution of extremely focused white X-ray beams only available at synchrotron radiation facilities.

Main Results

Here we propose to demonstrate the ability of Laue microdiffraction to resolve low strain gradients (in the 10⁻⁴ range) over large thickness layers with a spatial resolution of about 200nm. We have conducted Laue experiments with a 300nm diameter white beam probe using the micro-diffraction setup of the French CRG beamline BM32 at the European Synchrotron Radiation Facility (ESRF). We already demonstrated the ability of this setup to spatially resolve lattice deformation induced by processing steps in HgCdTe [1]. This time we focus our analysis on the extraction of biaxial strain along the growth direction in molecular beam epitaxy grown HgCdTe/CdZnTe structures, and we correlate our results with the evolution of the alloy fraction, either imposed by growth or induced by annealing.

The first example is the study of a diffused HgCdTe/CdZnTe interface after annealing at about 400°C. The measured strain deduced from the diffraction peak displacement when crossing the interface is displayed on Figure 1 together with the calculation of this strain component based solely upon the lattice parameter variation due to alloy composition variation extracted from SIMS data.

Microdiffraction and diffusion-derived strain data fully match over the substrate-layer interface demonstrating the ability of this technique to provide quantitative and spatially resolved strain values in quasi lattice-matched systems.

The second example is a more complex dual-band structure made of several HgCdTe layers of different alloy composition. The structural and compositional investigation is here made through energy dispersive X-ray (EDX) in scanning tunnelling electron microscopy mode (STEM) : Figure 2, showing in red the contrast the localization of the cadmium-rich layers (substrate-barrier-cap) and the superposition of the extracted cadmium profile with the out-of-plane stress extracted from micro-Laue. Again, the correlation is striking, thus demonstrating that the strain is mostly related to lattice parameter variation induced by composition changes throughout the entire stack.

Please note that we logically measure zero strain in the lowest cadmium concentration layer because the zinc content in the substrate has been set for lattice-matching to that particular layer.

Figure 2: Top: STEM-EDX image of a dual-band stack, bottom: micro-Laue strain (red) and EDX derived cadmium fraction as a function of depth z.

Perspectives

This study demonstrates the validity of the micro-Laue extracted biaxial strain in quasi lattice-matched HgCdTe/CdZnTe structures with a 200nm spatial resolution thus offering the potential for investigating localized strain fields in HgCdTe photodiodes with possible correlation with device performance. Going further, a complete technological device combining epitaxial and processing sources for strain could be successfully investigated.

Related Publications:

LIGHT INJECTION LEVEL DEPENDENT PHOTOLUMINESCENCE DECAY LIFETIME MEASUREMENTS IN SEMICONDUCTORS FOR IR DETECTION AND EMISSION

AUTHORS:
J. Rothman, B. Delacourt, P. Bleuet

ABSTRACT:
A photoluminescence decay (PLD) measurement set-up have been developed to measure the lifetime of minority carriers in small band-gap semiconductor devices. The set-up uses original HgCdTe avalanche photodiodes (APDs), manufactured CEA/LETI, to detect the temporal variation of the photoluminescence signal down to the low injection regime even in samples with low doping levels and up to wavelengths of 5.6 µm. This has enabled to study the PLD signal as a function of the injection level in small gap semiconductor. The analysis of this variation improve the separation of the different contributions to the recombination mechanism in the samples and our understanding of the fundamental limits in terms of dark current and operating temperature.

Context and Challenges
The understanding and quantitative calibration of the generation and recombination mechanisms, that govern the minority carrier lifetime, are essential for the optimization of the performance of semiconductor devices. In particular, a long lifetime at relatively high doping levels is essential to minimize the dark current and/or to increase the operating temperature in infrared photo-detectors, which is a main driver to reduce the cost, increases the reliability and reduce power consumption of the detectors.

The measurement of the lifetime in semiconductors is difficult as it require a high sensitivity to explore the temporal dependence of a small perturbation of the carrier density that is negligible to the doping level in the sample. This particularly relevant for PLD lifetime measurements in which the low level of emitted photons needs to be extracted from the sample and concentrated onto a fast photodetector. PLD measurement in the IR range is further impeded by the absence of commercially available high sensitivity and fast photodetectors in the IR range which have limited the full exploration of this measurement technique in the past.

Main Results

Figure 1: PLD signal at different initial light injection levels, measured on a mercury vacancy doped (V\text{Hg}) Hg_{0.7}Cd_{0.3}Te P-type sample with p=5x10^{15} cm^{-3} at 80 K.

The development of high sensitivity time resolved HgCdTe APD photo detection modules [1] have allowed us to reach a new level of sensitivity for PLD measurement at IR wavelengths up to 5.6 µm. This has enabled to explore the PL signals into the low injection regime and enable carrier lifetime measurement even in samples with low carrier densities. In addition, we have shown that the analysis of the evolution of the PLD signal from the high to low injection levels enables to quantitatively separate the Auger, radiative and Shockley-Read-Hall contributions to the carrier recombination by taking into account the expected variation of each contribution as a function of the excess carrier concentration [2]. Figure 1 shows a comparison between measured and calculated injection dependent PLD signal for different initial injection levels on a mercury vacancy (V\text{Hg}) doped P-type Hg_{0.7}Cd_{0.3}Te. The corresponding variation of the estimated contributions are plotted as a function of temperature in Figure 2. The incertitude of the estimation is presently limited by our knowledge of the photon extraction efficiency in the samples and will be reduced with time. In this sample of more academic interest, the analysis has improved our understanding of the SRH lifetime limitations of the centers associated with V\text{Hg} doping and improved our calibration of the Auger generation and recombination model in HgCdTe.

Figure 2: Variation of the estimated contributions to the lifetime in V\text{Hg} doped Hg_{0.7}Cd_{0.3}Te

Perspectives
The PLD measurement set-up have recently been improved to map the lifetime on wafers during the processing of the photodiodes. It is presently used to optimize the diodes in all projects that aim to increase the operating temperature of the detectors. The set-up will be optimized to achieve spectral and sub-pixel spatial resolution. We also intend to explore its use for other applications of time resolved IR microscopy, such as biology or surface chemistry.

RELATED PUBLICATIONS:
Rule 07 heuristic law is very convenient to describe the dark current for p-on-n photodiodes processed on high quality HgCdTe materials. Easy to compute, it is used as a powerful tool for comparison and benchmarking for II-VI manufacturers and III-V compounds competitors but also for agencies to specify the requirements for next generation ground or space instruments. However, Rule 07 law is not based on physic considerations and outside the application range it shows its limits, especially in the LW and VLW bands. An improvement of this rule has been proposed, based on results obtained on detectors from CEA-LETI.

Context and Challenges

The hunt for exoplanets has become one of the major challenge for deep space observation within the last decade. For some candidates, further analysis could be performed and particularly on the content of their atmosphere. ECHO and ARIEL ESA missions have been designed to answer this question. But observing cold and faint objects at a long distance from Earth leads to strong requirements: long cutoff wavelength and low dark current, the last one calculated according to Rule 07. Improvements of the technological process have been introduced to meet these requirements at low temperature.

Main Results

Different detectors batches have been manufactured to improve a new technological heterojunction process based on HgCdTe liquid phase epitaxy and to verify the gain on performances. The results show that the dark current is in good agreement with Rule 07 law at 78K, but when the temperature decreases, the dark current decreases at a lower rate than Rule 07, following a pure diffusion law [1].

The origin of the difference relies in the expression of Rule 07:

\[ J = J_0 \exp(C \times E(T)/K) \]

where \( C = -1.1624 \) according to the reference paper, instead of \(-1\) which corresponds to the physical law of the diffusion dark current. This rule appears to be very accurate to calculate the dark current at 78K on a large range of cutoff wavelengths, which was its main utility, and not the evolution of the dark current with temperature for a given HgCdTe compound.

Using the measurements performed at CEA-LETI and CEA-IRFU on various detectors of different cutoff wavelength, a new rule has been introduced to calculate the dark current of p-on-n photodiodes made of HgCdTe [2]. Even if it is partially inspired by the Rule 07, it allows to determine the dark current with a high reliability for a larger range of cutoff wavelength and operating temperature than Rule 07. This rule is less simple the Rule 07 but still easy to compute with only few parameters:

\[ J_{diff}(T) = J_0 \exp(-29.936/L_{optical}) \exp(-E_g(T)/K) \]

Its accuracy has been verified on detector from CEA-LETI (with cutoff wavelength from 9.5 to 17.2 µm at 78K) and on measurements published on detectors from other manufacturers.

Perspectives

This new rule, based on measurements performed on detectors from CEA-LETI, brings to IR community a tool to calculate the dark current on a wide range of cutoff wavelengths and temperatures for state-of-the-art p-on-n HgCdTe technology.
• Electromechanical resonators as thermal imaging sensors
• Silicon bolometers as millimeter wave detectors
• THz spectroscopy for hydration monitoring of green plants
OPTICS AND PHOTONICS

12 µm-PITCH ELECTROMECHANICAL RESONATOR FOR THERMAL SENSING


ABSTRACT:
We have demonstrated a 12 µm pitch nanoelectromechanical resonant infrared sensor with fully integrated capacitative transduction. Low temperature fabrication process was used to manufacture torsional resonators arrays. H-shape legs supporting pixel with 9 µm-long nano-rods and 250 nm × 30 nm-cross section were designed to provide strong thermal response, with experimental values up to 1024 Hz/nW. A mechanical dynamic range of over 113 dB was obtained, which led to an unprecedented Allan deviation of $\alpha_\alpha = 3 \times 10^{-8}$ at room temperature and 50 Hz noise bandwidth. These features allowed to reach a sensitivity of the 8-12 µm radiations of 27 µW/°K leading to a noise equivalent temperature difference (NETD) of 2 K for a 50 Hz noise-bandwidth. By both improving the temperature coefficient of frequency of a factor 10 and using a readout electronics at the pixel level, these resonators will lead to a breakthrough for uncooled infrared detectors.

SCIENTIFIC COLLABORATIONS: KAVLI NANOSCIENCE INSTITUTE, CALIFORNIA INSTITUTE OF TECHNOLOGY

Context and Challenges
Over the last 20 years microbolometer has become the most prominent uncooled infrared technology. They operate by converting the radiation-induced heating of a thin membrane in a variation of electrical resistance. Such thermistors are commonly made of a thin film of semiconductor, using mostly Vanadium Oxide (VOX) or amorphous silicon (α-Si). The induced heating effect is advantageously enhanced by achieving a high thermal insulation between the sensor and the substrate. Thermal insulation as high as 200 MK/W has been reported for microbolometers with 12µm-pixel pitch [5]. Such devices currently exhibit 50K-noise NETD (F/1 lens, 30Hz frame rate, 300K background) [1]. Nevertheless, in case of excessive radiant power the temperature of the sensing material can increase dramatically leading to a detrimental drift of the thermistor properties. To address this issue, we suggest unique pixel architecture whose arrangement calls for the replacement of the common thermistor by a mechanical nano-resonator designed to be highly sensitive to temperature.

Main Results
Contrary to NEMS approaches usually used to get stable nano resonators, we have chosen a low temperature fabrication process, which is inherited from classical bolometers [2]. The figure 1a) shows structures magnified by scanning electronic microscope (SEM). The microsystem is excited at its first torsion mode using an actuation electrode placed under the plate. An incident infrared electromagnetic wave is absorbed by a thin metallic layer deposited on top of the plate and causes the heating by free carriers Joule effect. Thereby, the temperature rise induces a variation of the torsional resonance frequency that is measured through capacitive signal between the detection electrode and the oscillating plate. A dedicated readout electronics board based on a trans impedance circuit was carefully developed for measuring the tiny capacitance variation (~30aF) compared to both the capacitance at rest (~0.18F) and the parasitic capacitance (~1pF). Typical electromechanical response with frequency and an AC-actuation voltage $V_{AC}$ (at $V_{bias}=10V$) is plotted in FIG. 1b. The output voltage at resonance is clearly proportional to $V_{AC}^2$ [3], [4]. To perform the thermal characterizations, we embed the system in a down-mixed Phase Locked Loop (PLL) to track the resonance frequency change in real-time. The electronics board with pixels were placed into a home-made vacuum chamber that were illuminated by a black body source.

Figure 1. a) Scanning electron microscope (SEM) picture of typical matrix of micro electromechanical pixels - b) electromechanical response according to frequency and actuation voltage

The frequency response to IR incident pulses (26nW-peak) is presented in Fig. 2. A typical experimental thermal response $R_i=720 \mu W$ has been extracted from this measurement. From noise measurements, we have estimated a sensitivity to 8-12 µm radiation below 27nW/°H leading to a NETD of 2 K at 50Hz and NETD=1.5K at 100ms (with a sub-millisecond response time) [1].

Figure 2. Frequency response. IR illumination corresponds to 26-nW incident power.

Perspectives
We have demonstrated the great potential of high frequency resonant sensor fabricated with a low temperature process dedicated to uncooled infrared imaging. A NEP of 190pW has been measured with our system at 50Hz-integration time. With a co-integrated electronics which reads 14 pixels in a 700 Hz-bandwidth through an above IC self-oscillating loop, the NEP should drop down to 165pW close to the anomalous phase noise of the resonant sensor. However, to surpass the bolometers below 12µm-pitch the temperature sensitivity has to be increased at least by a factor 10. To this end, works based on first order phase transition material should allow to increase the frequency response through a large improvement of the TCF.

DESIGN AND FABRICATION OF COOLED SILICON BOLOMETERS FOR mm WAVE DETECTION.

AUTHORS:

ABSTRACT:
CEA has a long history of optoelectronic components development for space and astronomy applications. With this expertise, we are undertaking the development of cooled silicon bolometers for millimeter (mm) and sub-mm wave polarization detection addressing the needs of next generation radio-telescopes. The sensor presented in this work is optimized for the 1.5-mm band and operates around 100mK to reach a noise-equivalent power of a few aW/Hz^{0.5}. The bolometer is composed of doped-silicon thermometers suspended above an optical cavity and supporting superconducting thin film absorbers. 16x16-pixel arrays with a pitch of 1.2 mm are fabricated in LETI’s facilities on 200-mm CMOS read-out circuit wafers in an above-IC configuration.

Context and Challenges
The development of large focal planes with high sensitivity cryogenic detectors is a strong need for the observation of the universe in sub-mm and mm-wave bands. The current state of the art includes several kinds of cooled detectors such as KIDs (kinetic inductance detectors), TES (transition edge sensors), and silicon bolometers. In contrast to KIDs and TES, silicon bolometer technology has been demonstrated successfully in space conditions through the Herschel mission. It benefits from a simple and low-power read-out circuit that can be integrated below the detector array in an above-IC (Integrated Circuit) integration scheme. The fabrication of large arrays of detectors, tuned in the mm-wave band, using standard microelectronic processes above a CMOS read-out IC is a key challenge addressed in these developments.

Main Results
A novel silicon bolometer pixel has been designed for radiation detection and polarization measurement at 1.5-mm wavelength. The fabrication is made in LETI’s clean room facilities on 200mm CMOS readout circuit wafers (figure 1). Each array is composed of 16×16 pixels with a pitch of 1.2 mm; the pixel structure is composed of active and reference thermometers arranged in four half-bridge circuits to enhance the sensitivity (figure 2). Thermometers are made of ion-doped and diffused silicon meandered arms suspended above a thick oxide layer and a metal reflector forming an optical cavity. The absorption of the incident radiation is made by a superconducting bi-layer Ti/TiN thin film deposited on the silicon thermometer. The silicon thermometers are 1.5 μm thick and doped with phosphorus and boron species. Doping and diffusion have been optimized to achieve an uniform doping profile through the thermometer thickness and to have a 3D variable range hoping (VRH) conduction with a weak 1/f noise at low temperature. Simplified thermometer test structures have been characterized at low temperature, typically in the range of 40-200 mK, and showed a good accordance to an Efros law. A sensitivity (S = -T/R*dR/dT) of -6.5 was measured at 100 mK and can be further increased by lowering the working temperature.

Superconducting absorbers made of Ti/TiN bi-layers were developed as well and tuned in critical temperature T_c and electrical impedance [1]. A thickness of 100/5 nm was selected with a critical temperature of about 750 mK.

Based on these experimental results, the electrical, thermal and optical performances of the pixel have been simulated. An optical absorption of about 95% at 1.5 mm wavelength is obtained (figure 2) and a Noise Equivalent Power (NEP) of a few aW/Hz^{0.5} at 100 mK is expected.

Perspectives
First wafers of silicon bolometer arrays without read-out circuit have been fabricated in LETI’s clean room facilities and are currently under characterizations. The experimental results will be used to improve electrical and thermal models for the design of next-generation focal plane arrays for mm wave detection.

Figure 1: Illustration of the collective manufacturing on a 200mm wafer.

Figure 2: Photograph of the fabricated pixel with a pitch of 1.2mm and simulated absorption as a function of wavelengths.

RELATED PUBLICATIONS:
HIGH PRECISION MONITORING OF PLANT WATER STATUS USING THZ TIME-DOMAIN SPECTROSCOPY

AUTHORS:
M. Hamdi, J. Oden, J. Meilhan, F. Simoens, and B. Genty (CNRS, Univ. Aix-Marseille, UMR7265)

ABSTRACT:
THz time-domain spectroscopy (TDS) is a promising method for drought stress monitoring in plants. Hence, the absorption coefficient of water in this part of the electromagnetic spectrum is remarkably high and can be used as a vital indicator for the physiological monitoring of plants. In this study, we analyzed the THz transmission through ivy leaves and a realistic multilayer model was developed to improve the estimation of the water content as compared to commonly used single layer models. Experimental results were obtained with less than 2% of residual error as compared to a reference gravimetric measurement.

Context and Challenges
Efficient irrigation is crucial to optimize the productivity and the use of water resources in agriculture. Plant water status can be used as a reliable indicator for irrigation schedule. For this purpose, the non-destructive monitoring of leaves/plants water content has gained major interest since existing techniques like gravimetric method, distillation method and pressure chambers are mainly time-consuming and destructive.

The THz spectrum range appears to be well suited for continuous non-invasive contactless water content monitoring. One of the unique properties of the THz radiation is the strong absorption by polar liquids like water, which can be considered as a reliable indicator for leaf water content [1]. In this work, we focus on mild water stress for physiological leaf water contents which range between full turgor and turgor loss point. In addition, we take a closer look at the physical modeling of the leaf by using a more realistic multilayers approach.

Main Results
Experiments were performed on Ivy leaves (Hedera helix). Gravimetric and THz measurements were carried out simultaneously on a single leaf disc dehydrating in the ambient atmosphere. The THz measurements were carried out using a fiber-coupled THz TDS system in transmission mode employing a collimated beam. The THz and gravimetric measurements were done at the sampling rate of 15 Hz and 5 Hz, respectively.

Figure 1 presents the transmission coefficient at a frequency of 200 GHz as a function of dehydration time. The results show a clear increase in transmission as the leaves loose water, which demonstrates the high sensitivity of THz spectroscopy even at high water content.

The first leaf model used in this study was a simple heterogeneous layer made up of water, air, and dried leaf tissue. We noticed a significant deviation between the relative water content (RWC) derived from the gravimetric and THz measurements; the relative error is up to 5%, which prevents a reliable evaluation of leaf water content from THz measurement.

Typical leaf anatomy shows that distinct tissue layers compose the leaf and makes it a complex medium. We modeled the leaf by a new multilayer stack composed of distinct layers mimicking the different tissues and we developed a dedicated root finding algorithm based on latent variables for the inverse problem extraction process. Figure 2 shows a good agreement between the RWC derived from the gravimetric and THz measurements. In this case, we obtained a residual error less than 2%.

Figure 2. Comparison of gravimetric (triangles) and THz (squares) measurements of the RWC of ivy leaves.

Perspectives
Future works will include the experimental validation on new plant species and more statistical analysis of the root-finding algorithm for the inverse problem extraction process with refined models.

Figure 1. THz transmission at 200 GHz as a function of dehydration time.

REFERENCES:
• CMOS-integrated interference optical filters
• Depth imaging with indirect time-of-flight
• Curved CMOS sensors
TRANSMISSION MEASUREMENTS OF MULTILAYER INTERFERENCE FILTERS DEVELOPED FOR A FULL INTEGRATION ON CMOS CHIP

AUTHORS:
L. Masarotto, L. Frey, M.-L. Charles, J.-B. Mancini, A. Roule, G. Rodriguez (DTSi), R. Souil (DTSi), V. Larrey (DTSi), C. Morales (DTSi)

ABSTRACT:
We describe a method to measure the transmission spectra of thin multilayers optical filters in order to be fully integrated on various types of CMOS image sensors (ambient light sensors, proximity detection, red green blue colour imaging, etc.). As the filters have to be deposited on top of a CMOS device, a promising approach in order to evaluate with accuracy their response on chip is (i) first to achieve the stacks on Si wafers (ii) then to perform a direct bonding of the structures on glass wafers (iii) in the end to remove the entire bulk silicon. In this way, we show the measured spectral responses of interference filters and can check particularly the agreement of transmission peaks with the simulations and their reproducibility wafer to wafer. It enables to optimize the filters designs and to check that the optical responses fulfill typical CMOS requirements of integration and reliability.

Context and Challenges
The spectral signatures of integrated multilayers filters on CMOS chip are observed in quantum efficiency measurements but do not show a perfect agreement in magnitude and in wavelength compared to simulated curves. As it is complex to differentiate the errors resulting from filters stacks and CMOS stacks, carrying out transmissions measurements becomes essential with a view to optimize the filters designs. Thus we show the possibility of bonding filters stacks on glass substrates and removing the Si initial bulk with chemical/mechanical thinning down in order to obtain the measured spectral transmittance of multilayers stacks made in similar conditions to the integration on CMOS chips.

Main Results
In this study, we design and make bandpass filters using single or multiple Fabry-Perot cavities. In the prospect to integrate ambient light and presence detection on CMOS chip, we investigate filters with Cu/dielectrics and a-Si/SiO	extsubscript{2} multilayer stacks for respectively the ALS and NIR functions. At first, the entire filters were deposited on 200mm Si wafers with polished and cleaned top PECVD oxides The Cu and SiN films of ALS stacks were developed at ambient temperature using DC magnetron sputtering. The SiO	extsubscript{2} and a-Si layers of NIR stacks were processed at 400°C by the PECVD technique. As shown in Fig. 1, both process techniques were adjusted to lower deposition rates to achieve a high control on the layer thicknesses and uniformities. The various stacks were carried out in different chambers of same tool without breaking the vacuum between the depositions in order to have clean interfaces without impurities or residual oxidations.

Then face-to-face direct bondings were performed on glass 200mm wafers and followed with a 400°C annealing for 2H. Finally, using successive mechanical and chemical thinning down processes, the sacrificial Si bulk were removed. Transfer process of multi-layer stacks shows a change of optical systems support without deteriorating or modifying the morphological properties. It enables the optical measurements in transmission of optical systems processed on Si bulk. The optical measurements of the multilayer have been performed by spectrophotometry. The measured and calculated spectral transmittances of the a-Si/SiO	extsubscript{2} and Cu/dielectrics multilayer filters are presented in Fig. 2. Each filter was measured several times with distinct wafers to check the structures reproducibility. We observe for both studied designs an excellent agreement between measured and simulated data with regard to the transmission peak wavelength and magnitude. The reproducibility of filter responses is moreover very satisfactory meaning the achieved processes are stable with standard deviation much better than the specified dispersion (5%) for the used tools. These results confirm that this method is a reliable way to optimize the designs and responses of the filters.

Figure 2: Comparison between the simulated and measured spectral responses of (a) NIR a-Si/SiO	extsubscript{2} filters (b) ALS Cu/dielectrics filters

Perspectives
This paper presents a novel method to measure the spectral transmittance of filters on opaque Si wafers by carrying out the transfer of multilayer stacks on glass wafer via direct molecular bonding. The transfer process did not impair the morphological and optical properties of the thin multilayers stacks and a good agreement between simulated and measured spectral responses is observed for both ALS and NIR interference filters with an excellent reproducibility. The bonding of multilayers stacks on glass substrates appears as a useful and efficient technique in order to measure the spectral transmittance and can be used for the optimization of filter designs and check precisely the predictions of optical responses in view of an integration on CMOS chips.

RELATED PUBLICATIONS:
DEPTHPMAP IMAGE OBTAINED FROM INDIRECT TOF (TIME OF FLIGHT) PIXELS WITH FAST TRANSFER GATES

AUTHORS:
B. Rodrigues(ST), M.Guillon, N.Billon-Pierron, J-B.Mancini, O.Saxod, B.Giffard, Y.Cazaux, P.Malinge (ST), P.Waltz (ST), A.Ngoua (ST), Y.Kerleguer (ST), A.Taluy (ST), S.Kuster (ST), S.Joblot (ST), F.Roy (ST), G.N.Lu (INL)

ABSTRACT:
We developed a time of flight (TOF) pixel with implementation of 3-tap phase-shifting technique [1]. The pixel integrates a pinned photodiode (PPD) and 3 charge-transfer paths. Each path is delimited by deep trenches and integrates a fully depleted memory (storage site) enabling Correlated Double Sampling (CDS) and a low-noise buried-channel Transfer Gate (TG). In order to achieve fast and efficient charge transfer, the pixel was designed in a size of 6.2μm x 6.2μm, and an image sensor chip was fabricated. Testing results show a dark current of 30 e-/s @60°C, readout noise of 3.2e- and a demodulation contrast (DC) of 73% @110 MHz using a 930nm light source.

SCIENTIFIC COLLABORATIONS: Institut des Nanotechnologies de Lyon, Univ. C.Bernard Lyon1, 69622 Villeurbanne, France

Context and Challenges
Several methods based on Time-of-flight (TOF) can be realized for acquiring a depth image: one of them is based on a continuous wave (CW) modulation with implementation of a multi-tap approach. The proposed pixel integrates a pinned photodiode (PPD) and 3 fully depleted memories as storage sites. It also integrates low-noise buried-channel to optimize charge collection and transfer efficiency from PPD to the 3 storage sites. The achieved pixel size is 6.2μm x 6.2μm, integrated in a QVGA image sensor chip which was fabricated and tested.

Main Results
To measure the distance, the scene is illuminated by a modulated near infra-red light source and the reflected light with delay is detected by the PPD of the pixel. Photo-generated electrons are then successively sampled at high frequency, typically 10 to 130MHz, and stored in 3 different memory sites. An additional fourth path is also included for anti-blooming (AB) purpose. Fig. 1. When TG is ON, photo-generated electrons from PPD are temporarily stored beneath its gate. When TG is OFF, the electrons are transferred into the memory (storage site). After a succession of switching TG with charge transfer, when the integration period is over, the whole sampled signal in charges is stored in the memory. For signal reading, the stored charges can be transferred into the FD node by turning Tx gate ON. This architecture allows CDS (before and after charge transfer through Tx gate), which eliminates kTC noise and rejects most 1/f noise. The phase difference between the emitted light signal and the received one by reflection is easily calculated and the distance is then determined:

\[ \phi = \arctan\left(\sqrt{\frac{1}{3}} \frac{Q_{in} - Q_{out}}{Q_{in} + Q_{out}}\right) \]

\[ D = \frac{c\phi}{4\pi} \]

where A and B correspond to the maximum and minimum of the signal.

The designed 464x197 pixel (QVGA) test chip was fabricated by a “burst characterization” was performed to evaluate charge-draining capability of the TGs, consisting in synchronizing a received laser pulse with one TG’s opening time during integration. Then the sampled signal (in charge packet) stored in the corresponding memory (after integration time) was compared to the sum of the stored charges in all memories. The results show that more than 70% of photo-generated electrons go to the desired storage site and the charge-draining via TG control is efficient for opening time down to a few ns. The demodulation contrast (DC): DC = (A-B)/(A+B), where A and B correspond to the maximum and minimum of the charge ratio respectively, reaches 75% at 50 MHz and 73% at 110 MHz (3ns of corresponding sampling period) @ 930nm illumination signal. Table 1 presents a summary of our pixel’s characteristics, in comparison with recently reported studies. Our achievements include high demodulation contrast ratio, low dark current, and low readout noise. Fig. 2 shows an acquired 3D image from the (QVGA) test chip, illuminated by a 25MHz 870nm LED.

Table 1: compared measured characteristics

Perspectives
This paper presents a novel pixel structure for depth map acquisition. We developed 6.2μm 3D-TOF pixel using pinned photodiode, fully depleted memories and operating with a 4T reading architecture. Integration of buried-channel TGs built on a doping-profile-controlled epitaxial layer improves charge-transfer efficiency and speed, which lead to high demodulation contrast. Due to its compatibility with common imaging process and voltage supply, the proposed pixel can be applied to the ultimate goal which is the integration of depth and color pixel in the same die, the standalone RGBZ camera.

CURVED CMOS SENSORS: TOWARDS MORE COMPACT OPTICAL SYSTEMS

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ABSTRACT:
In this paper, we first describe advantages of curved sensor and associated packaging process applied on a 1/1.8” format 1.3Mpx global shutter CMOS sensor (Teledyne EV76C560) into its standard ceramic package with a spherical radius of curvature Rc=65mm and 55mm. The mechanical limits of the die are discussed (Finite Element Modelling and experimental), and electro-optical performances are investigated. Then, based on the monocentric optical architecture, we propose new design, compact and with a high resolution, developed specifically for a curved image sensor including optical optimization, tolerances, assembly and optical tests. Finally, a functional prototype is presented with same performances and a x2.5 reduction of length compared to a commercial one. The finality of this work was a functional prototype demonstration on the CEA-LETI during Photonics West 2018 conference.

SCIENTIFIC COLLABORATIONS: Astrophysical Laboratory of Marseille (LAM), France.

Context and Challenges
Curved sensors help the correction of off-axis aberrations, such as Petzval Field Curvature, astigmatism, and bring significant optical and size benefits for imaging systems. There are already several developments on the fabrication of curved sensors. For the monolithic approach, the fabrication has been demonstrated on uncooled and cooled infrared sensors, for very compact high-performance camera [1], Charge Couple Device (CCD) (ex.: http://www.andanta.de), or Complementary Metal Oxide Semiconductor (CMOS) (Itonaga, K. et al., Sony R&D Platform, Atsugi, Japan. Symposium on VLSI Technology, 2014 and Guenter, B. et al., Optics Express 25, no. 12, 2017). None is in industrial production. In 2017, two optical systems prototypes equipped with curved sensor have been realized and tested. One is dedicated to professional photography and the other one for machine vision (discussed in this paper). These demonstrations were possible with mechanical and optical modelling, curved CMOS sensor packaging, electro-optical tests, and optical characterization.

Main Results
In order to implement a spherically shaped CMOS sensor, changes are required to adapt this standard structure. First, the sensor is thinned with a grinding equipment to a targeted thickness in order to make the sensor mechanically “flexible”. It can be followed by a Chemical Mechanical Polishing (CMP). In this work, the targeted thickness is 100µm. Mechanical models (ANSYS software) help us to define curving limits of the dies. Then, that thinned chip is glued (structural attachment) onto a curved substrate. The CMOS final shape is drove by the substrate. Wire bonding process, developed for electrical connections, is also optimized in order to prevent damages on thinned dies. Figure 1 shows a global view of the final packaging, curved into its commercial packaging. The radius of curvature is R=65mm.

Effects of tensile or compressive stresses applied on the CMOS active layers have to be studied in order to know if curved sensors keep good performances. Results on curved sensor show a standard response compared to flat sensor (standard) and we can confirm that within (+inf.; 55mm) radius of curvature range, curving process has no significant impact on the Teledyne EV76C560. The step forward is the optical design. Thanks to Zemax software, monocentric architecture (system which combines compactness, wide field of view, high resolution, large light collection, and highly curved focal plane) has been implemented and optimized according to mechanical limits of the CMOS sensor. After tolerances, assembly, optical tests, and using our curved technology, we demonstrate an impressive simplification of the optical system (~40% of lenses) and a huge reduction of the total length by 2.5 time for the same optical performances compared to an equivalent commercial system (figure 2).

Perspectives
Curved sensor technology is a disruptive approach to bring innovations in optical systems. Using curved sensors, we demonstrate the opportunity to drastically reduce the complexity of existing solutions. Our bending process is scalable to any die size. Further developments are in progress for cost effective, large-scale manufacturing processes.

Figure 1: Curved Teledyne EV76C560 sensor with CEA-LETI process (R=65mm).

Figure 2: a) LETI prototype equipped with curved sensor. b) Image from this prototype (working distance 40 cm).

REFERENCES:
• Sol+SiN platform for $\theta$-insensitive CWDM transceivers
• Frequency-combs with $\text{Si}_3\text{N}_4$
• GeSn lasers
• 200 mm CMOS-compatible III-V/Si DFB lasers
• Micro-ring modulators integrated with III-V/Si lasers
• Reflective FTTH/PON unit
OPTICS AND PHOTONICS

SOI-SiN PHOTONIC PLATFORM FOR TEMPERATURE-INSENSITIVE CWDM OPTICAL TRANSCEIVERS.

AUTHORS:

ABSTRACT:
Within the framework of the H2020 European project COSMICC, we report on the integration of a SiN photonic layer in the LETI's 200 nm silicon photonics platform. This enhanced platform targets energy-efficient optical transceivers for datacom applications by taking advantage of the low temperature sensitivity of SiN. Water-level characterizations of low-loss SiN waveguides in the O-band confirm the superior passive properties of SiN. Furthermore, we demonstrate a temperature quasi-insensitive SiN multiplexer as well as broadband hybrid Si-SiN grating fiber couplers and Si-SiN interlayer transition.

Context and Challenges
The constantly growing network traffic in data centres requires low cost, high speed and energy efficient transmission solutions. This challenge can be met by Silicon photonics in the near future. Using CMOS compatible manufacturing process opens the way to large volume and low cost fabrication of on-chip photonic transmitters or receivers [1]. Looking toward integrated photonic systems, and targeting data center applications, an attractive solution to expand the data rate of transceivers is coarse wavelength division multiplexing (CWDM). This standard provides a large enough channel spacing of 20 nm to avoid an energy-consuming temperature control of the lasers but it requires broadband and low temperature sensitivity optical devices. In this respect, Silicon Nitride (SiN) is an appealing material for photonics: it is CMOS-compatible, its lower optical index offers a better robustness to fabrication imperfections, lower propagation losses and above all, its thermo-optics coefficient, 10-fold lower than Silicon’s, allows the development of temperature quasi-insensitive devices.

Main Results
We successfully demonstrated the integration of SiN in the LETI's silicon photonics platform [2] (see Fig. 1.a). Notably, the SiN is deposited at a low enough temperature (300 °C) to allow compatibility with Si or Ge implanted active devices such as modulators and photodetectors.

![Figure 1](a) SEM image of the platform cross section. (b) Insertion loss of the Si-SiN grating coupler (green line) compared with Si and SiN only couplers (black and blue lines). SiN monomode strip waveguides show reduced propagation losses (0.8 ± 0.3 dB/cm compared to 5 ± 3 dB/cm for Si and SiN waveguides). Furthermore, the SiN thermo-optics coefficient is measured at 1.7x10^-5 K^-1, which is one order of magnitude lower than Si and lower than most previously reported SiN platforms.

In order to be able to manipulate light in both layers, interlayer Si-SiN transitions are designed and measured, showing a great efficiency with losses below 0.1 dB all over the O-band. Taking advantage of the new platform, we designed and measured a bi-layer Si-SiN grating fiber coupler showing a large bandwidth enhancement compared to its pure Si counterpart, as shown in Fig. 1.b. This will prove particularly useful to test CWDM components for which the bandwidth extends over 80 nm.

![Figure 2](a) SEM image of the 400nm-period grating of the SiN Echelle multiplexer. (c) Transmission spectrum of the 20 nm-spaced 4-channels SiN Echelle multiplexer for CWDM applications.

Finally, we report on design, fabrication and test of SiN echelle grating (de-)multiplexers for CWDM [3] (see Fig. 2). It exhibits low average insertion loss (1.5 dB), high inter-channel isolation (~ 30 dB), and a -1 dB channel bandwidth above 8 nm. Moreover, the device shows a very low temperature sensitivity, measured below 13 ppm/°C, thus constituting an ideal candidate for high-performing wavelength de-multiplexing operation in radically different thermal environments.

Perspectives
We have demonstrated a 200 nm Si-SiN platform with passive components; the next step will be to demonstrate the SiN integration with Si active components, such as modulators, and hybrid III-V/Si lasers to develop full transmitter circuits, and to enhance the Left's device library with SiN polarization management devices for receiver circuits. SiN is also intended to be used for other applications and will be included in a future 300 nm photonic platform.

RELATED PUBLICATIONS:
ANNEALING-FREE Si$_3$N$_4$ FREQUENCY COMBS FOR MONOLITHIC INTEGRATION WITH SI PHOTONICS

AUTHORS:
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ABSTRACT:
We report on the fabrication and testing of Si$_3$N$_4$ nonlinear photonic circuits for CMOS-compatible monolithic co-integration with silicon-based optoelectronics. In particular, a novel process has been developed to fabricate annealing- and crack-free Si$_3$N$_4$ 750-nm-thick films for Kerr-based nonlinear functions featuring full thermal budget compatibility with front-end CMOS and Silicon photonics. Frequency comb generation in microring resonators based on such annealing-free silicon nitride films is demonstrated spanning 800 nm (1300 nm - 2100 nm) and counting almost 250 newly generated frequencies. Such milestone paves the way to low-threshold power-efficient Kerr-based broadband sources featuring full thermal processing compatibility with Si photonics integrated circuits (Si-PICs).

SCIENTIFIC COLLABORATIONS: CNRS / Lyon Institute of Nanotechnology (INL), France; Technological University of Denmark (DTU), Denmark

Context and Challenges
Silicon-based photonic integrated circuits (Si-PICs) pave the way towards a brand-new optoelectronics featuring full thermal processing compatibility with cost-effective complementary metal-oxide-semiconductor (CMOS) technology and micro-nano-electronics circuits and nodes. A paradigm shift in optical transmission can be however constituted by exploiting the full potential of X$^2$ nonlinear optical processes to generate Kerr-based optical frequency combs (OFCs). In this way, tens or even hundreds of optical channels can be obtained thus substituting an equal amount of III-V on Si individual laser diodes to be integrated on a chip as illustrated in Fig. 1. However, all prior works based on stoichiometric Si$_3$N$_4$-based OPOs made use of high-temperature annealing (~1200°C) of the nitride film and silica undercladding used to break N-H bonds otherwise causing absorption in the C-band, otherwise severely degrading its nonlinear functionality. As well as that, substrate preparation made by etching crack-limiting trenches in the SiO$_2$ undercladding has been also used to prevent the propagation of tensile strain-related cracks in the nitride film which would deteriorate dramatically the optical quality of the material. Indeed, the use of such annealing is intrinsically incompatible for a monolithic co-integration of such nonlinear circuits on existing Si-based photonics and optoelectronics as, for instance, extreme annealing would destroy the Silicon optical layer underneath along with its functions (modulation, photodetection, etc...). To prevent the aforementioned drawbacks, a novel annealing-free crack-free fabrication process has been developed to deposit such thick nitride-based films for nonlinear optics applications exhibiting front-end process compatibility with CMOS and Silicon photonics integrated circuits (Si-PICs). Such generated broadband sources can be able to provide sufficient aggregate data transmission bandwidth to reach 100’s of Tbit/s and beyond.

Main Results
Optical frequency comb generation. The silicon nitride microresonators based on the annealing-free CMOS-compatible process are shown in Fig. 2. The chips were then continuous-wave pumped via an external C-band EDFA laser + amplifier at 1569 nm wavelength. Quality factors of the microring exceeding 600,000, allowing to reach optical parametric oscillation threshold at 80 mW pumping power. Cascaded four-wave mixing (FWM) processes and parametric gain via anomalous-dispersion-engineered waveguide constituting the microring allow to generate a native-line-spaced optical frequency comb counting almost 250 new generated frequencies over a wavelength span of nearly 800 nm (1300 nm - 2100 nm). Its optical spectrum is reported in Fig. 3. Via such demonstration, we claim the first-time realization of annealing-free silicon nitride frequency comb microresonators, following a tailored deposition method, minimizing the hydrogen content, Our annealing-free and crack-free fabrication process provides our devices with the right specification (microring GVD and characteristics) to underpin Kerr frequency combs, thus representing a significant step toward the full compatibility of Si-Ni-based Kerr-comb sources with the thermal budgets of front-end CMOS and Si photonics processing.

Figure 2: SiN-based waveguides and microresonators for nonlinear parametric amplification.

Figure 3: Kerr-based frequency comb generation spanning 1300 nm - 2100 nm in front-end CMOS-compatible Si$_3$N$_4$ µrrings.

Perspectives
Current research is focused on both material and technology optimization to reduce the parametric threshold power dramatically.

RELATED PUBLICATIONS:
LASING IN OPTICALLY PUMPED GeSn PHOTONIC CRYSTALS

AUTHORS:
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ABSTRACT:
Germanium based materials can overcome some limits inherent to standard Silicon Photonics devices and be used notably in Mid-Infrared sensing applications and Network-On-Chip applications. One of the main challenges in this field is to transform the indirect group-IV semiconductor bandgap to a direct one using high tensile strains or by alloying germanium with tin. We lately demonstrate lasing in optically pumped GeSn photonic crystal membrane with 16% Sn content. The active $\text{Ge}_{0.84}\text{Sn}_{0.16}$ layer is grown on a step-graded GeSn buffer, thus limiting the density of the misfit dislocations. Obtained thresholds (227 kW/cm$^2$ at 15 K to 340 kW/cm$^2$ at 60 K) are comparable to our previous works indicating the robustness of GeSn optical gain.

Context and Challenges

Si photonics is advantaged by its full compatibility with the current massively produced Si complementary metal-oxide semiconductor (CMOS) technology. Lately, germanium (Ge) based materials appeared to be a good candidate to tackle the current limitations of Si, since it is also fully CMOS compatible. Recent progresses in Chemical Vapor Deposition (CVD) allowed to grow in LETI high Sn content in the Ge crystalline matrix. A direct bandgap can be obtained in GeSn if the Sn content is high enough and the residual compressive strain low enough (when grown on Ge). The low thermal stability of GeSn alloys requires a careful selection of process parameters during epitaxy. Recent studies have demonstrated lasing in optical cavities made with Ge$_{1-x}$Sn$_x$ alloys. So far, lasing were reported in Fabry-Perot cavity [1] and in micro-disk cavity [2].

Main Results

We investigated the benefit of using photonic crystals structures that contain some guided modes with group velocities approaching zero. The slowing down of the light propagation enhances light-matter interaction, which a favourable condition to achieve lasing effect. This effect is known in literature as band-edge lasers.

The GeSn layers were grown in a 200 mm Epilux Centura 5200 Reduced Pressure-Chemical Vapor Deposition (RP-CVD) cluster from Applied Materials. The growth was carried at reduced temperatures – between 300°C and 350°C. The optically active layer was grown on top of a thick Ge strain relaxed buffer, with Ge$_{0.42}$Sn$_{0.58}$ flux ratio modified during the process to create discrete concentration ramp– referred here as “GeSn step-graded buffer”– before reaching the target concentration of Sn (16%). This method helps to relax partially the compression in the GeSn layer, while capturing misfit dislocations at the interfaces inside the graded buffer (instead of propagating them towards the surface), thus preserving the crystalline quality of the partially relaxed $\text{Ge}_{0.84}\text{Sn}_{0.16}$ optical layer [3].

We developed processes on (i) GeSn anisotropic etching and (ii) isotropic selective etching of Ge versus GeSn to get suspended photonic crystals structures (Figure 1). Highly selective under etching was achieved even for GeSn with a Sn content as low as 6% (selectivity of 57 for 6% Sn layers, and 433 for layers with 8%) [4].

Perspectives

Our results confirm the robustness of GeSn optical gain for lasing applications, despite a high surface/volume ratio of the photonic crystal membrane. Surface passivation and carrier confinement using SiGeSn/GeSn heterointerfaces and/or multi-layer structures will be later used to enhance the $\text{Ge}_{1-x}\text{Sn}_x$ radiative recombination efficiency.

RELATED PUBLICATIONS:
HYBRID III-V/Si DFB LASER INTEGRATION ON A 200 MM FULLY CMOS-COMPATIBLE SILICON PHOTONICS PLATFORM

AUTHORS:
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ABSTRACT:
In this work we demonstrate the first integration of a hybrid III-V/Si laser in a fully CMOS compatible 200nm technology. Device with SMSR up to 50 dB and a maximum output power of 4mW coupled in the waveguide have been measured. The fabrication flow is fully planar and compatible with large scale integration silicon photonics circuit. The conventional Au-based contacts used in III-V laser are replaced by Ni-based alloyed contact with no penalties on the series resistance.

Context and Challenges
Silicon photonics platforms are becoming more and more mature with competitive devices suitable for increasing needs of HPC (High Performance Computing) systems and datacenters. However, compared to bulk III-V technologies, Si photonics technologies are suffering from the lack of integrated light source. Several works have been done in the past years to integrate laser on silicon using III-V direct bonding on top of patterned silicon. Although, these demonstrations relied on CMOS-compatible process for the silicon part, all the process steps following the introduction of the III-V material were carried out with small wafer diameter III-V fabrication lines [1]. With such integrations, the cost advantage of silicon photonics based on the use of CMOS platforms and large wafer format is no more valid. It is therefore necessary to propose the same kind of III-V on silicon hybrid device integration using CMOS compatible technology on 200 or 300mm wafer.

Main Results
In this work we present, to the best of our knowledge, the first monolithic integration of a fully CMOS compatible hybrid DFB laser on a 200mm silicon photonics platform is demonstrated. A damascene process is used to locally increase the silicon thickness in order to have the 500nm thick silicon layer needed for the hybrid laser. This approach leads to a modular integration scheme, the laser being really an optional device of the overall platform, keeping the same silicon substrate with or without laser integration. The novelty here also relies on the use of innovative laser electrical contacts which do not contain any noble metals such as gold and for which integration “lift-off” based process are prohibited [2]. Thanks to these properties, the contacts are using a planarized BEOL and are CMOS-compatible both in terms of composition and integration scheme. Figure 1 is showing a tilted SEM picture of the device before encapsulation and an optical top view of the device under test.

Figure 1: Tilted SEM view of the III-V/Si DFB laser after the IIIV patterning steps (left). Optical microscope views of the Hybrid III-V/Si DFB laser under test probe (right)

A typical laser spectrum is shown in Fig. 2 reflecting its single-wavelength laser operation. A Side Mode Suppression Ratio (SMSR) of 50 dB has been measured, proving the good spectral purity of this laser. The laser central wavelength is 1300nm, slightly shifted vs. the optimum of the output grating coupler (see insert of Fig 2) which add a noticeable power penalty to the fiber. The typical output power measured in the single-mode fiber is in the range of 150μW (maximum 400μW). Taking into account the grating coupler loss, it corresponds to a typical output power of 1.5mW coupled in the silicon waveguide (maximum 4mW). The lasing threshold current is stable between 50mA and 65mA. The series resistances are in the range of 10Ω which is in line with device fabricated with non-CMOS compatible process and materials. These results therefore validate the integration and the choice of fully CMOS-compatible Ni-based alloys as III-V metallization.

Figure 2: Laser spectrum at 160 mA injection currents. In insert is the transmission test of the grating couplers used as output of the laser. Peak wave length is at 1320nm. Around 10 dB loss per grating are measured at 1300nm

Perspectives
The monolithic integration of a fully CMOS compatible hybrid DFB laser on a 200mm silicon photonics platform is demonstrated. Only CMOS compatible process are used resulting in a fully planarized technology on which a multi metal level BEOL can be fabricated for large scale integration. The conventional Au-based contacts used in III-V laser are replaced by Ni-based alloyed contact with no penalties on the series resistance. Future works will concern the implementation of optimized designs taking into account the use the amorphous silicon to improve the emitted power level. Two metal levels routing will also be used to improve the current driving capabilities and reduce furthermore the series resistance.

Acknowledgment
The research leading to these results has received funding from the French national program ‘programme d’Investissements d’Avenir, IRT Nanoelec’ ANR-10-AIRT-05

RELATED PUBLICATIONS:
**DIRECT MODULATION ENCHANCEMENT OF HYBRID III-V ON SILICON LASERS WITH SILICON RING FILTERS FOR CHIRP MANAGEMENT**

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**ABSTRACT:**
The use of a micro-ring resonator (MRR) to enhance the modulation extinction ratio and dispersion tolerance of a directly modulated laser is experimentally investigated with a bit rate of 25 Gb/s as proposed for the next generation data center communications. The investigated system combines a 11-GHz 1.55-µm directly modulated hybrid III–V/SOI DFB laser realized by bonding III–V materials (InGaAlAs) on a silicon-on insulator (SOI) wafer and a silicon MRR also fabricated on SOI. Such a transmitter enables error-free transmission (BER < 10−9) at 25 Gb/s data rate over 2.5-km standard single mode fiber without dispersion compensation nor forward error correction.

**SCIENTIFIC COLLABORATIONS:** DTU, NETLAB, FOTON, III-V LAB, KTH

**Context and Challenges**
The traffic in data centers has been steadily growing to fulfill the ever increasing customer demand and this has pushed research towards finding energy- and cost-effective solutions capable of reaching modulation speeds higher than the current standard of 10 Gb/s [1]. Transmission at 25 Gb/s over standard single mode fiber (SSMF) has been proposed as next target to be included in the IEEE 802.3 standard. In this perspective, directly modulated lasers (DMLs) have been recognized as good candidates to address these needs. We show in this work the enhancement of modulation speed of DMLs obtained with a silicon ring resonator filters.

**Main Results**
We report on an all-on-silicon transmitter operating at the target bit rate of 25 Gb/s. This is achieved by combining a directly modulating III-V/Si hybrid DFB laser and an optimized silicon MRR filter [2].

The hybrid III-V on silicon laser was fabricated on a 200-mm CMOS line starting with SOI wafers having a silicon top layer thickness of typically 440 nm. A patterning of the silicon is performed in order to define all the passive circuitry, including Bragg gratings used to realize an hybrid distributed feedback laser (DFB) cavity. In parallel, a 2" InP wafer containing multiple quantum well layers is grown. Next this III-V gain material is subsequently bonded onto the silicon wafer through molecular bonding, prior to the III-V patterning (gain, mesa, and electrical contacts). The fabricated laser is ready for wafer level probe testing using silicon vertical grating coupler as access for the optical probe. For this demonstration, a silicon micro-ring resonator (MRR) was realized on a second chip, as depicted in the Figure 1. The MRR parameters were optimized numerically in order to maximize the optical modulation amplitude (OMA) of a 25-Gb/s signal affected by transient and adiabatic chirp after filtering it, with free spectral range (FSR) of 100 GHz. The FSR value was chosen to potentially allow for simultaneous filtering of multiple FSR spaced WDM channel in a N × 25 Gb/s laser array.

The dynamic characterization setup is shown in Fig. 1. The hybrid III-V/Si DFB laser was biased at 138 mA and directly modulated at 25 Gb/s with a 27 –1 non-return-to-zero (NRZ) pseudo-random binary sequence (PRBS) generated by a bit pattern generator with a peak-to-peak voltage of 3.4 V.

After direct modulation, the optical signal was coupled to the silicon MRR for ER enhancement through optical filtering. The laser bias current was adjusted to match the MRR resonance for suppression of the low-frequency content of the modulated optical spectrum.

**Figure 1:** Experimental setup for dynamic characterization of the DFB laser at 25 Gb/s. After ER enhancement by the MRR, the optical signal was transmitted over up to 2.5 km of SSMF and received by a standard preamplified receiver connected to an error analyzer for bit-error ratio (BER) measurements and to a sampling oscilloscope for eye diagram monitoring. The recorded eye diagrams are shown in Fig. 2. Considering first the back-to-back (B2B) scenario, it is possible to observe how the modulation ER is enhanced by the suppression of the signal ‘0’ level by the MRR. The ‘0’ level decreases getting closer to the yellow dashed line showing the oscilloscope ground level. This corresponds to an enhanced eye opening and an improvement in the ER from 3.8 dB to 6.8 dB.

**Figure 2:** Eye diagrams of the 25 Gb/s signal for back-to-back and after transmission over 1, 2 and 2.5 km of SSMF with and without MRR filtering.

In this perspective, it is clear how the MRR filtering also enhances the signal dispersion tolerance. In fact, even if the dispersion effects are visible in all the eye diagrams, for the MRR filtered signal the eye remains open for a transmission distance up to 2.5 km.

**Perspectives**
As both DFB laser and MRR have been fabricated on the SOI platform, combining the two devices can provide a compact all-silicon transmitter suitable for data center applications [3].

**RELATED PUBLICATIONS:**
DEMONSTRATION OF A SILICON PHOTONICS BASED OPTICAL NETWORK UNIT FOR FTTH/PON

AUTHORS:

ABSTRACT:
Within the European project FABULOUS, we achieved the transmission experiments of a self-coherent reflective PON (Passive Optical Network), demonstrating 500 Mbps per user with a power budget of 24 dB in off-line processing and 21 dB in real-time. The transceiver module, aiming at being implemented in a Fiber To The Home (FTTH) Optical Network Unit (ONU), integrates a Silicon Photonics Circuit with a dedicated driver Electronic chip.

Context and Challenges
Fiber-To-The-Home (FTTH) Networks are among the most challenging applications for optoelectronic modules in term of integration and mass manufacturability. The FABULOUS European Project proposes a novel Optical Network Unit (ONU) for such Networks, relying on Silicon Photonics (SiPho) Circuits and dedicated driving CMOS electronics hybrid Integration, using flip-chip. The architecture has already demonstrated, with discrete optical components and the off-line processing approach, to be capable of granting an aggregate capacity of 32 Gbps per wavelength compatible with new standards like XG-PON ODN class N2. Within the FABULOUS project, an integrated SiPho module has been demonstrated.

Main Results
The tested demonstrator is made of a Silicon Photonics circuit with a Reflective Modulator, enabling Frequency Division Multiple Access (FDMA) transmission. The required CMOS driver has been designed and manufactured by ST Microelectronics, while the SiPho Circuit has been designed and manufactured by CEA-LETI’s 200mm Silicon Photonics platform, using SOI (Silicon-On-Insulator) wafers. It is made of a Reflective Mach Zehnder Modulator (R-MZM) with segmented electrodes, exhibiting a Vₘₙₖₙ of 2 V/cm and an E/O bandwidth of 20 GHz when biased at −1 V [1].

The SiPho circuit was hybrid assembled with the driver using a flip-chip assembly method with interconnects made of Copper pillars. The resulting optical engine has been packaged by UCC Tyndall to form a testable module, made of a PCB with front-end electronics, and with temperature stabilization provided by a thermo-electric cooler (Figure 1). Optical Fibers have been aligned and glued to the SiPho circuit to enable system level tests (Figure 2), with two FPGA emulating a Central Office and a Network User.

Figure 1: the packaged FABULOUS module (a), with Zoom-in of the optical engine (b). Further zoom-in showing the many discrete copper pillar bumps used to interconnect the driver to the SiPho circuit (c), and Microscope image of the copper pillar cross section (d).

Figure 2: FABULOUS real-time experimental setup (left), with the measured constellation at 300MBd QPSK (right).

We demonstrated the feasibility of a reflective ONU with an unprecedented level of optical integration, achieving 300 MBaud QPSK transmission [2] leading to a useful resulting bit-rate of 500 Mbps per user. The use of QPSK provides more robustness with respect to the laser linewidth, which can be a sensitive parameter in this system.

Perspectives
For the first time, an integrated Silicon MZM is operated in real time over the FDMA PON proving that the different important features demonstrated with discrete components (reflective polarization insensitive carrier suppressed modulation) can be obtained at low cost and high production volume with a fully integrated silicon ONU. This experiment assesses Silicon Photonics as a promising technology, for next generation Passive Optical Networks, especially future standards requiring higher bandwidth and date rate per user (e.g., 25 Gbps PON) and also for future Central Office to Base Station optical interconnects in 5G Networks.

RELATED PUBLICATIONS:
- Si nanostructured µ-hotplates
- Si photoacoustic cell analyze multiple gases
- Mid-infrared photonic integrated circuits
NANOSTRUCTURATION OF A SUSPENDED HOTPLATE: IR-EMISSION EFFICIENCY MULTIPLIED BY 2.

AUTHORS:
P. Barritault, E. Lorent, S. Boutami, A. Lefebvre

ABSTRACT:
In this letter, we present an IR emitter based on a freestanding hotplate coated with an array of tungsten nanostructures. The characterization of this hotplate, which follows its manufacturing in Leti’s facilities, demonstrates a two-fold gain in the electrical to optical efficiency at the target wavelength of 4.26 µm. This IR emitter, when used as the µSource of a CO2 NDIR based sensor, greatly helps reducing the power consumption of the sensor. This is of key importance in order to obtain the autonomous sensors required in Air Quality Monitoring. We are further developing this type of solution for the startup eLichens our joint lab partner.

SCIENTIFIC COLLABORATIONS: this work was supported by the National Research Agency (ANR) via project IDEE.

Context and Challenges
In the field of Air Quality control, a common solution to monitor certain gas, such as CO2, is based on the measurement of IR gas absorption; the so-called Non Dispersive Infra-Red (NDIR) Sensors. These sensors need to be autonomous, and thus to have a low power consumption. Most often, the IR source used, a black body, has the biggest contribution in terms of power consumption, and therefore, increasing the IR source efficiency is particularly relevant to obtain an autonomous sensor. We present below a µSource IR emitter, developed at Leti [1], with an improved efficiency.

Main Results
This µSource is a freestanding hotplate, consisting in a micro-structured conductive track sandwiched between two dielectric layers. By applying a current through the track, Joule effect heats the membrane at a typical temperature of 650 °C thus enabling IR emission. More recently, we were able to improve significantly the efficiency of the source by only adding a few steps to the standard µSource process. We have implemented on top of the µSource an array of tungsten squares (width 700 nm, thickness 100 nm and pitch 2.5 µm). This stack forms a so-called Metal-Insulator-Metal (MIM) resonant structure. The µSource when heating will emit light more specifically at a resonant wavelength, which in our case corresponds to the CO2 maximum absorption: 4.26 µm.

We manufactured the nanostructured µSources in Leti’s facilities on 200 mm wafers. In Figure 1, we present a photography of the µSource along with a MEB image of the W-nanostructures.

Fig. 1: µSource released (left) and W nanostructurations (right)

The µSources IR emission spectra were then measured showing the MIM resonance effect (see Figure 2): for the same input electrical power, a two-fold gain, at 4.26 µm, is obtained for nanostructured sources as compared to non-nanostructured ones.

Let us add that it is possible to tune the resonance wavelength or enlarge its width by modifying the dimensions of the nanostructures. Finally, in order to evaluate the dispersion over a wafer, we measured the electrical and optical (@ 4.26 µm) characteristics of the µSources on an automatic prober. The Fab yield measured is over 90% and the dispersion on optical power is below 10%. This last point is encouraging since it shows that the dispersion on the W-dots width, inherent to technological process, has a limited impact on the optical properties of the source.

Perspectives
We are currently pursuing this work through our joint lab with the start-up eLichens [2]. The goal is to increase the process maturity before transferring it to a foundry. The next step will be to process nanostructured µSources along with a Vacuum Wafer Level Packaging (WLP). This will reduce by 20-folds the electrical consumption of the source, for the same output optical power.

RELATED PUBLICATIONS:
PHOTOACOUSTIC CELL ON SILICON FOR MID-INFRARED QCL BASED MULTIGAS SPECTROSCOPIC ANALYSIS

AUTHORS:

ABSTRACT:

Photoacoustic cells are one type of optical sensors that can be used to detect gas traces. The photoacoustic spectroscopy technique is based on the absorption of photons by the molecules of interest and the subsequent creation of acoustic waves. Our new miniature silicon-based photo-acoustic cell combined with a quantum cascade laser exhibited high performance sensitivity. This new generation of photoacoustic cell open the gate to a cost effective sensor and mass production market.

Context and Challenges

PhotoAcoustic Spectroscopy (PAS) is one of the most sensitive techniques used to monitor chemical emission or to detect gas traces [A. Miklós et al., Rev. Sci. Instrum., vol. 72, no. 4, pp. 1937–1955, Apr. 2001]. In particular, in the Mid InfraRed (MIR), many gases of interest have their strongest absorption lines. We have demonstrated [1, 2] our centimetric PA-device can compete with bulky systems for multi-gas sensing without any compromises on performances. Today we have bring this technology on silicon enabling dramatic cost reduction and extreme integration of this high performance gas sensor.

Main Results

First, a complete new design has been achieved using Finite Element Modeling. Our acoustic model based on the Navier-Stokes equation taking in account the losses (surface, volume), enables to set the dimensions of the photoacoustic cell for maximizing performances.

The cells have been fabricated using our 200mm pilot line using standard processes (see figure 1).

Several wafers have been released. We have tested single chips on our reference CO2 test bench facility. The photoacoustic cells feature a very good matching with the simulation regarding the resonance frequency response (see figure 2). Moreover the miniPA cell on silicon exhibits a sensitivity down to the ppm level in a gas flow.

Perspectives

The miniPA concept is being extended to an integrated multigas detector achieved in collaboration with the start-up mirSense (www.mirsense.com) under a joint laboratory (the multigas sensor from mirSense is shown in figure 3). We are focusing our development on the TRL improvement of this ultra-small cell assessing various conditions (temperature, hygrometric, aggressive gas, etc.).

Figure 1: Scale of the miniPA cell

Figure 2: Photoacoustic wavelength modulation absorption spectroscopy with 1f and 2f detection on CO2 absorption line at 2302 cm⁻¹.

Figure 3: Picture of the compact QCL based sensor multiSense from mirSense

RELATED PUBLICATIONS:
MID INFRARED PHOTONIC INTEGRATED CIRCUITS

AUTHORS:
J-M Fedeli, P Labeye, A Marchant, O Lartigue, M Fournier, J-M Hartmann (DTSi)

ABSTRACT:
For small gas system systems based on QCL arrays, we have developed two technology platforms for the fabrication of AWG with more than 35 inputs in the bands 3µm-8µm and 8-12µm with SiGe core clad with Si or Ge core clad with SiGe.

Context and Challenges
Gas analysis in the Mid-Infra-Red wavelength region, also called the fingerprint region, allows to address a unique combination of fundamental absorption bands that are of orders of magnitude stronger than in the near IR. This feature enables highly selective, highly sensitive unequivocal identification of chemicals. Indeed, many molecules have strong and distinct absorption lines in the Mid-IR giving much interest to spectroscopic detection. With the recent progress in Quantum Cascade Laser (QCL) and Interband Cascade Laser (ICL) technologies, compact and reliable Mid-IR light sources are becoming available. In particular, specific emission wavelengths can be selected through Distributed FeedBack (DFB) QCLs in order to target the chemicals of interest.

Main Results
In this approach, the spectroscopic analysis uses a Mid-IR multi-wavelength source formed by an array of QCL lasers coupled to the multiplexer. This Photonic Integrated Circuit (PIC) is used to deliver each wavelength on a specific output. In order to address the 3-12µm QCL spectral range, our group developed two silicon photonics technologies. We designed Arrayed Wave Guide (AWG) type multiplexers using a fast design tool based on a Gaussian approximation of waveguide fundamental mode and Fourier diffraction optics. Dimension fluctuations were taken into account in order to guarantee a good fabrication reproducibility. For the 3-8µm band, we selected a SiGe 40% core waveguide surrounded by Si. Basic passive devices (lines, bends, and splitters with Multi-Mode Interferometers) were first characterized in order to verify the quality of fabrication and to calibrate the testing apparatus. An ultra-low waveguide loss was estimated by the spirals method at 0.3 dB/cm. The Arrayed Wave Guide (AWG) presented a low loss normalized transmission (~1.6 dB) with a cross talk below -12 dB [1].

RELATED PUBLICATIONS:

Perspectives
These technologies are now offered to customer via the MIRPHAB pilot line [4]. Under new projects, more integrated devices will be searched as well as high performance non-linear ones.
• Size governs non-radiative losses in pixelated LEDs
• 3D-stacked pixelated wireLEDs
SHOCKLEY-READ-HALL AND AUGER NON-RADIATIVE RECOMBINATION IN GaN BASED LEDs: A SIZE EFFECT STUDY

AUTHORS:
F. Olivier, A. Daami, C. Licitra (DTSi), and F. Templier

ABSTRACT:
We investigate in this study the LED size influence on the radiative and non-radiative recombination [1]. The standard ABC model has been widely used to describe the efficiency of GaN based LEDs. Using this model, we extract A, B and C coefficients for various LED sizes showing how the competition between radiative and non-radiative recombination processes varies with LED geometry. Time-resolved photoluminescence allows us to determine coefficient B, related to radiative recombination. Through current-voltage-luminance characterizations we determine parameters A and C related to Shockley-Read-Hall (SRH) and Auger recombination. We find that coefficient A is strongly dependent on LED size, indicating a drastic effect of sidewall defects on the performances of LEDs. On the other hand, coefficient C is independent of LED size. This latter result demonstrates that efficiency droop does not depend on LED size.

Context and Challenges
GaN-based light-emitting diodes (LEDs) are very promising light sources for lighting and display applications. The growing interest for wearable devices and their numerous applications (augmented reality, head-up displays, etc.) have highlighted the need for high-performance micro-displays. Today’s smaller pixel pitch in LED micro-displays is typically 10µm [2]. As a result, the comprehension of the relationship between size and performances of a LED is an important subject to tackle. LED efficiency is a competition between radiative and non-radiative recombinations A common method to modelize such effects is known as the ABC model. In this work, we propose an extraction method to determine A, B and C coefficients, allowing the analysis of GaN-based LEDs efficiency, for different sizes ranging from 500×500 to 4×4 µm².

Main Results
According to the ABC model, the internal quantum efficiency (IQE) is expressed in terms of coefficients A, B, C and the carrier concentration n as:

\[
\text{IQE} = \frac{B_n n}{A_n n + B_n n^2 + C_n n^3}
\]  (1)

while current density J is expressed as:

\[
J = q w (A_n n + B_n n^2 + C_n n^3)
\]  (2)

where w is the total quantum wells thickness; and q is the elementary charge.

We here assume that Auger recombination is the cause of the efficiency droop. First, B has been calculated by plotting the normalized TRPL intensity decay curve at 5K. After extraction, we obtained a value of \(B = 1 \times 10^{-3} \text{ cm}^2 \text{ s}^{-1}\) which is in good agreement with literature values.

In order to extract coefficients A and C, we have performed IVL characterizations for various LED sizes, which allows to determine the external quantum efficiency (EQE), defined as:

\[
\text{EQE} = \frac{(P_{\text{max}} - P)}{(h \nu) \text{LED}}
\]

where LEE is light extraction efficiency. We have determined a value of 14% for LEE for our structures.

From above equation we can calculate the IQE for all measured devices.

Using expressions (1) and (2), we can express the carrier density n as:

\[
n = \sqrt{\left(\frac{\text{IQE}}{J(q w B)}\right)}
\]

Putting, \(Y_1 = J/q w, X = \sqrt{\left(\frac{\text{IQE}}{J(q w B)}\right)}\), \(\alpha = C/B^{1/2}\), and \(\beta = A/B^{1/2}\) we obtained a simplified expression of IQE written as:

\[Y_1 = \alpha X + \beta X^1\]

This equation implicitly shows that coefficient A (hence \(\beta\)), respectively C (hence \(\alpha\)), will have an important effect at lower, respectively higher, current densities. Therefore the extraction of parameters A and C can easily be undertaken under different current density ranges by neglecting in equation (6) one parameter or the other, which finally gives us two adjusting simple equations:

\[Y_1 = \alpha X + 1\]

and \(Y_2 = \beta X^1\) where \(\alpha\) and \(\beta\) are related to high, respectively low, current densities.

Following the adjustment with above equations we can determine coefficients A and C. We have determined values of \(A = 3.7 \times 10^6 \text{ s}^{-1}\) and \(C = 2.6 \times 10^{31} \text{ cm}^3 \text{ s}^{-1}\), for a typical LED size of 100 x 100 µm². These extracted values are in good agreement with those published for InGaN/GaN blue LEDs for both A and C values.

We plot on the figure below the experimental IQE data of the 100 x 100 µm² sized LED and its adjustment by the ABC model after determining all coefficients. We obtain a good fit of all data in all current ranges. At low current density, the small mismatch between experimental data is mainly attributed to the experimental error in the measurement of very low optical power mainly due to intrinsic dark current of the measuring photodiode.

With parameters A, B and C fixed, we can now get back to the carrier concentration at each current density level, using equation (5). This gives us values ranging from \(6 \times 10^{10} \text{ cm}^2\) to \(3 \times 10^{11} \text{ cm}^2\), which is in accordance with typical values of carrier density in GaN LEDs.

Perspectives
In summary, we have determined recombination coefficients of the ABC model on different LED sizes by IVL and TRL measurements. Parameter B is calculated from time resolved photoluminescence decay through the measurement of carrier lifetime at 5K, while parameters A and C are determined by a simple extraction method based on IVL characterization. This model is particularly well suited for the study of GaN-based LEDs size effect. We have shown that non radiative SRH-like recombination is related to the LED perimeter and intensifies as LED size decreases. Meanwhile, coefficient C generally related to Auger effect, has been found to be a constant whatever the pixel size is, proving that efficiency droop is mostly related to the quality of the InGaN/GaN epitaxy.

RELATED PUBLICATIONS:
3D STACK HIGH VOLTAGE WIRELEDS : INVESTIGATIONS ON THERMAL, PROCESS DEVICE AND PACKAGING ISSUES

AUTHORS:
B. Chambion, B. Bouillard, A. Gasse, A. Vandeneynde, N. Ait-Mani, A. Gueugnot, B. Bouillard, M. Volpert, B. Soulier, D. Henry, F. Mercier (ALEDIA), P. Rueda (ALEDIA), V. Beix (ALEDIA), T. Lacave (ALEDIA)

context and challenges
Solid State Lighting systems need compact and reliable packaging technologies to be implemented. A 3D-stacked pixelated wireLED flip chip bonded onto a dedicated ASIC is proposed to target a direct high voltage AC LED. The high voltage wireLED is flip chip bonded on a dedicated ASIC. With this we reach a high level of packaging integration into a 6.7*3.9*1 mm package, directly pluggable on 230 volts AC power supply. However in this configuration the thermal management of the package becomes crucial.

Main Results
For the thermal study, we have tested various solder bumping patterns with a dummy thinned silicon die (thermal load) on a dedicated readout circuit.

Along the red line (figure above) are some pixels with and without bumps, which strongly impacts thermal dissipation. Comparing finite element modelling with IR measurement, we exhibit a good agreement with only 11% difference located in the “no bump” area.

Figure 3: Comparison between IR measurement and simulation

We have also implemented wireLEDs on the same vehicle test where pixel LEDs line can be driven separately or in series to target 230 V.

Perspectives
Next to this reliable thermal modelling of a 3D stack and first wireLEDs lighting demonstration, we will transfer the process to a dedicated ASIC enabling to drive the LED pixel lines in accordance with a 230V direct AC.

RELATED PUBLICATIONS:
• Intraocular projection display
• High-resolution GaN LED μ-display
• Thin-film packaging of OLED μ-displays
• Curved OLED μ-displays
• In-plane-switching liquid-crystal modulator matrix
HOLOGRAPHIC RECORDING SETUP FOR INTEGRATED SEE-THROUGH NEAR-EYE DISPLAY EVALUATION

AUTHORS:
Chr. Martinez, V. Krotov, D. Fowler

ABSTRACT:
We present a design of a hologram recording setup used to evaluate a concept of near to eye see-through display. Our goal is to record a set of hologram element distributions related to a given image pixel orientation sequence. The recovery of the hologram should project a static image into the eye by a self-focusing effect.

Context and Challenges
Holographic optical Elements (HOE) are often used in see-through devices due to the spectral selectivity of the hologram. Bragg selectivity allows the coding of optical function at a specific wavelength without jeopardizing the device transparency on the remaining visible spectrum. Various schemes have been developed for Augmented Reality displays based on holography (C. Jang et al., Appl. Opt. 55, A71-A85 (2016)).

The concept we propose is based on a coherent integral imaging scheme and on the use of 2D waveguides. The role of the hologram is to produce a distribution of emissive points that direct a wave front at a specific angle towards the eye. The image is then formed by a self-focusing effect into the eye [1].

As a general problem in holographic devices, the recording setup has to be carefully designed in order to produce the required interference distribution in a configuration as close as possible to the real device implementation. We have designed a free space holographic set up to validate the concept of a multiple holographic element (hoel) distribution. The goal is to manufacture a sampled hologram that could project an image directly into the eye when addressed by the appropriate reference beam sequence.

Main Results
First studies have been dedicated to the choice of the optical elements of the recording set-up [2]. We have shown that a compromise is necessary between the size of the hologram and the viewing angle of the hologram. A first set of lens parameters led to the combination of 14 mm for the hologram diameter and 14° for the viewing angle.

The recording setup has been recently built and will integrate soon all the motion control elements to implement our hoel distribution concept (figure 2a). A collaborative contract has been established with Holococept, a French holographic material supplier. A set of holograms has been recorded on our set-up with this material. First results show a good material response in terms of efficiency (> 90%, figure 2b).

Perspectives
Our next developments concern the implementation of the hoel segmentation on the holographic material. This will allow us to evaluate experimentally at short term the self-focusing effect in a device similar to the near-eye display we investigate. At midterm the holographic recording process will be implemented in conjunction with our 2D waveguide design to evaluate the physical interaction between guided-mode and holographic free space propagation. In a more general perspective the holographic recording set-up will be used to investigate innovative HOE designs for a large variety of applications.

Figure 1: Description of the hologram recording set-up.

Figure 2: a) photography of the hologram recording set-up currently built on the laboratory, b) reflection spectra of a hologram recorded in the laboratory (thickness 9 µm, index change amplitude 3.2 10^-2).

A NOVEL PROCESS FOR FABRICATING HIGH-RESOLUTION AND VERY SMALL PIXEL-PITCH GaN LED MICRODISPLAYS.

AUTHORS:

ABSTRACT:
A new approach for fabricating very-small pixel pitch GaN microdisplays is proposed. It is based on the principle to bond directly an epitlayer onto a CMOS wafer. MicroLEDs are then directly patterned on the wafer using the high-precision silicon line tools. Using this approach, we have demonstrated that MicroLEDs obtained from silicon grown epi GaN layers exhibit performances comparable to those obtained on classical sapphire templates. This technology shows very great promises in the fabrication of high brightness, ultra-high-resolution microdisplays required for augmented reality systems.

Context and Challenges
The growing interest for wearable devices has highlighted the need for high-performance microdisplays. To address this demand, inorganic GaN LED based arrays appear as a promising technological option [1]. Such microdisplays can be fabricated using hybridization of a GaN array on sapphire with CMOS active matrix. It has been already demonstrated that using microtube hybridization technology it is possible to reduce the pitch down to 10 µm [1]. However, for high-brightness LED microdisplays, there is a need for a much smaller pixel pitch, typically 5 µm or even 2 µm. Therefore, a new integration strategy for fabricating these GaN LED microdisplays is required. Recently, we have proposed a new approach for the fabrication of high-brightness LED [2], and here we report new results on this promising approach [3].

Main Results
On a first series of wafers, matrices of GaN microLEDs with different size and spacing were patterned using classical lithography and dry etching. No post-metallization has been applied. Arrays of MicroLEDs as small as 2 µm with a spacing of 1 µm were fabricated and operated successfully [2]. However, the lack of top-metal limited the On-current at higher voltages. Therefore it was decided to fabricate new devices with an n-contact metallization.

On a second series of wafers, Indium Tin Oxide (ITO) was deposited on top of the structures to provide an n-type contact. The transparency of ITO is well suited to permit the top-emission of structure by ensuring a wide current spreading without affecting the light emission. GaN microLEDs with different size and spacing were then patterned using standard lithography and subsequent dry etch of ITO and GaN layers. Figure below shows the current-voltage characteristics of a microled (3µm size) fabricated using this new approach (GaN/Si) with ITO as the contact layer on N-type GaN. We compare it to a reference pixel (5 µm size) fabricated directly on sapphire and having both n and p-type metallizations.

The GaN/Si microLED shows a comparable turn-on voltage of about 2V, and comparable current levels to the GaN/sapphire microLED up to 1mA. This important result is mainly due to the contribution of the ITO layer on top of the n-type GaN. However, the GaN/Si 3µm microLED exhibits a slightly higher leakage current, which is interpreted as peripheral leakage due to the absence of passivation of the pixel mesa sidewalls in these first generation devices.

Perspectives
This work demonstrates the feasibility and improvement of high-resolution and very-small pixel pitch high-brightness GaN microdisplays. It highlights the feasibility of very small pixel pitch (3 µm) microLED arrays from GaN epi layers grown on silicon wafers. Not only these are the smallest pitch microLED arrays achieved in the world to our knowledge, but these devices exhibit performances at least equivalent to those fabricated directly on sapphire. Furthermore, using this novel process integration, the devices are entirely fabricated using a CMOS line, which simplifies significantly the supply chain and paves the way for future low cost, mass production of GaN-based microdisplays. This technology is very promising for fabricating high-brightness, ultra-high-resolution microdisplays, which are necessary for new applications such as wearable devices, advanced Head-up display (HUD) systems and compact projectors.

RELATED PUBLICATIONS:
UV-CURABLE THIN-FILM PACKAGING FOR OLED-BASED MICRODISPLAYS

AUTHORS:
M. Provost, T. Maindron, A. Suhm, K. Raulin (Polyrise SAS), V. Gaud (Polyrise SAS)

ABSTRACT:
A thin-film Hard-Coat (HC) layer was investigated for the collective encapsulation and mechanical protection of top-emission OLED micro displays on wafer-scale and as an alternative solution to individual glass-lid protection. The HC is fabricated by UV-curing process from a silica-based hybrid polymer synthetized by sol-gel process.

Context and Challenges
It is widely known that organic light emitting diodes (OLEDs) are highly sensitive to moisture and oxygen ingress and require high barrier encapsulation. Moreover, a specific protection needs to be added to protect the device from mechanical failure. Depending on the application, various options from glass lids to flexible barriers have been developed. However, the former offers high mechanical protection but suffers from long implementation processes, while the later typically exhibits low hardness and poor wear resistance. This work aims to develop an alternative packaging solution using a thin-film HC layer directly processed onto OLED displays by photolithography [1].

Main Results
After the deposition of our HC protective layer at the wafer scale, the silicon wafer is diced under constant cooling water stream to obtain individual OLED chips. No major degradation such as scratches or stuck silicon residues can be observed. It turns out that the HC efficiently protects the ALD encapsulation layer from mechanical failures. Moreover, the HC shows a full chemical resistance to organic solvents used for surface cleaning. No solid residues were found surrounding the pattern. As a result, the hybrid encapsulation allows the easy electrical contact bonding of the display, using probes and wire bonding process.

Preliminary electro-optical caracterizations were performed on white-emitting OLEDs. The HC slightly appears to impact the optical properties. The luminance does not change but a slight reduction of the emission in green region is observed, leading to a decrease of the OLED efficiency. It is expected that thin-film packaging allows a dramatic increase of image contrast especially at high brightness levels over the glued glass-lid packaging by removing the internal reflections on the glass and in the glue layer.

Enhancement of the performances of the HC layer can be obtained by optimizing the balance between organic and inorganic parts of the sol-gel formulation and by controlling the structure of the hybrid. The wear resistance of the HC appears to be sufficient for the dicing, cleaning and also the handling of the silicon substrates. The HC shows improved flexibility and resilience compared to pure inorganic layers, leading to a less brittle coating (Fig. 1).

Table 1 Mechanical properties of the hybrid thin-film.

<table>
<thead>
<tr>
<th>Property</th>
<th>PMMA 4-40 µm</th>
<th>Hybrid HC 3.5 µm</th>
<th>SiO₂ 1 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardness (GPa)</td>
<td>0.13 [7]</td>
<td>0.19</td>
<td>0.34</td>
</tr>
<tr>
<td>Young Modulus (GPa)</td>
<td>2.75 [7]</td>
<td>4.5</td>
<td>6</td>
</tr>
<tr>
<td>Abrasion ISO9211-0104</td>
<td>19 %</td>
<td>6 %</td>
<td>0 %</td>
</tr>
</tbody>
</table>

The fillers contained in the hybrid enhance the gas barrier properties of polymer matrices by increasing the diffusion pathway. The intrinsic properties of the composite cannot reach the requirement for OLED encapsulation but can be combined with a single alumina layer by Atomic Layer Deposition and exhibit high-barrier properties [2]. Accelerated aging tests were performed: no swelling or delamination were observed on the HC layer due to thermal choc or moisture ingress over the 300 hours of aging. In ambient conditions, regardless of the initial luminance, the samples exhibit systematically similar behaviors for as for standard OLED encapsulation.

Table 2 Picture of white emitting OLEDs before and after the storage test (60°C, 90%HR).

Perspectives
Thin-film alternatives to the glass lid are developed and promote environmental as well as mechanical resistance. These packaging scenarios also opens up the possibilities for the use of flexible or conformable substrate.

Acknowledgment
This study is founded by the French Defense Procurement Agency (DGA).

RELATED PUBLICATIONS:
[1] M. Provost, A. Suhm, T. Maindron, K. Raulin, V. Gaud, UV-curable Thin-Film Packaging for OLED-based Microdisplays, SID Symp. Dig. Tech 2018
OLED ON CMOS: WHAT ABOUT THINNING AND CURVING?

AUTHORS:
T. Maindron, B. Chambion, A. Vandeneynde, S. Gétin, M. Provost, A. Suhm, P. Peray, M. Zussy, J. Dechamp (DTSi)

ABSTRACT:
In this work, we use our technical background of CMOS thinning (historically developed for Through Silicon Via technology) to realize curved OLED-based microdisplays. This feature can allow significant innovation on the system/application because it will help to redesign simpler and lighter optical engine systems.

Context and Challenges
For today’s near-to-eye technologies, CMOS microdisplay-based systems like glasses or goggles will have to be performant in term of resolution, brightness, contrast but primarily also in term of reduced footprints to look like standard view glasses. Recently advancement fabrication techniques have been developed to provide curved focal plane arrays for CMOS-based image sensors [1] and K. Itohana et al., Symposium on VLSI Technology (2014), B. Guenter et al., Optic Express 25 (2017), 13010. In this work we propose to apply such techniques to OLED-integrated microdisplays in such a way that optical engine footprints can be reduced, in the meantime improving the field-of-view of the system as well as the image quality. In this miniaturization context, the packaging strategy becomes crucial and the main issues (OLED fragileness management, stress management, thermal management and thermo-mechanical features) will have to be considered.

Main Results
First studies have been conducted onto testing vehicles (no CMOS). Two scenarios have been explored for thinning of the OLED chips: Chip Level Thinning (CLT) as well as Wafer Level Thinning (WLT), with OLED layers deposited before thinning in all cases. The OLED has been protected from thinning process using a dedicated hard coat layer, made from a sol-gel material (provided by Polyrise Company, Bordeaux). Both scenarios can be implemented with great success.

Figure 1: generic concepts of curved displays, following display scale [image source: Samsung, LG and Emagin]
Figure 1 represents a general concept of curved displays, showing that the technological need for such displays increases as display size decreases. In the end, curving microdisplays turn out to be a key feature for microdisplay-based systems while it is purely marketing appeal for large displays such as TV displays.

Figure 2: IVL characteristics of a white OLED (a) made onto a thinned Si substrate following WLT process (circles) and (b) following CLT process (squares) with 45 mm radius of curvature; inset: EL spectrum of the white OLED at 2000 cd/m²
The IVL characteristics of a reference OLED made onto a thick Si substrate are identical (not shown here). It is therefore possible to thin down the OLED substrate without altering the fragile OLED architecture, by proper use of a dedicated hard coat layer deposited onto the thin-film encapsulation. The top-emitting white OLED architectures used in this study presents high efficiency (10 cd/A at 5000 cd/m²) and high luminance (10 kcd/m²) in the region < 5V.

Figure 3: 0.38” OLED-based microdisplays from MicroOLED company, curved with 45 mm radius.
Perspectives
The development of a thinning and curving process onto active matrix (CMOS) OLED is ongoing for innovative 1” diagonal chips developed in the framework of the LOMID project (this work is H2020-funded) [2].

RELATED PUBLICATIONS:
TRANSMISSIVE LIQUID CRYSTAL SPATIAL LIGHT MODULATOR (SLM) FOR LIGHT MODULATION USING IN-PLANE SWITCHING (IPS) TECHNOLOGY

AUTHORS:
C. Abélard, B. Racine, U. Rossini, F. Templier

ABSTRACT:
An investigation of IPS-SLM architecture with small pixel pitch (around 5 µm) for phase modulation and amplitude modulation application was achieved. The studies were focused on the SLM architecture in order to optimize the performances for specific applications. Most of the transmissive SLM configurations use nematic liquid crystals (LC). We studied in this work the SLM in IPS technology which is well adapted to address pixel at the micrometric scale (around 5 µm). SLM can modulate either phase or amplitude of the light, depending of the application. In this work, we studied both, the phase modulation studies resulted from a Vertically Aligned (VA) LC SLM architecture with IPS addressing allowing 2π phase shift and the amplitude modulation studies resulted from an architecture using cross-patterned electrodes with Homogeneously Aligned (HA) LC allowing a very short response time (around 2 ms).

Context and Challenges
The current SLMs are either reflective or transmissive with nematic LC and use different types of liquid crystal alignment like Parallel Aligned (PAL), Twisted Nematic (TN), and Vertical Aligned (VA). However, today no commercial SLM uses IPS configuration while it allows a better contrast and a viewing angle than other technology. Moreover, driving voltage and response time need to be improved to address specific applications. Due to the reduction of the pixel size, SLM can be more compact and it became usable in specific systems like Head Mounted Display (HMD) or foveated optical systems. An improvement of response time with CMOS compatible voltages could also allow an application for sequential color display application.

Main Results
Several IPS technologies have been investigated for pure phase modulation. It appears that the IPS-VA gives a more homogeneous and higher phase shift than IPS-TN or IPS-HA. However, the phase modulation depends on many parameters such as: birefringence, cell gap, wavelength and electrodes voltage. Moreover, in the IPS configuration, electrodes size and gap are also critical for driving voltage values. In this work we investigated an optimal pixel configuration by changing the geometrical, electro-optical and elastic parameters by simulation using LCDMaster software.

The pixel architecture (figure 1) which has been patented [1] giving the best result is obtained for a cell gap (d) and pixel size of 5 µm, a pitch between two electrodes (P) of 2.5 µm and an electrode width of 0.8 µm. They are elevated of d/3 by an insulator (ds) and we also add a 0.5 µm insulator below the upper substrate (di).

With this architecture, a phase shift of 2π can be reached with a low driving voltage (below 3V).

For amplitude modulation, a IPS-HA configuration (figure 2) was studied as well as the configuration with the cross-patterned electrodes, also patented [2].

Perspectives
The studies on amplitude modulation proved the interest of IPS in particular for small pixel pitch. This kind of SLM could be integrated in a sequential color display. These display require a very short response time and could benefit of all the other advantages of IPS technology.

The studies on phase modulation configuration has been pushed further by simulating a foveated optical system integrating the newly simulated SLM. Encouraging results have been found in some specific configurations of optical systems. These studies will be implemented on prototype to confirm the simulations.

RELATED PUBLICATIONS:
• Robust automated design/optimization of nanophotonic components
• HgCdTe strain-gap topological insulators
Context and Challenges

Designers of photonic devices increasingly rely on numerical optimization. However, the actually fabricated object may differ significantly from the ideal design. Accounting for manufacturing errors, together with variations of the environmental conditions, is a key issue on the path towards robust industrial deployment.

Main Results

The design of broadband devices is a valid heuristic to search for photonic components which are tolerant to fabrication error. This approach has been previously demonstrated during the design of a silicon-on-insulator adiabatic coupler used as a power splitter [1]. The robustness to fabrication errors has been confirmed experimentally. Since then, a new metamodel based multi-objective optimization method, adapted to the worst-case scenario, has been devised and implemented [2, 3]. The procedure is based on the coupling of genetic and gradient-based methods. First, the NSGA-II genetic multi-objective optimization algorithm is applied on the metamodel prediction of each objective. At each generation, the population is selected, crossed-over and mutated (classical genetic algorithm operations). A clustering procedure then selects a given number of points among the final solutions. The selected points are used as starting points of the multiple gradient descent algorithm (MGDA). The points obtained from MGDA are filtered, based on their prediction error, and then evaluated and added to the training dataset. This sequence is iterated until convergence. A nicely spread Pareto front, which represents the set of optimal solutions among the training dataset, is thus obtained. As can be seen on Fig. 1 (right), a wideband power splitting ratio is attained.

An analogous procedure was adapted to the context of topology optimization, where non-parametric shapes, such as the one presented on Fig. 2 (left), are generated. The wavelength duplexer obtained using a MGDA-like algorithm, presents a larger bandwidth than the non-robust one (Fig. 2, resp. right and center).

An approach, which directly deals with manufacturing errors has also been implemented [4]. This algorithm considers three shapes: the nominal one, as well as the same dilated and eroded by a certain distance. Since the three shapes do not necessarily share the same topology, it is necessary to limit the dilations and erosions up to the skeleton of the nominal shape. A multi-objective optimization is performed, leading, again in the case of a wavelength duplexer, to a shape that is robust to fabrication errors (Fig. 3).

Perspectives

A first set of shape-optimized components will shortly be fabricated by e-beam lithography on SOI substrate. The performances of individual devices, as well as statistics on full wafer variability, will be assessed to confirm the robustness of the design and the validity of our approach.

RELATED PUBLICATIONS:

MBE GROWTH OF HgZnTe/CdTe: TOWARDS ENHANCED STRAIN-GAP TOPOLOGICAL INSULATORS

AUTHORS:
J. Papin, A. Chorier, P. Noël (INAC-SPINTEC), L. Vila (INAC-SPINTEC), J.-P. Attané (INAC-SPINTEC), T. Meunier (I.NEEL-CNRS), P. Ballet

ABSTRACT:
Tensile-strained HgZnTe layers have grown on CdTe(100) and represent topological insulator structures with an inverted band structure inheriting from HgTe for zinc fraction lower than about 15% and with a larger strain-induced bandgap due to the increase in lattice mismatch with zinc concentration. MBE growth and material characterization are presented showing excellent crystal quality and surface morphology in the topological range. Low temperature transport of Hall bar devices exhibit electronic mobility close to 100000 cm^2/V.s and clear quantum Hall signatures.

SCIENTIFIC COLLABORATIONS: CEA-INAC-SPINTEC, CNRS - I. NEEL

Context and Challenges

Topological Insulators (TI) are a new class of materials attracting great interest both theoretically and experimentally thanks to their unique electronic and spin properties that arise at their interfaces. With an inverted band structure, the semi-metal HgTe has been identified as a strong TI assuming the opening of a bulk gap. In the general case of 3D-TI, the growth of tensile strained HgTe/CdTe structures naturally opens a gap in the order of 20meV and convincing signatures of topological transport have been demonstrated in such system (C Brüne et al., Phys. Rev. Lett. 106, 126803 (2011), and [1-2]). However and despite the predicted robustness of topological states, it is generally found that such small bandgap TIs produce unstable results with a clear trend of mixing surface and bulk electronic properties. While the origin is still unclear, crystal defects or material fluctuation such as interface roughness, intermixing or bulk residual doping level represent plausible causes. Increasing the bulk strain obviously represents a way to reduce the sensitivity of surface electronic states to any material fluctuation in addition to possibly decouple the surface states from the 18 bulk heavy hole band.

Main Results

Here we present the MBE growth of HgZnTe layers on CdTe(100) substrates. Introducing zinc in amounts lower than 15% would considerably increase the tensile strain in the growing layer while preserving the inverted band ordering. While the critical thickness for plastic relaxation is in the order of 150nm for HgTe/CdTe, it is expected to be significantly reduced when increasing strain i.e. when increasing the zinc fraction. 50nm-thick HgZnTe layers have been grown with different zinc fraction ranging from pure HgTe to about 25% of zinc allowing to continuously follow the increase in tensile strain while checking on bulk or surface relaxation using high resolution X-ray diffraction (HRXRD), see figure 1, and atomic force microscopy. Obviously, increasing the zinc fraction from pure HgTe (black) to 25% (purple) causes a systematic shift to larger Bragg angles witnessing the reduction of the out-of-plane lattice parameter of the tensile-strained layer. The layer quality is found to be excellent for zinc content as high as 10-15% resulting in estimated strain bandgap in the order of 70-80meV. For higher zinc fraction, some degradation in the X-rays together with the appearance of dislocation lines in the AFM images suggest partial plastic relaxation.

Perspectives

Additional work is needed and currently underway to quantitatively determine the exact gain in strain-gap which is expected to be in the order of 70-80meV compared to the 20meV of current HgTe topological structures. If confirmed, this would lead to a new topological material with enhanced bandgap and as a result enhanced robustness and applicability.

RELATED PUBLICATIONS:
09 PhDs AWARDED IN 2017

- Bruno DELACOURT
- Olivier DUBRAY
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- Jérôme MEILHAN
- Yolande MURAT
- Dinh Chuong NGUYEN
- Aymeric TUAZ
BRUNO DELACOURT
EXTRINSIC DOPING OF CdHgTe APPLIED TO INFRARED PHOTODIODES

Infrared photodiodes, which are based on narrow gap semiconductors, permit collection of carriers generated by photons impact but also by thermal agitation. This agitation create a parasitic dark current deteriorating device performance. In order to minimize this dark current, the key parameter to maximize is the minority carrier lifetime. In high operating temperature (HOT) context, it open the possibility to increase the operating temperature of photonic infrared detectors. For the mid-wave infrared window, the goal is to work at 150−180 K instead of 80−120 K currently. This would allow significant progress in terms of energy consumption, power and thus autonomy and reliability of the systems. The objective of this thesis is to experimentally determine the theoretical limits of the minority carrier lifetime in HgCdTe and in a III-V semiconductor. For this, a photoluminescence decay measurement bench as well as a data extraction method making possible to discriminate the recombination mechanisms from the evolution of the signal as a function of the level of carrier injection in the sample were developed. In parallel, a set of characterizations was carried out to assist the development of technologies addressing the HOT context.

OLIVIER DUBRAY
DESIGN AND CHARACTERIZATION OF TRANSMITTER ARCHITECTURES USING SILICON RING RESONATOR MODULATORS FOR HIGH BIT RATE COMMUNICATIONS

Over the past decade, with the diversification of connected devices (PCs, Tablets, TVs and Smartphones), the Internet ecosystem has drastically extended. Today, 80 % of the IP world traffic runs inside the data centers. To address such scaling issues as bandwidth density, energy consumption and cost of the interconnects inside the data centers, the development of new optical transmitters is critical. The purpose of this thesis is to propose and evaluate transmitter architectures built from Silicon Photonics for next 400 Gbit/s data rate standard over up to 2 kilometer-links. The selected optical modulator is the silicon ring resonator modulator which has substantial benefits: low footprint, low energy consumption and enables dense multiplexing.
Recently, Silicon Photonics has emerged as a solution for the mass manufacturing of optical transceivers addressing datacenter’s needs in terms of increasing data-rate and reduced cost. Several Silicon-Photonics platforms have been demonstrated using standard Si technology. While these platforms differ in many regards, they all lack a solution for a monolithically integrated light source. To solve this problem, the most commonly proposed approach consists in bonding an InP-stack onto a Si-wafer in order to fabricate a Hybrid III-V/Si laser. However, none of those demonstrations have been made with a standard CMOS-BEOL, preventing a proper electronic-photonic integration. To solve the topographical problem induced by the additional layers, a new integration scheme, called Back-Side, has been developed and is presented in this document. We have proved that, under specific conditions, the grating coupler has the same measured performances in Back-Side and in Front-Side. The implemented laser is based on a hybrid DBR (Distributed Bragg Reflector) III-V/Si cavity. In order to increase the mode confinement in the MQWS (Multi Quantum Wells) and hence ensure a high optical gain, the optical mode is gradually transferred between the III-V waveguide and the silicon waveguide of the hybrid laser by adiabatic tapers, patterned on both sides of the gain zone, to finally be reflected by the mirrors DBR in the silicon. Finally, its manufacturing process is explained before its opto-electronic characterizations are presented.

Nowadays, microelectronic chips and sensors are not simply electronic circuits anymore. They are able to convey both electric and optical signal. As shown by the so-called photonic chips used to transmit data at high speed rate. However, this technology only exploits a very small part of the light spectrum, namely in the near infrared. Exploitation of the whole mid-infrared domain (λ=2-20 µm) would allow to develop new integrated sensors using molecules specific spectral fingerprints in this part of the electromagnetic spectrum. This thesis deals with the development of integrated optical circuits on silicon capable of handling these wavelengths and compatible with 200 mm clean room fabrication processes. The technology developed in this work, is based on Si0.6Ge0.4 channel square waveguides in order to obtain compact and low loss optical circuits. First of all, the design of optical functions required to build circuits is presented. Then, these functions are assembled into circuits which are manufactured and characterized in order to assess performances of the developed technology. Two circuits have been produced: one with standard processes and one with damascene processes. The first one has the advantage of using known processes, whereas the second one allows to make waveguides for different wavelengths on a single chip. These two circuits have been characterized in order to conduct a comparative study between the two fabrication processes. Finally, in order to mature the technology, an in-depth...
AINUR KOSHKINBAYEVA
NEW PHOTONIC ARCHITECTURES FOR MID-INFRARED GAS SENSORS INTEGRATED ON SILICON

This work focuses on optical multiplexers for mid-IR broadband source in gas sensing application. The design of multiplexer configurations based on two types of diffraction gratings is discussed. Owing to utility of Gaussian approximation of the field and Fourier Optics, we developed a semi-analytical tool allowing to evaluate the responses of array waveguide grating (AWG) and planar concave grating (PCG). This approach also opened the way to implement numerical phase error analysis by introducing normal distribution of errors and to study the correlation between standard deviation of phase errors and the level of crosstalk. FTIR spectroscopy measurement results of 5.65 µm AWGs, built with SiGe graded index core encapsulated in a thick Si cladding on standard silicon substrate, are compared with the theoretical expectations. We have also performed evaluation of AWG response at elevated temperatures, in the range between 20 °C and 41°C. The spectral shift showed linear dependence with the temperature, which is in a good agreement with simulation predictions.

JEROME MEILHAN
DESIGN, MODELING AND CHARACTERIZATION OF MICROBOLOMETRIC DETECTORS FOR SUB-THZ IMAGING APPLICATIONS

This PhD dissertation presents the analysis, characterization and optimization of the performances of micro-bolometric imagers in the sub-THz frequency range. This non ionizing span of the electromagnetic spectrum is currently a booming field of research. Development of high-performance and room temperature imagers opens the path towards many applications. One of such promising application is non-destructive screening enabled by the good penetrating power of these radiations through many materials, especially at frequencies lower than 1 THz. Through a radiometric analysis of an active imaging system, we assess the required performances of an imager suited for this application. In this context, we have analyzed the electrothermal performances of the cutting-edge THz imagers based on micro-bolometer developed at CEA-Leti. Thanks to a detailed model of the bolometer bridge of these detection arrays, we have brought into focus the limiting factors of the current devices. Technological improvement have been considered such as the integration of a new thermometer material. The performance improvements brought by these optimizations have been quantified thanks to the modeling tool we have developed and it is showed that sensitivity close to the pW range can be reached on these imagers. An intensive experimental work have also been carried out in order to assess the sub-THz electromagnetic performances of the micro-bolometer.
One objective of the microbolometers industry roadmap is to scale down the sensor surface – the pixel pitch – in order to increase the number of imagers fabricated on a silicon wafer. The scaling has been recently slowed down, mostly because of microbolometers self-heating issue and 1/f noise which are inherent to the resistive transduction.

Our work has focused on a new type of sensor at 12µm pixel pitch, which theoretically gets rid of self-heating and 1/f noise. In our approach, an absorbing plate is excited at its mechanical resonance through two tiny torsion arms using an actuation electrode placed 2µm underneath. Pixel motion is also transduced electrostatically. Since micromechanical resonators feature very low frequency noise, we believe that an uncooled infrared sensor based on the monitoring of its resonance frequency (which changes with temperature through the TCF) should be extremely sensitive.

We present different models (linear and nonlinear) for the pixel mechanical behavior and compare them to experimental characterization of resonators which were fabricated in dense arrays. We measure the frequency stability of our sensors along with their sensitivity to infrared flux. The best devices show a resolution of 30pW/Hz, with a response time lower than one millisecond. The scene resolution (NETD) is 2K for an integration time compatible with imaging frame rate. These performances overtake results previously published on this topic with such reduced pixel pitch.

Light-emitting diodes (LEDs) used in solid lighting systems are made from GaN and its alloys. Although commercial LEDs are mainly developed on sapphire substrate, manufacturers and research laboratories are also interested in silicon substrate, which is cheaper and available in larger diameters. However, its usage raises two issues: the presence of a high dislocation density in epitaxial layers and their tensile stress leading to the formation of cracks. In order to avoid them, solutions exist but require long and complex growth processes resulting in an increase in production costs. The alternative proposed in this thesis is focused on the selective area growth (SAG) of GaN pseudosubstrates on silicon by metalorganic vapour phase epitaxy (MOVPE). Indeed, the SAG through a dielectric mask should make it possible to obtain a good crystalline material displaying a limited stress (avoiding coalescence) while reducing epitaxy duration. Our work focused on the analysis of the influence of growth parameters (growth conditions, mask design, substrate polarity) in order to understand the involved mechanisms and to control the effect of each of them on the material morphology. The growth of hexagonal [0001] GaN pseudosubstrates on Si (100) was demonstrated by using a textured N-polar AlN layer. Optical and structural characterisations displayed a stress relaxation as well as a good crystalline quality of these structures’ surface material. The growth on top of those of
OLED (Organic Light-Emitting Diode) technology has been exploited on an industrial scale for several years, principally in smartphones, TV displays, and similar devices. However, current fabrication processes, such as thermal evaporation under high vacuum, are expensive and cannot be used for low-cost applications (signage, lighting, etc.). This work aims to develop high-performance, stable, low-cost OLEDs. Fabrication by solution processing was chosen to reduce the processing costs in any future commercialization of the work, while the inverted architecture was used to optimize device stability. In this work, ethoxylated polyethylenimine (PEIE) was used to reduce the work function of the transparent cathode. It was shown that higher performances could be obtained with inverted OLEDs compared to direct devices incorporating the same emissive polymer (Super Yellow). Furthermore, it was demonstrated that a binary blend, (PEIE and a hole blocking material) could be deposited in a single step without reducing the OLED device’s performance – greatly simplifying the fabrication process. A TOF-SIMS (Time of Flight-Secondary Ion Mass Spectrometry) study was conducted which demonstrated a vertical phase segregation of the binary blend. Finally, the indium tin oxide (ITO) electrode, which represents at least 25% of the fabrication cost, was successfully replaced with a tin oxide (SnO2) layer, deposited by ALD (Atomic Layer Deposition).

This PhD. works, which was carried out inside CEA-LETI, aims to dissociate the various mechanisms occurring inside a GaN-based LED employing numerical simulation and experimental characterization. In the chapters 1 and 2, various mechanisms occurring inside a diode/LED are theoretically described. In chapter 3, through numerical simulation, the dominant mechanisms as well as their locations in a VTF ("vertical thin film") LED structure are determined for different voltage ranges. A parametric study follows to assess the interactions between the mechanisms. In chapter 4, the simulations are carried out with an additional field-dependent model for charge carrier mobility. With this model enabled, the simulated LED-electrical-and-optical characteristics approximate the real LED characteristics. Carrier-velocity characterization on p-type GaN, using a specific sample structure and the resistivity method, is also shown in chapter 4. It can be inferred from the results that under strong electric-fields, the carrier velocity might saturate, or the carrier mobility might decrease. These results strengthen the hypothesis used for the simulations in this chapter 4. The simulations introduced in the chapters 3 and 4 allow the proposition of an equivalent circuit for a GaN-based LED by dissociating the different mechanisms and retaining the dominant ones. This equivalent circuit could help, for instance, identify the different regimes in a real-LED electrical characteristics in order to improve the LED’s
This thesis concerns the field of HgCdTe infrared detectors for night vision, for which the Infrared Laboratory of CEA -Leti - Minatec is a world leader. The student will participate in the full development of a dual-band detector that simultaneously detects several parts of the infrared spectrum. The active area is a superposition of nanometric layers doped during growth by molecular beam epitaxy, which is then subdivided into photodiode arrays of micrometer size by etching before passivation. Very specific and extremely sensitive investigation techniques, using synchrotron radiation and ion beams will be used to study these structures and determine the local properties of processed materials. In particular, the immediate environment of dopants, local strain generated by etching and atomic displacements induced by the manufacturing process will be determined.
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OPTICS AND PHOTONICS

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