

3D INTEGRATION

CUSTOM YOUR IC DESIGN & ARCHITECTURE WITH AN EASY TO PLAY 3D KIT

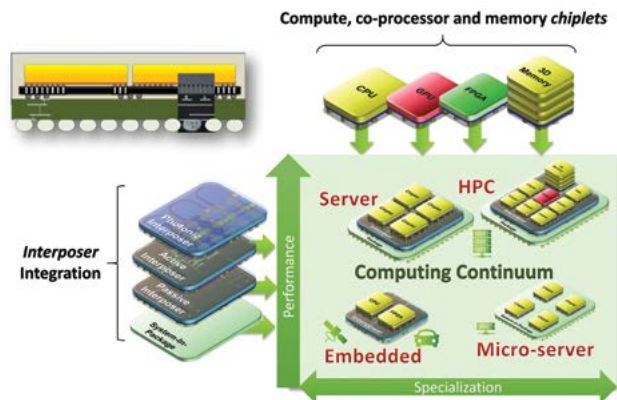
+ WHAT IS 3D INTEGRATION?

Your solution to design complex and heterogeneous SoCs. 3D Integration offers a new concept of architecture with its associated IPs, it enables you to:

- Split your design in chiplets with Leti's **3D Kit**, an advanced concept relying on 3D stacking. It provides the 3D enablement IPs and methodology to deliver best-in-class performances. This 3D Kit is available in 2.5D and 3D versions.
- Simplify the design of complex SoCs thanks to **ANoC**, an asynchronous network-on-chip. ANOCs are compatible with traditional bus protocols.
- Communicate between heterogeneous SoCs with high bandwidth and low latency thanks to **RDMA**. It can be used on a motherboard or with 3D stacked chiplets.

+ APPLICATIONS

With billions of transistors integrated on SoCs, design is more and more complex and must be approached differently. Leti's ANoCs, 3D Kit and RDMA provide you with solutions for your high-end SoC. They address various application segments, such as microservers, servers and HPC.



+ WHAT'S NEW?

The Leti 3D offer is based on the strong association of 3D technology, design and architecture. We have developed a set of communication IPs and associated design methodology, validated on complex demonstrators.

3D KIT

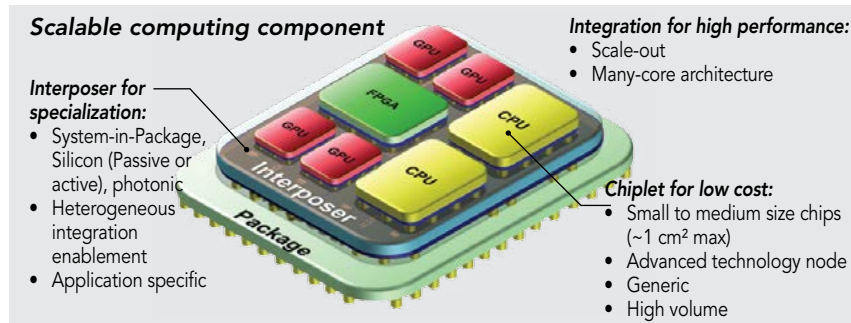
- Target any combination of homogeneous/heterogeneous multi-core and technologies
- No global clock tree
- Ultra-low-power 3D communications (demonstrated 0.32 pJ/bit transmission @ ISSCC'16)
- DFT and considering electrostatic discharge protection
- Full 3D design methodology, including thermal analysis and 3D physical sign-off

RDMA

RDMA technology is developed by Leti over the interposer to provide efficient communication between SoC devices. This implementation of RDMA has one important specificity: instead of relying on expansive and power hungry legacy host channel adapters like 10GbE or Infiniband, it communicates on top of lightweight chip-to-chip NoC interface, further reducing latency and data transfer power consumption.

ANOC

- Power : average gain of 60% thanks to event-driven and clockless logic (no global clock tree power consumption)
- Throughput: better throughput in typical case
- Latency: gain of 30% thanks to reduced number of resynchronization cycles
- Area: overhead is about 10% on a 64-bit-wide data path
- Variability: natural robustness to PVT variations thanks to delay insensitive design style
- Physical implementation:
 - No global clock tree allowing divide-and-conquer floor plan strategy
 - No long-wire impact helping interconnect timing closure



+ WHAT'S NEXT?

Next step is to demonstrate the value of an active interposer for partitioning an architecture embedding 96 MIPS cores and using a series of chiplets in FDSOI 28 nm co-integrated on a 65 nm CMOS mixed-signals active interposer. Our vision is extended through Leti's participation in several European projects in the field of computing. CEA is currently coordinator of the European ExaNoDe project (Horizon 2020 Framework Program) that investigates and develops building blocks for a highly integrated, high-performance, heterogeneous SoC aimed towards exascale computing. In a longer term approach Leti is developing a demonstrator for an optical NoC to interconnect microprocessors and memories integrated in a photonic interposer aiming ultra-high bandwidth communications.

Leti's potential contributions as an R&D provider in the field of computing can be tailored to the needs of our partners, whether their architectures are cost, latency or bandwidth driven.

Leti, technology research institute

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INTERESTED IN THIS TECHNOLOGY?

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