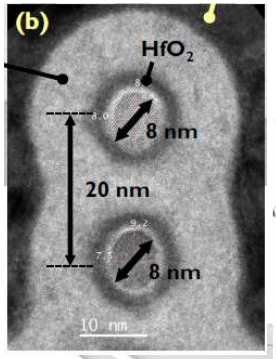
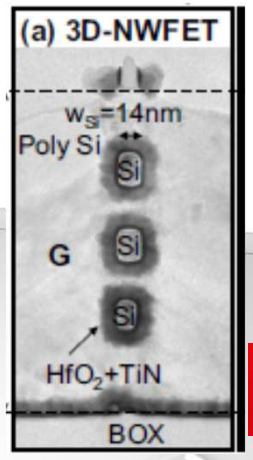
SCALING ROADMAP

SUPERAID 7

5nm

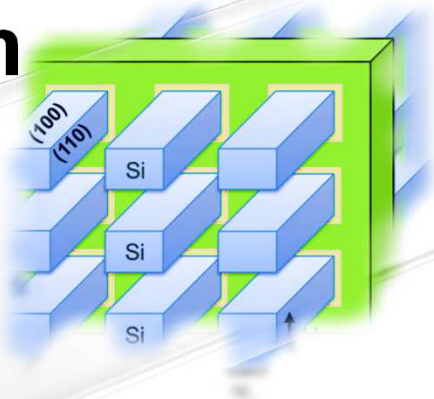


IMEC (VLSI 2016)



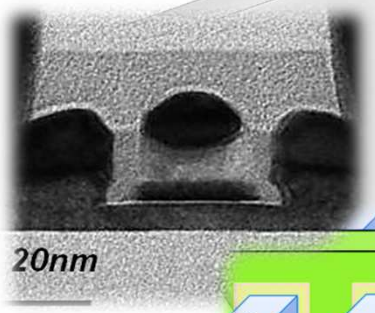
Leti (IEDM 2008)

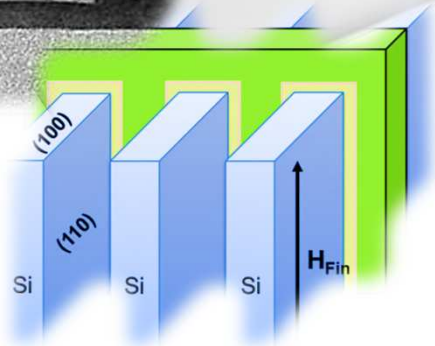
7nm



Stacked-NWs (nanosheets)

10nm



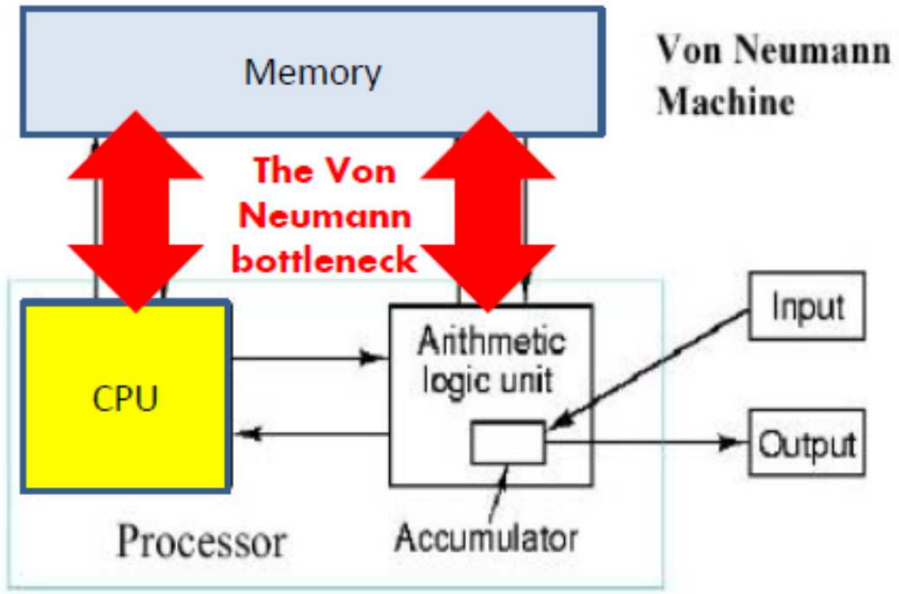


S. Barraud et al, session 17.6 Vertically Stacked-NanoWires MOSFETs in a Replacement Metal Gate Process with Inner Spacer and SiGe Source/Drain

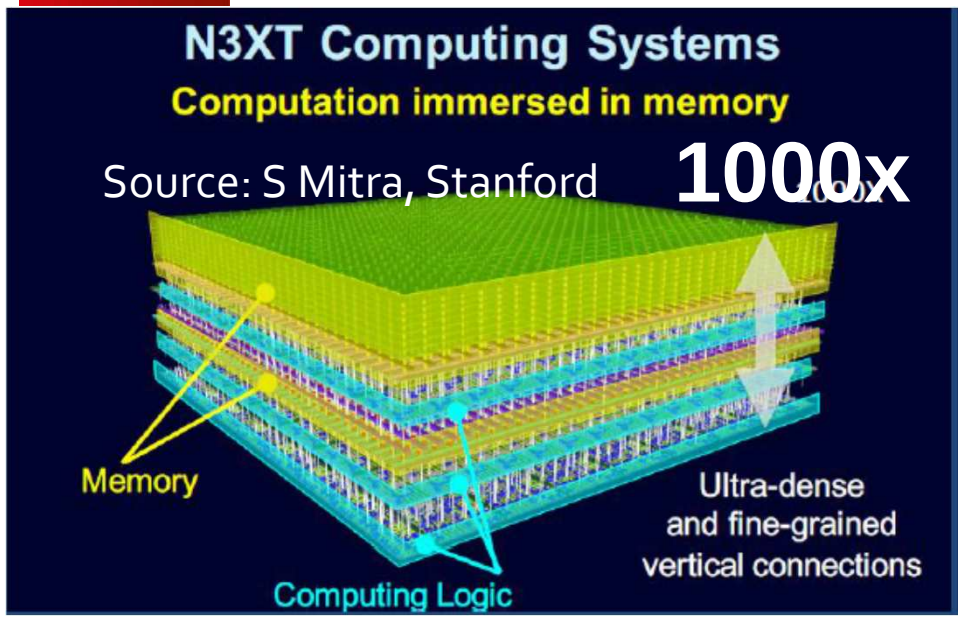
VON NEUMANN PROCESSOR

A Von Neumann processor can execute an arbitrary sequence of instructions on arbitrary data but the instructions and data must flow over a **limited capacity bus** connecting the processor and main memory.

Thus, **the processor cannot execute a program faster than it can fetch instructions and data from memory.**

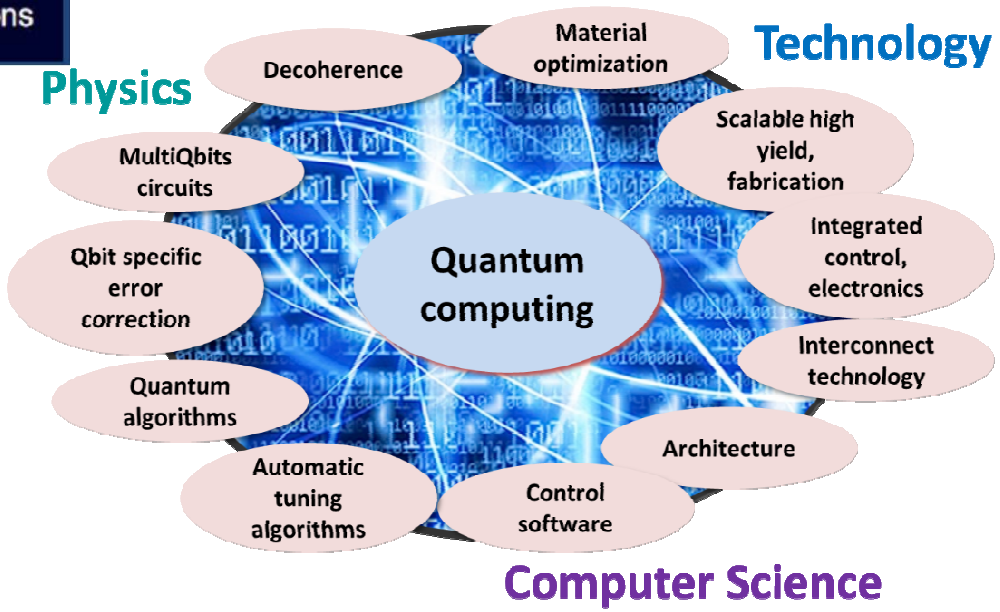


NEW COMPUTING PARADIGMS



Computation Immersed in Memory

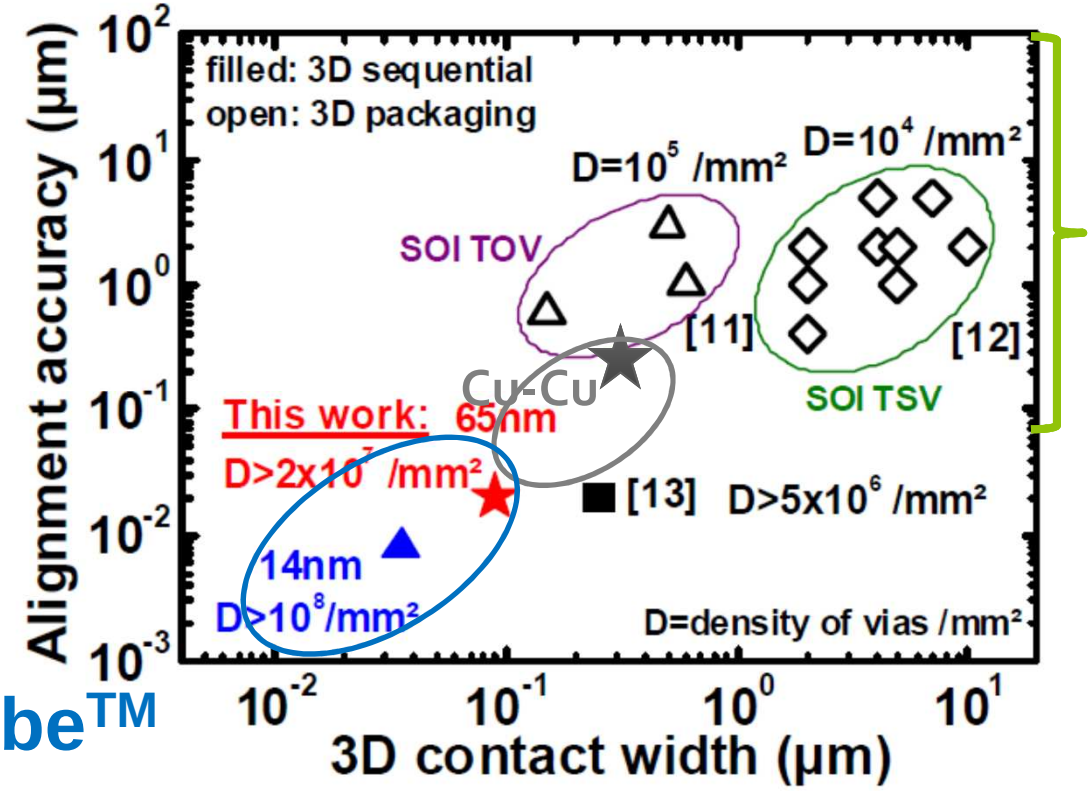
Massive parallelism
Quantum computing



WHICH DEVICES FOR NEW COMPUTING PARADIGMS?

Leti Devices Workshop | Maud Vinet | December 4th, 2016

HIGH DENSITY 3D TECHNOLOGIES



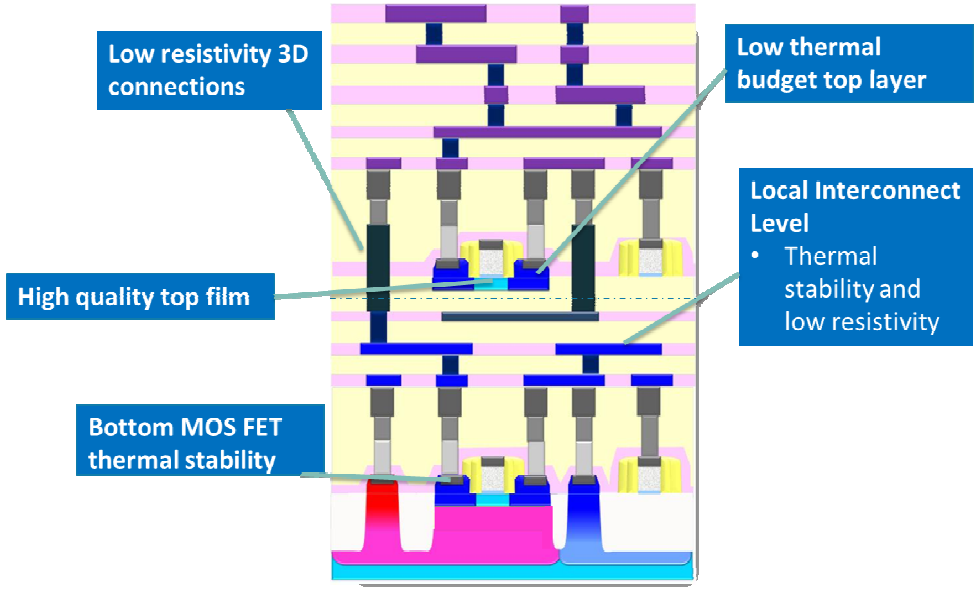
3D Technologies: Several Disruptive Technologies to Look Ahead
Dr Olivier Faynot

CoolCube™

Above 2x10⁷vias/mm² demonstrated with CoolCube™

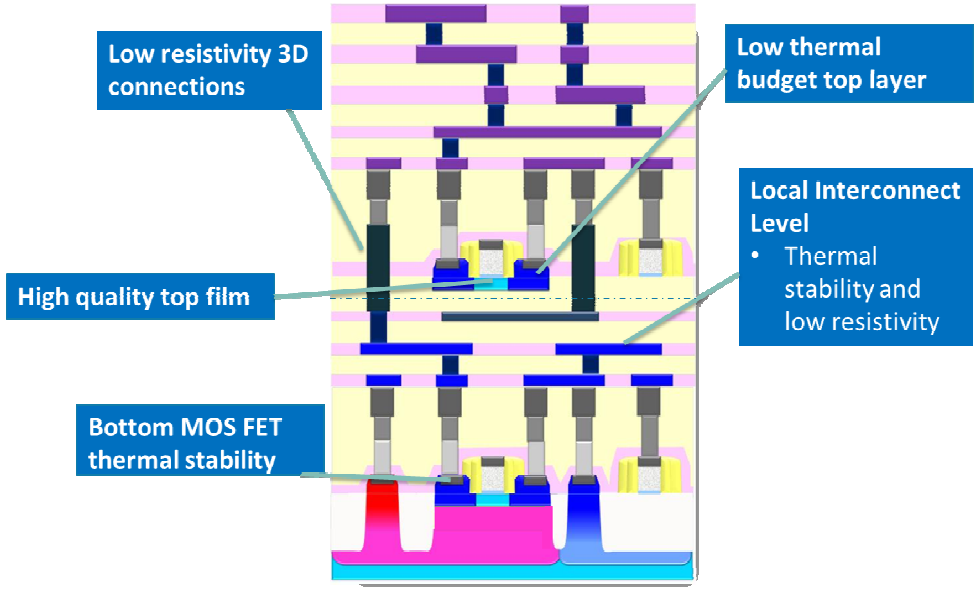
Reachable 3D via pitch @ 14nm = 80nm

CoolCube™



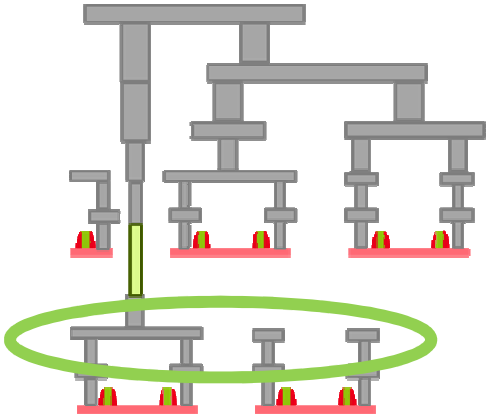
1. Top Junction Performance?
2. Inter Metal Interconnects?
3. Is It a Manufacturable Process?
4. Do You Really Benefit From the Lithographic Alignment?

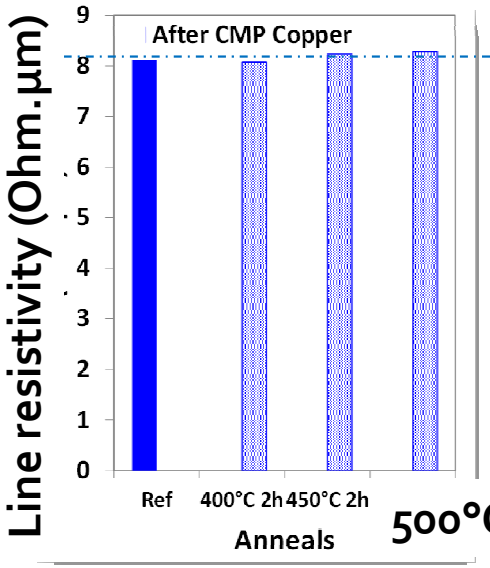
CoolCube™



1. Top Junction Performance?
   Same as bottom one (Pasini, VLSI 2015 and 2016)
2. Inter Metal Interconnects?
3. Is It a Manufacturable Process?
4. Do You Really Benefit from The Lithographic Alignment?

WHAT ABOUT INTER LAYERS INTERCONNECTS?

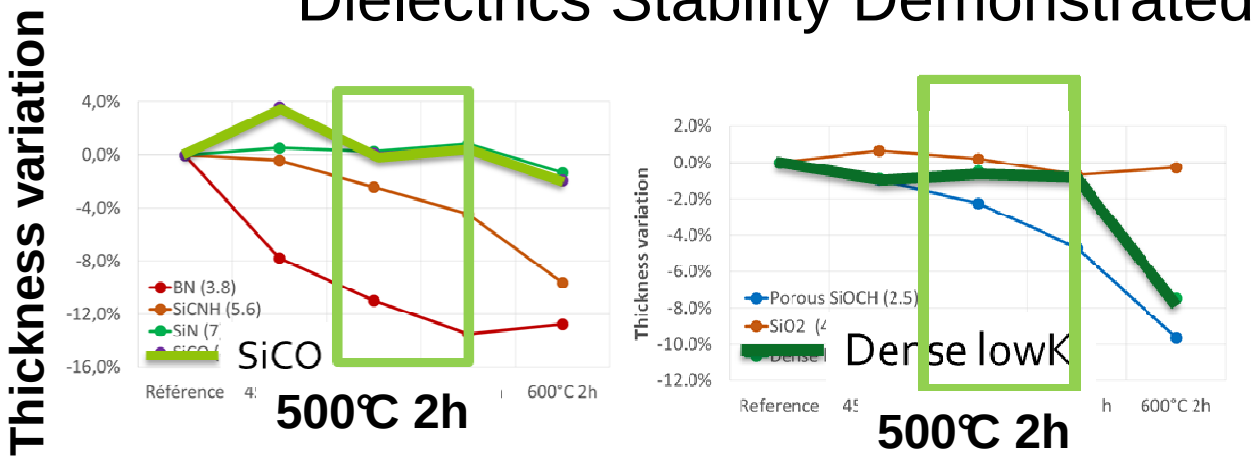




Copper lines **500℃** thermal stability proven

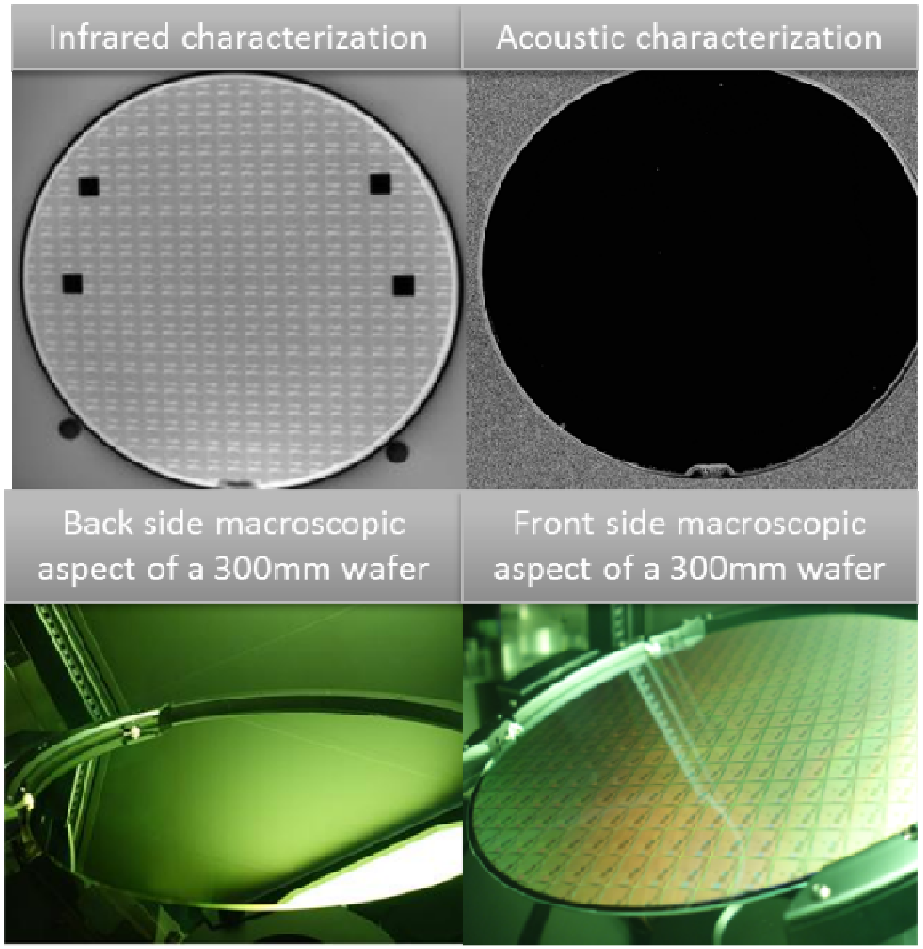
C Fenouillet, SSDM 2015

Dielectrics Stability Demonstrated



F Deprat, MAM 2016

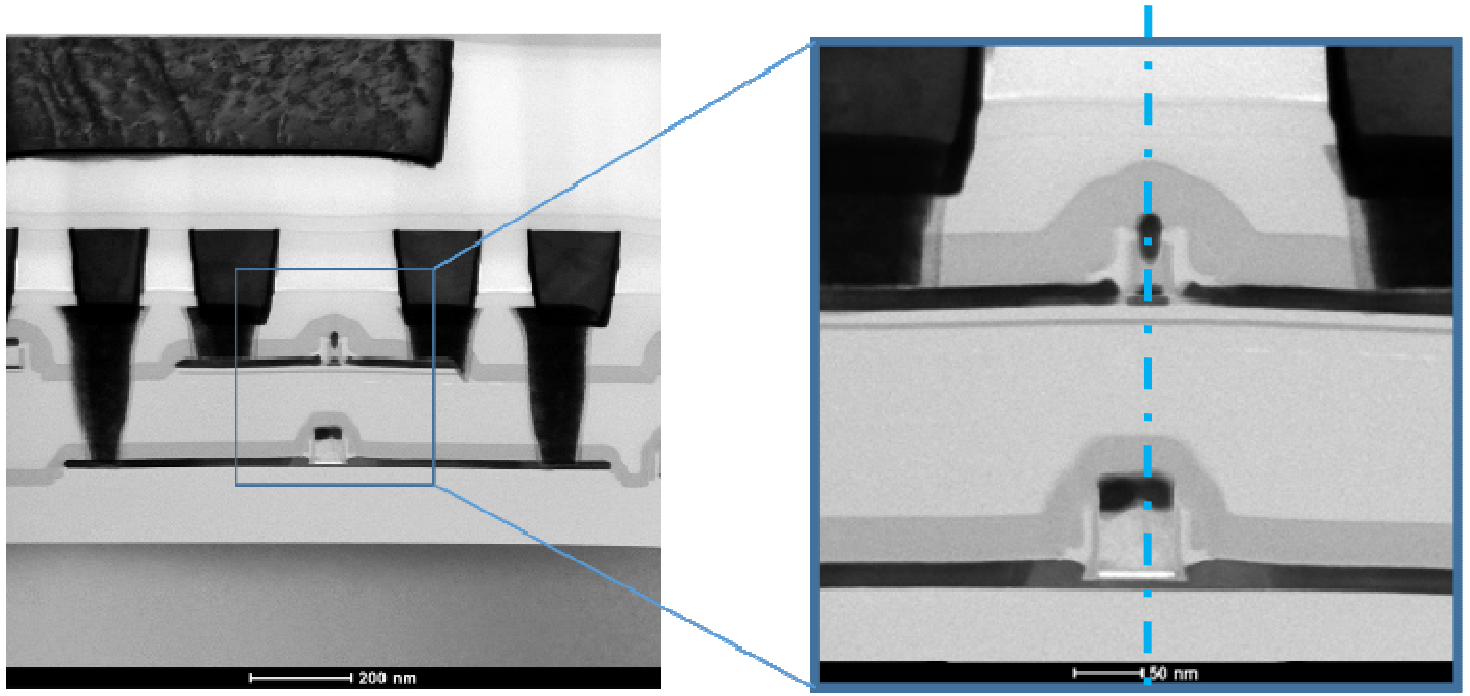
300mm WAFERS IN PRODUCTION FAB



No macroscopic bonding defects at 300mm wafer scale

L Brunet, VLSI 2016

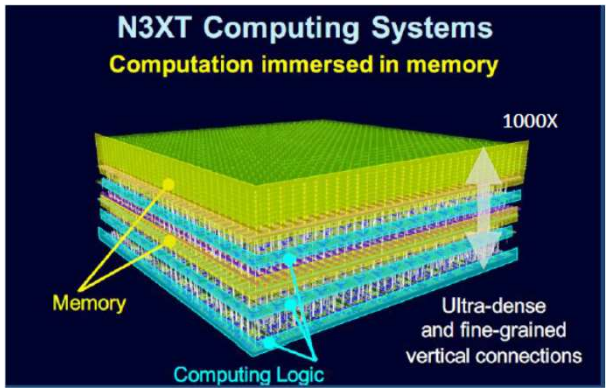
NANOMETRIC LITHOGRAPHY ALIGNMENT AT WAFER SCALE

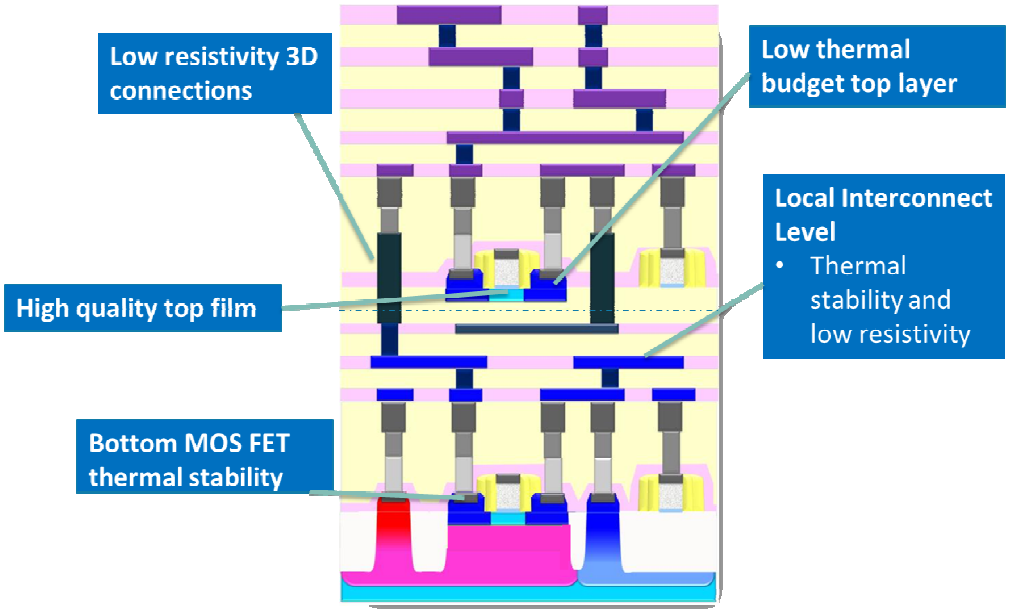


No Impact of Layer Deformation During Bonding and Thinning

L Brunet, VLSI 2016

CoolCube™



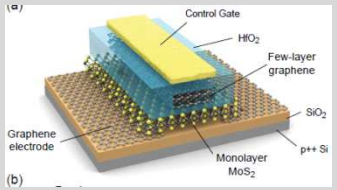


- ✓ Top Junction Performance
- ✓ Inter Metal Interconnects
- ✓ Manufacturable Process
- ✓ Lithographic Alignment

2D TMD (TRANSITION METAL DICHALCOGENIDES)

Opportunities for Logic and Non-Volatile Memory Co-Integration

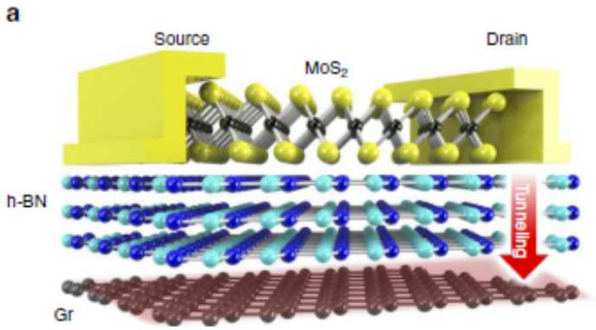
S. Bertolazzi
ACS nano 2013



Memory

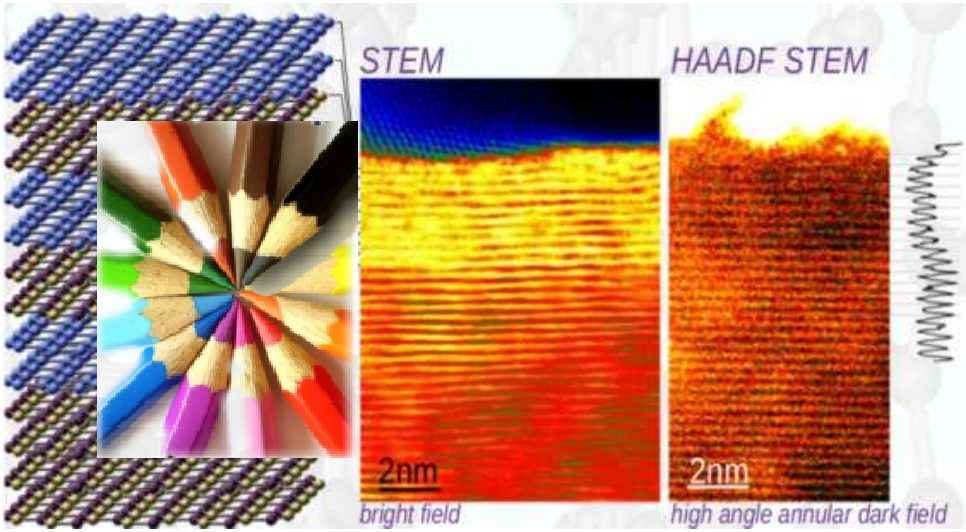
Spintronics

Spin Logic with Ferromagnetic Memories

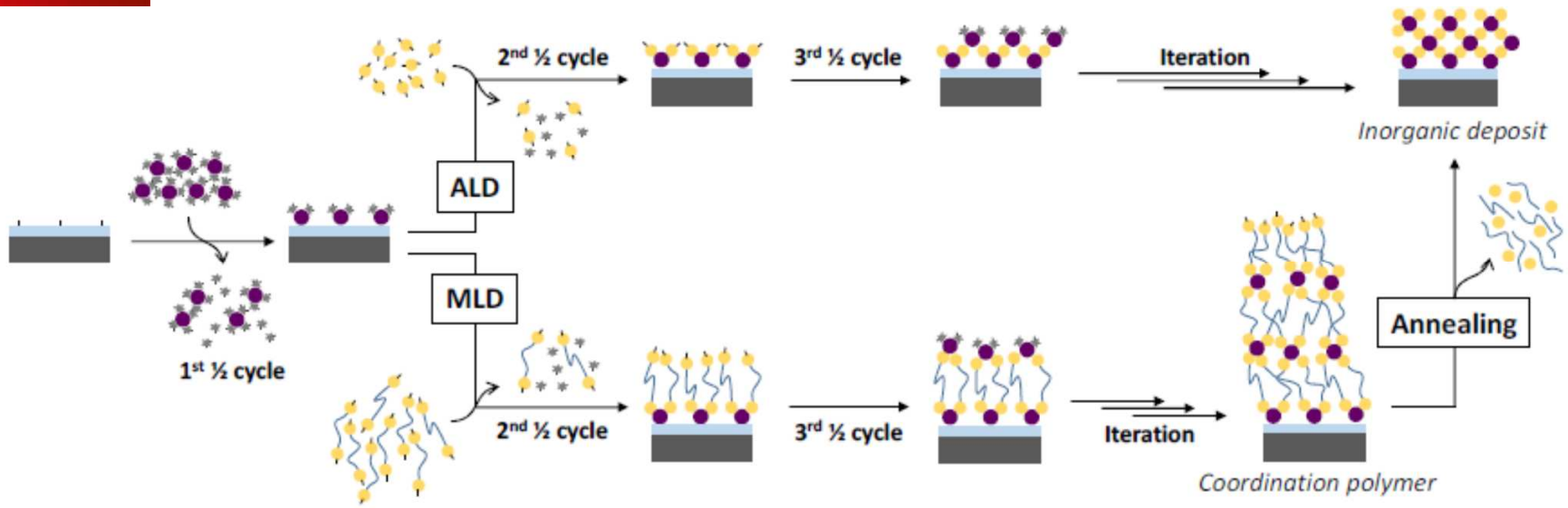


Quoc An Vu, Nature Comm, 2016

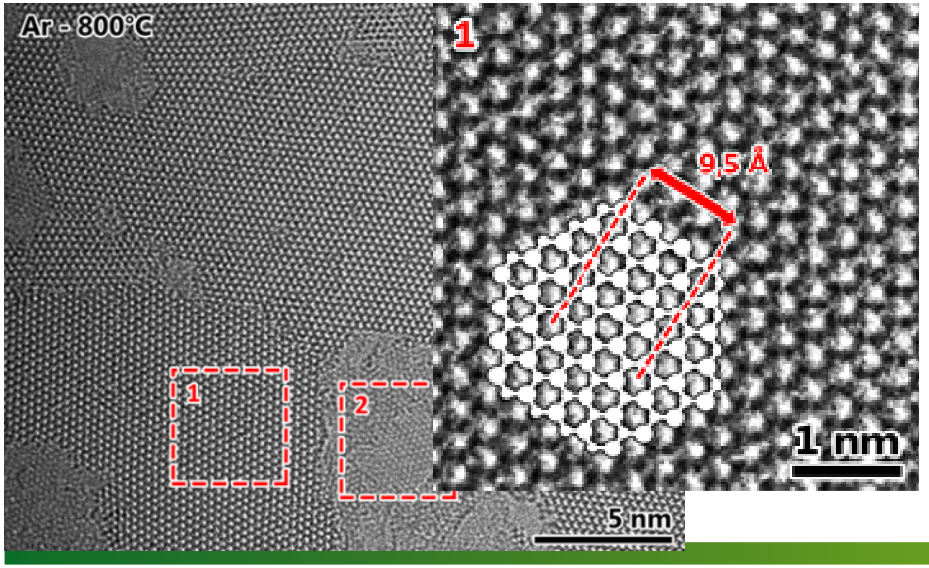
Geim et al, **Manchester team: '***Graphene cake'*

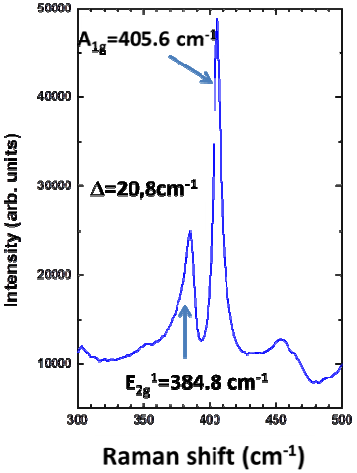


2D TMD LARGE SCALE GROWTH



Low-temperature Atomic Layer Deposition of MoS2 using a novel organometallic precursor S. Cadot, et al, ALD 2015



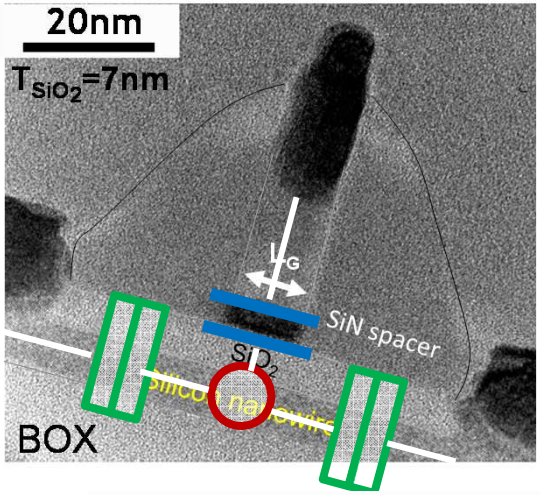


ALD of MoS2 on SiO2

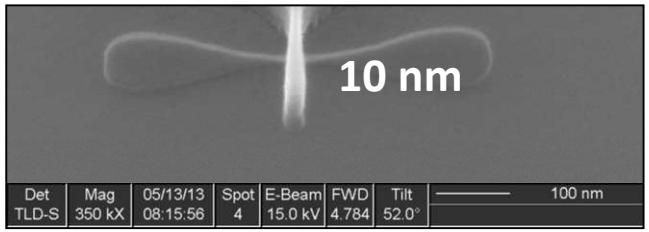
NANOWIRES TO DESIGN QUANTUM DOTS

Quantum Electronic for Efficient Computing

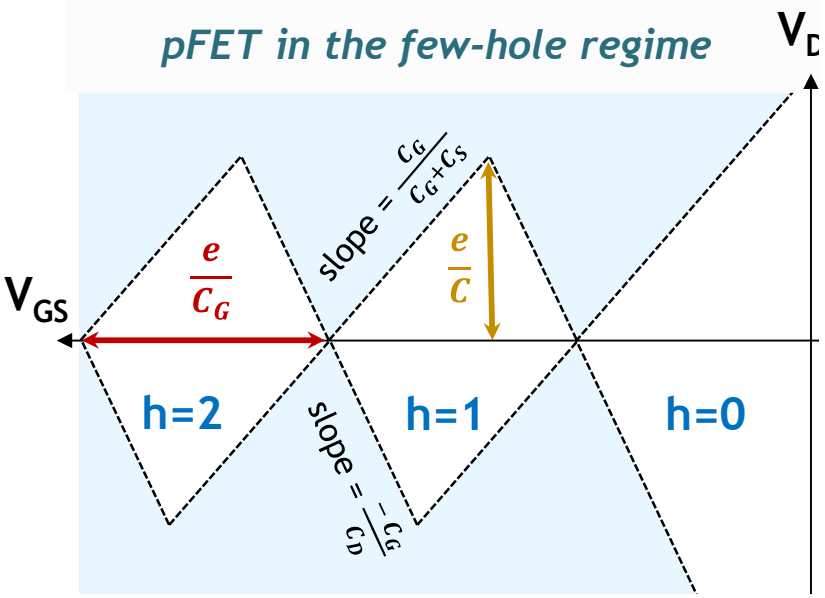
Dr Silvano de Franceschi



Wide Spacers over thin, undoped SOI

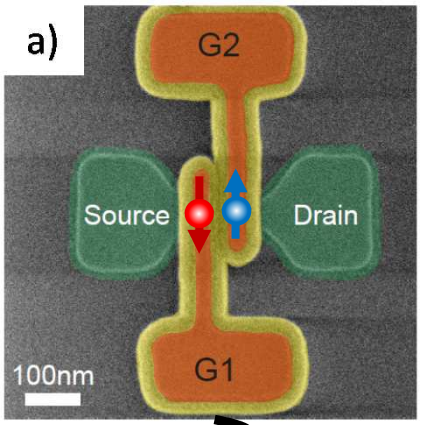


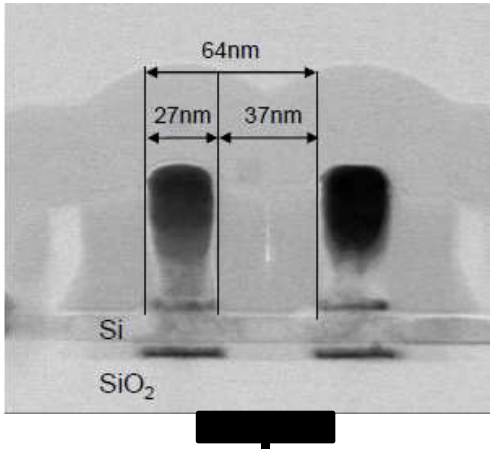
V. Deshpande, IEDM 2012, M. Vinet IEDM 2013



FETs are Turned into Single Electron or Single Hole Transistor

Si SPIN QUBITS EXTEND NANOWIRES OPERATION





Definition of a Two-Level System with Long Quantum Coherence

E field burst

Vbg

Communication Via Tunable Quantum Coupling Between Qubits

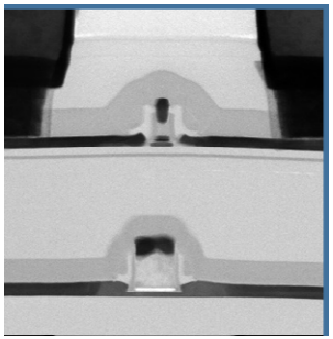
Control of A Single Qubit: Initialization, Manipulation

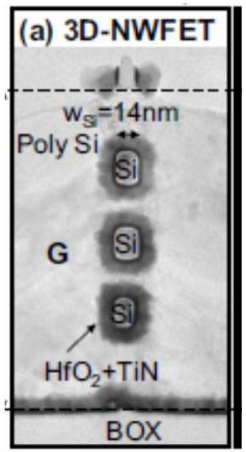
L. Hutin et al., VLSI Tech. Symp. 2016

R. Maurand et al., Nature Comm 2016

S. De Franceschi et al, 13.4 SOI Technology for Quantum Information Processing (Invited)

ROADMAP

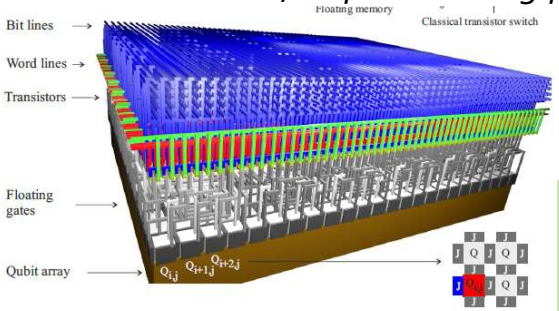




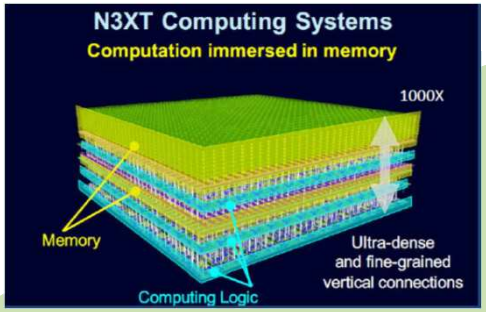
Leti advanced technologies of today

ROADMAP

M. Veldhorst et al., https://arxiv.org/pdf/1609.09700.pdf



2025

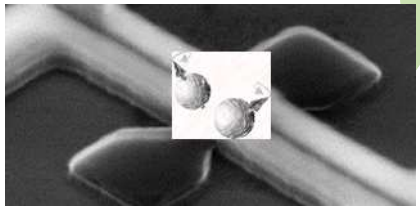


2020

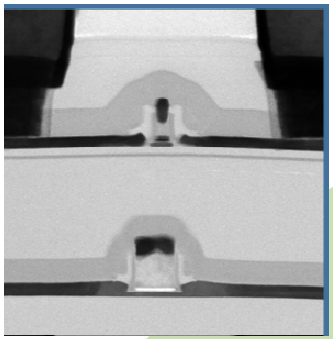
Logic in memory

NeuRAM3

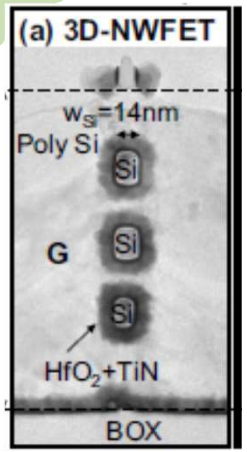
Neuromorphic computing



Quantum Computing

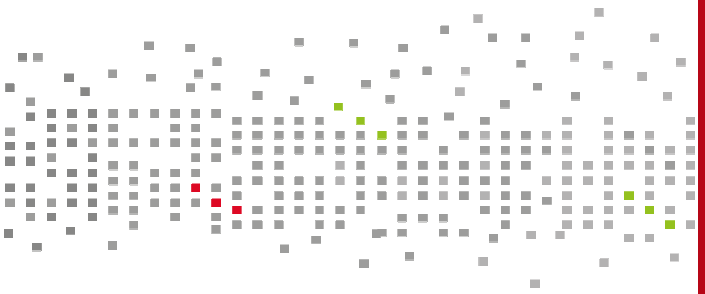


2016



Leti advanced technologies of today are supporting the shift in computing paradigms

Thank you for your attention



Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
www.leti.fr

INSTITUT CARNOT CEA LETI