3D TECHNOLOGIES: SEVERAL DISRUPTIVE TECHNOLOGIES TO LOOK AHEAD

Leti Devices Workshop | Olivier Faynot | December 4, 2016

SOMMAIRE

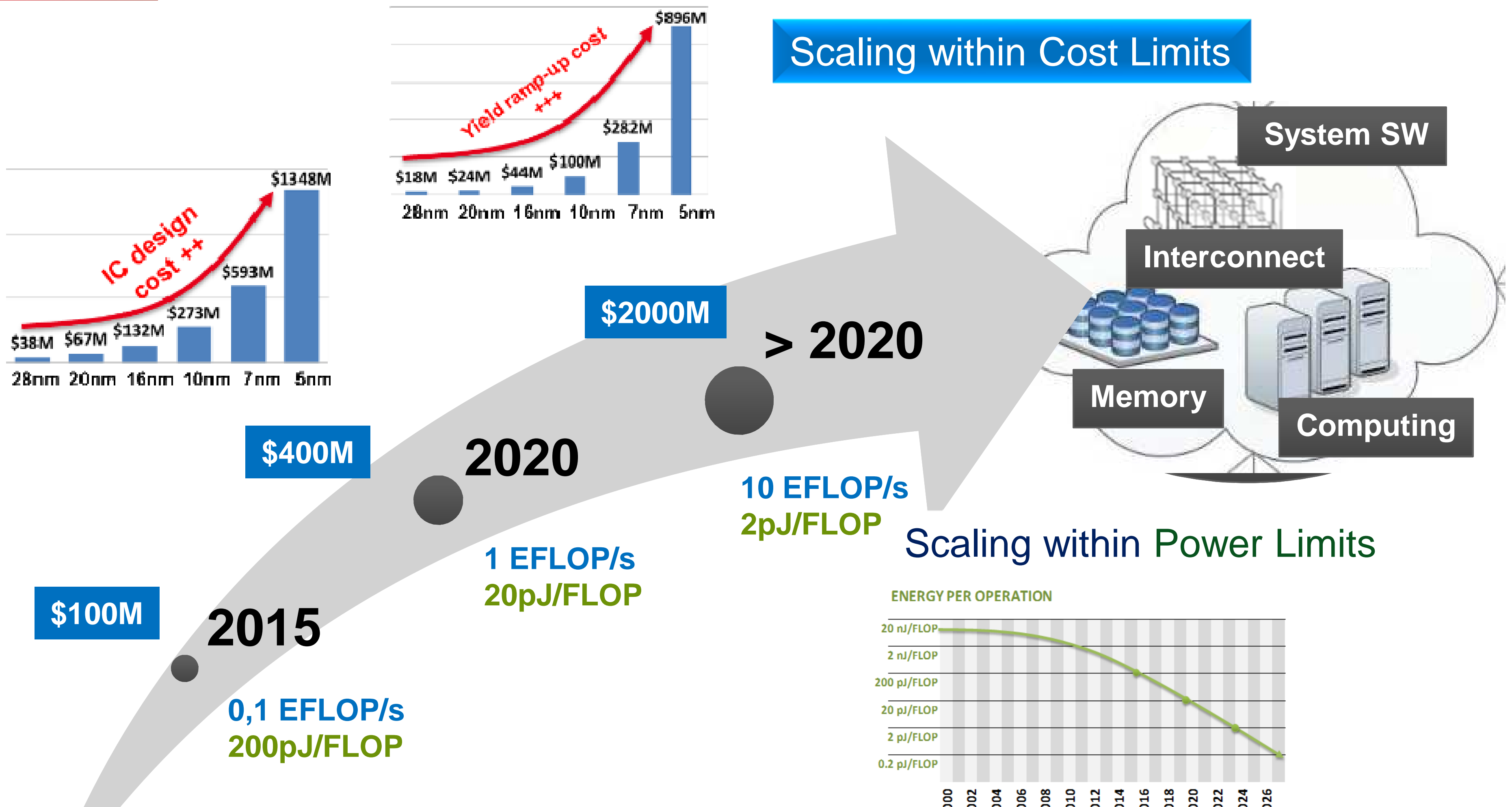
1 Top Challenges for Computing

2 How 3D Can Help?

3 Our Options Towards Fine Pitch

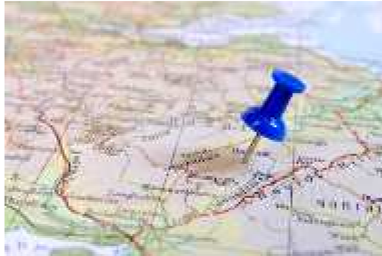
4 Summary

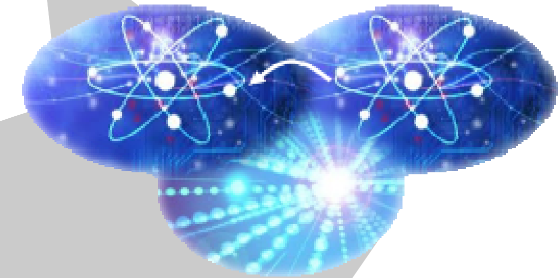
TOP CHALLENGES FOR COMPUTING



1. Cost: Disruptive Architecture and Integration Technologies are Required
2. Performance: Disruptive Technologies are Required

LETI'S ROADMAP FOR COMPUTING

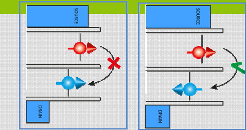




> 2020

Computer Architecture Paradigm Shift

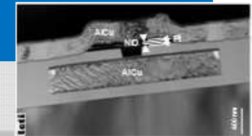
- Quantum Computing
- Neuromorphic Architectures

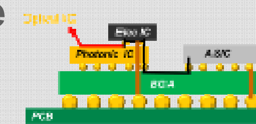


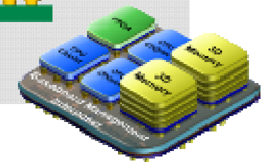
2020

Technological Shift

- New Memory Materials and Architecture
- 3D VLSI and High-Density 3D
- Integrated Silicon Photonic Dies
- Neuromorphic for Advanced Chiplet Architecture



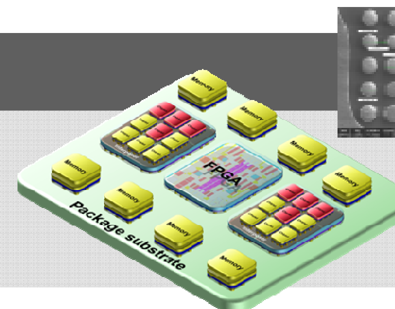


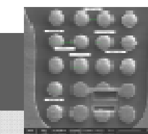


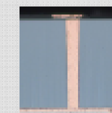
2015

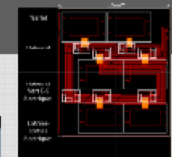
Integration Shift

- 3D Integrated Circuits
- Interposer Integrated Chiplets
- Integrated Photonic Links

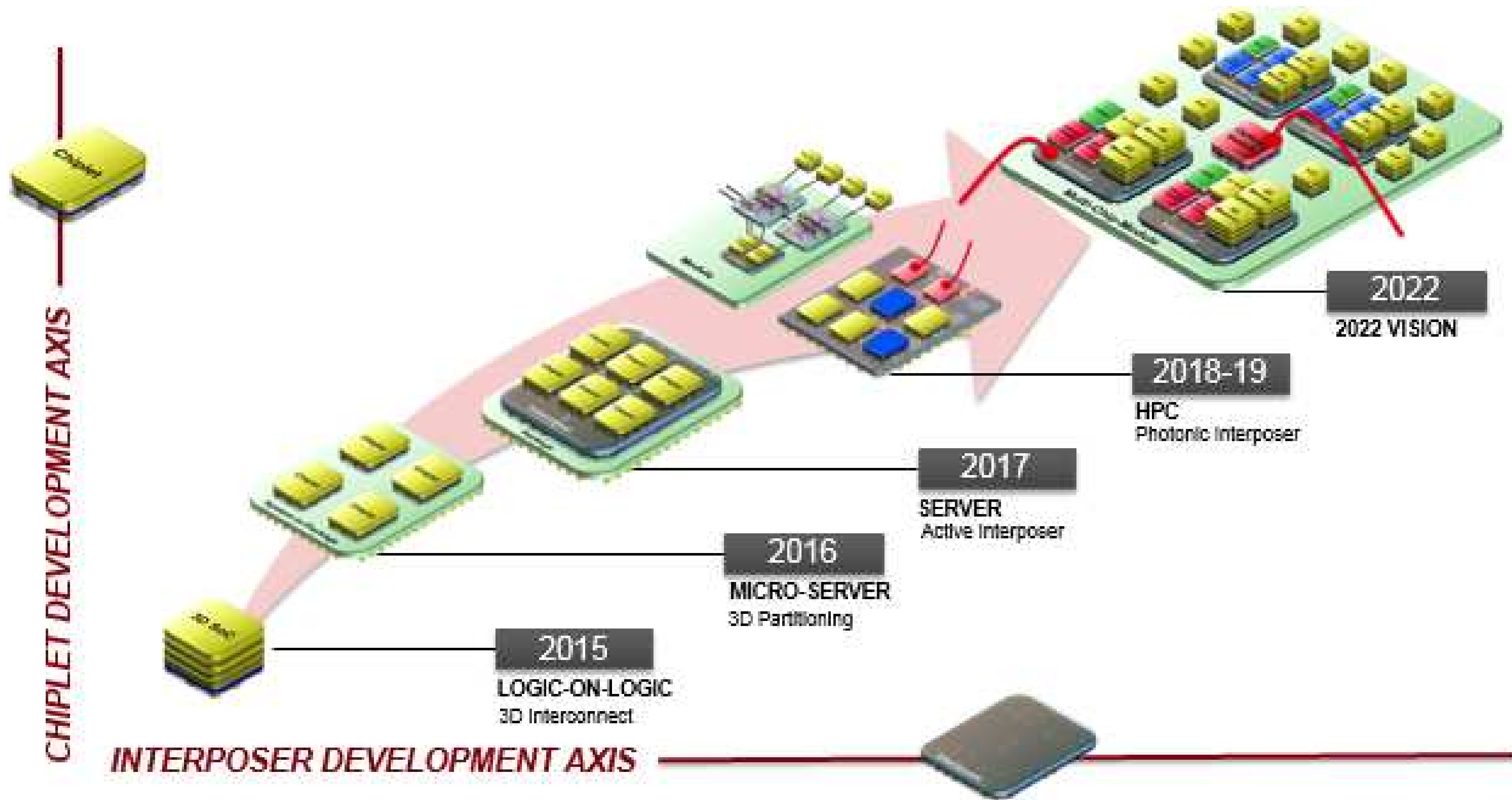








3D TECHNOLOGIES EVOLUTION



HIGH DENSITY 3D: A REAL ALTERNATIVE TO SCALING

TSV + µBump[1]
Pitch : 20 µm

~10^3 3DC/mm²
=> Entire core

Multiple cores
L2

Self Assembly
Pitch : 1-5 µm

Cu/Cu [2]
Pitch : 2-5 µm

~10^5 3DC/mm²
⇒ Logic Blocs
⇒ Logic Gates

HD-TSV [2]
Pitch : 1-3 µm

M3D (CoolCube™) [3]
Pitch : 0.05-0.1 µm

10^8 3DC/mm²
=> Transistor level

Vdd
d2d vias
gnd
x

diameter
Pitch
3D Contact = 3DC

[1] Cheramy, S., et al. “Advanced Silicon Interposer”, C2MI Workshop, 2015
[2] Patti, B., “Implementing 2.5D and 3D Devices”, In AIDA workshop in Roma, 2013
[3] Batude, P., et al. "3DVLSI with CoolCube process: An alternative path to scaling ." VLSI technology symposium 2015

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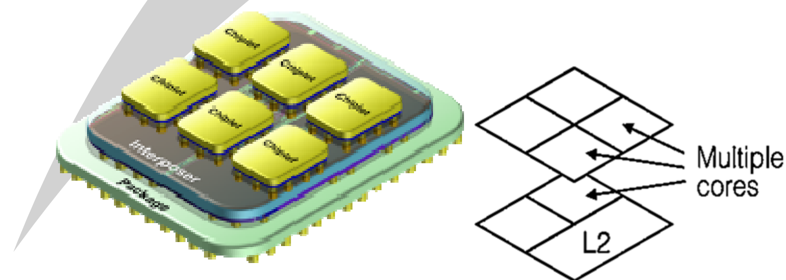

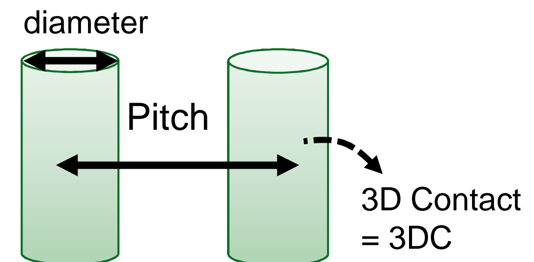

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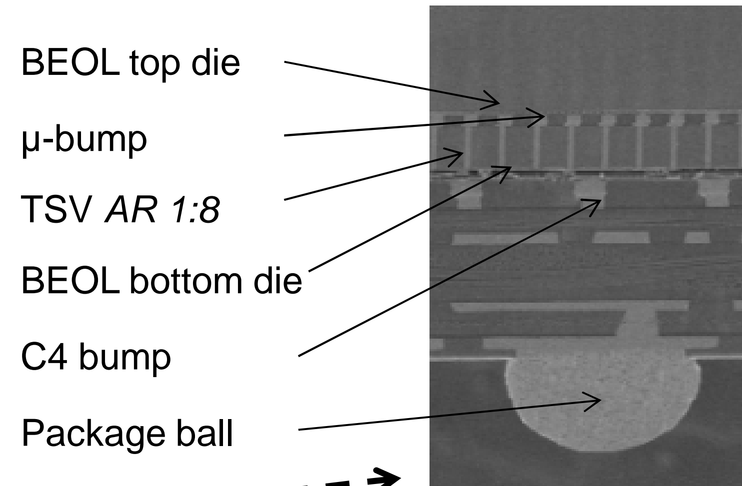
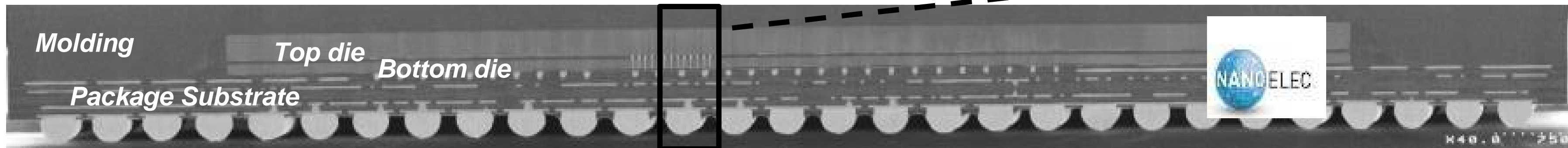
HOW 3D CAN HELP?

Network-on-Chip 3D Asynchron

- Multi core aplications, high bandwidth
- Serial links
- Logic on Logic stack
- Fauls tolerance, repair





	GeorgiaTech ISSCC'2012	*Kobe Univ. ISSCC'2013*	*This Work*
Architecture	Cache-on-CPU Manycore	Memory-on-Logic 1 layer DRAM	Logic-on-Logic 2 layers 3DNOC
Process & 3D technology	130nm F2F CuCu	90nm F2B TSV	65nm F2B TSV
3D Bandwidth	277 Mbps	200 Mbps	**326 Mbps**
3D I/O Power	-	0.56 pJ/bit	**0.32 pJ/bit**

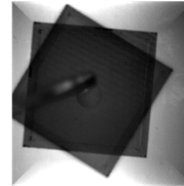
[P. Vivet et al. ISSCC'16]

3D Link Performances

- Fastest Link, **+20% (326 Mflit/s)**
- **Best Energy Efficiency, +40% (0.32 pJ/bit)**
- Self-Adaptation to Temperature, a Strong 3D Concern

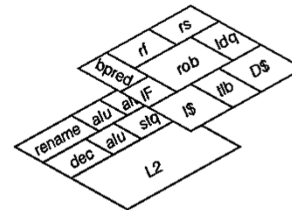
HIGH DENSITY 3D : A REAL ALTERNATIVE TO SCALING

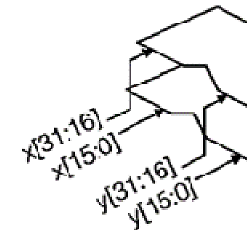
Self Assembly
Pitch : 1-5 µm

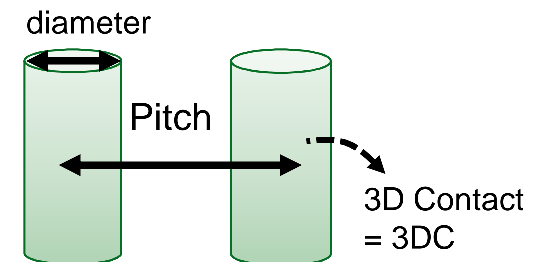


~10^5 3DC/mm²
⇒ Logic Blocs
⇒ Logic Gates

Cu/Cu [2]
Pitch : 2-5 µm







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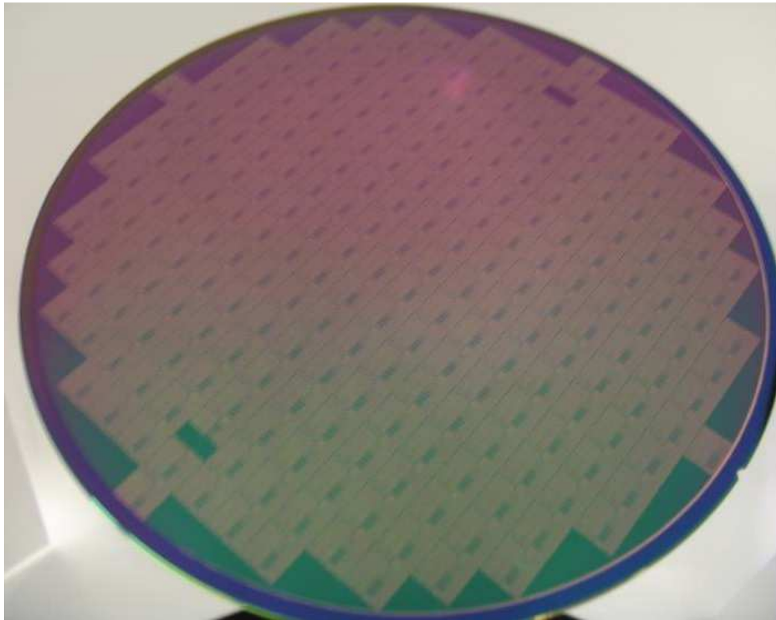
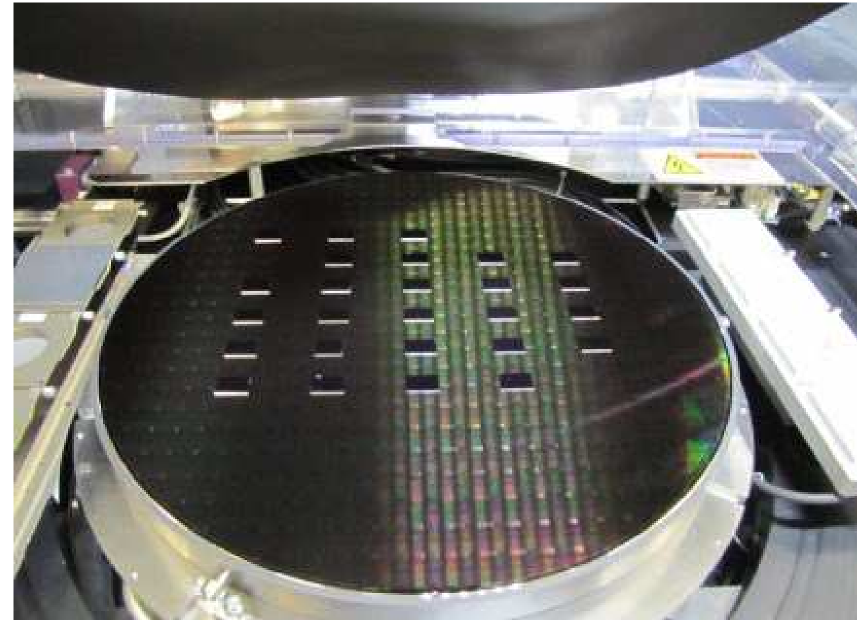
WAFER TO WAFER OR CHIP TO WAFER?





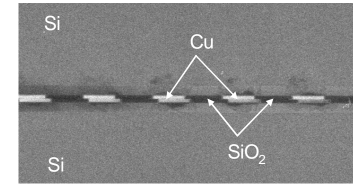
Wafer-to-wafer

Objectives:
- Ultra Fine Pitch
- Throughput

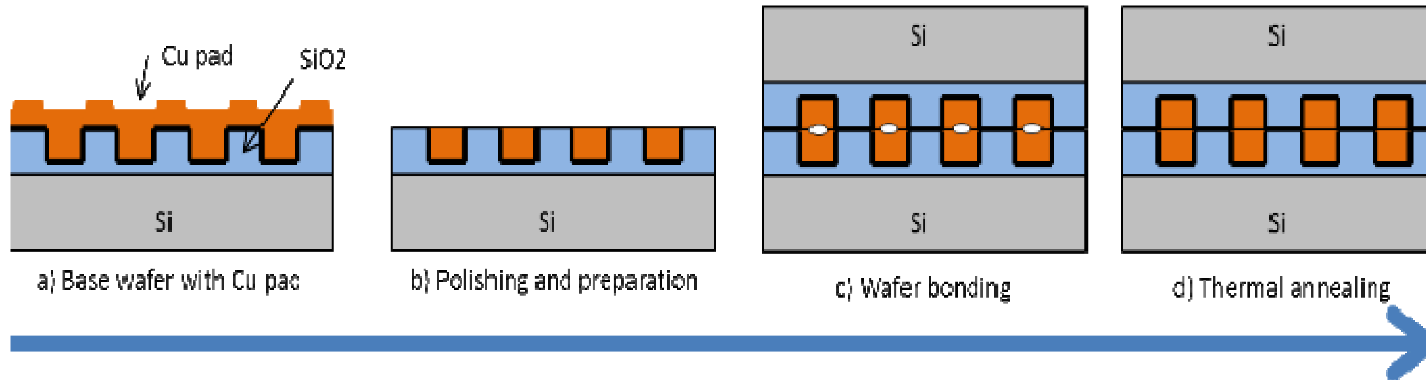
Chip-to-wafer

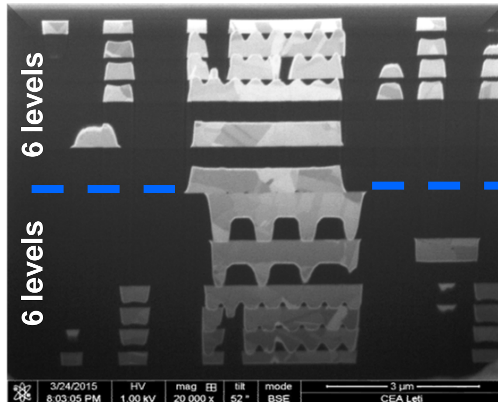
Objectives:
- Heterogeneity
- Multi Dies Stacking
- Low Yield Devices Stacking

CU/CU BONDING : PRINCIPLE

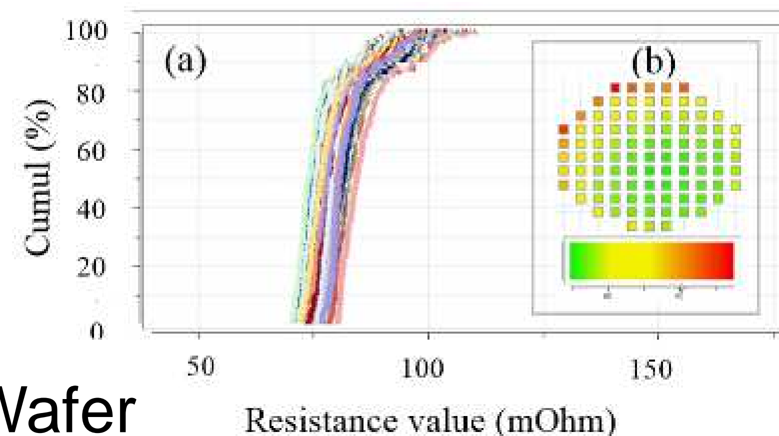


Maximize chip-to-chip connection density





- ✓ No adhesive (underfill), No pressure, Room T° process: high throughput
- ✓ From 200°C to 400°C annealing
- ✓ Pitch : **5-10µm (2015) => 1-2µm (2017)**



L. Benaissa et al, EPTC 2015
Lacourbe S.et al,, ECT2016

Demonstration done on Wafer to Wafer

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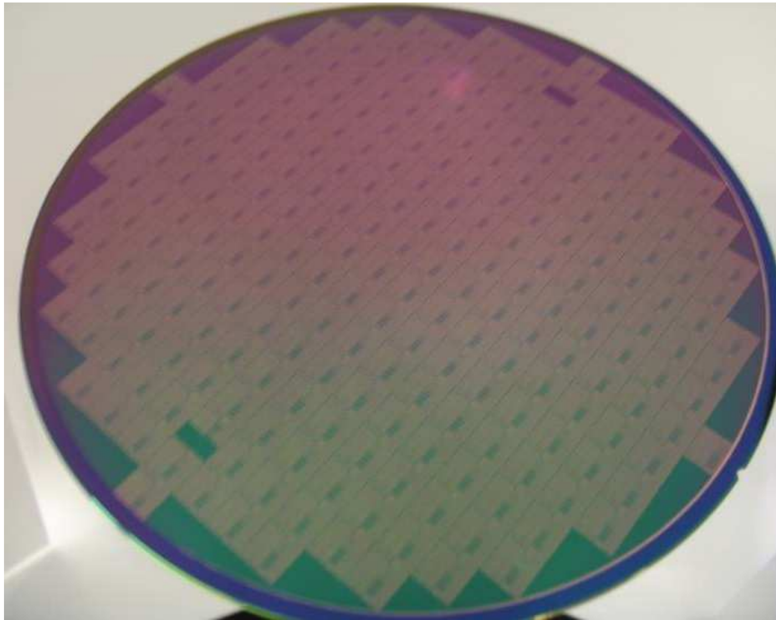

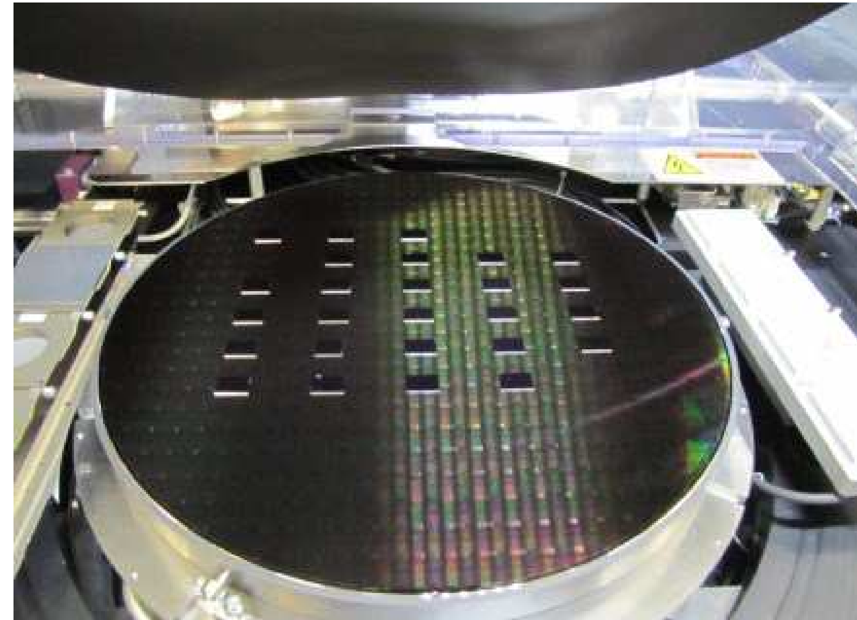

Wafer-to-wafer

Objectives:
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Chip-to-wafer

Objectives:
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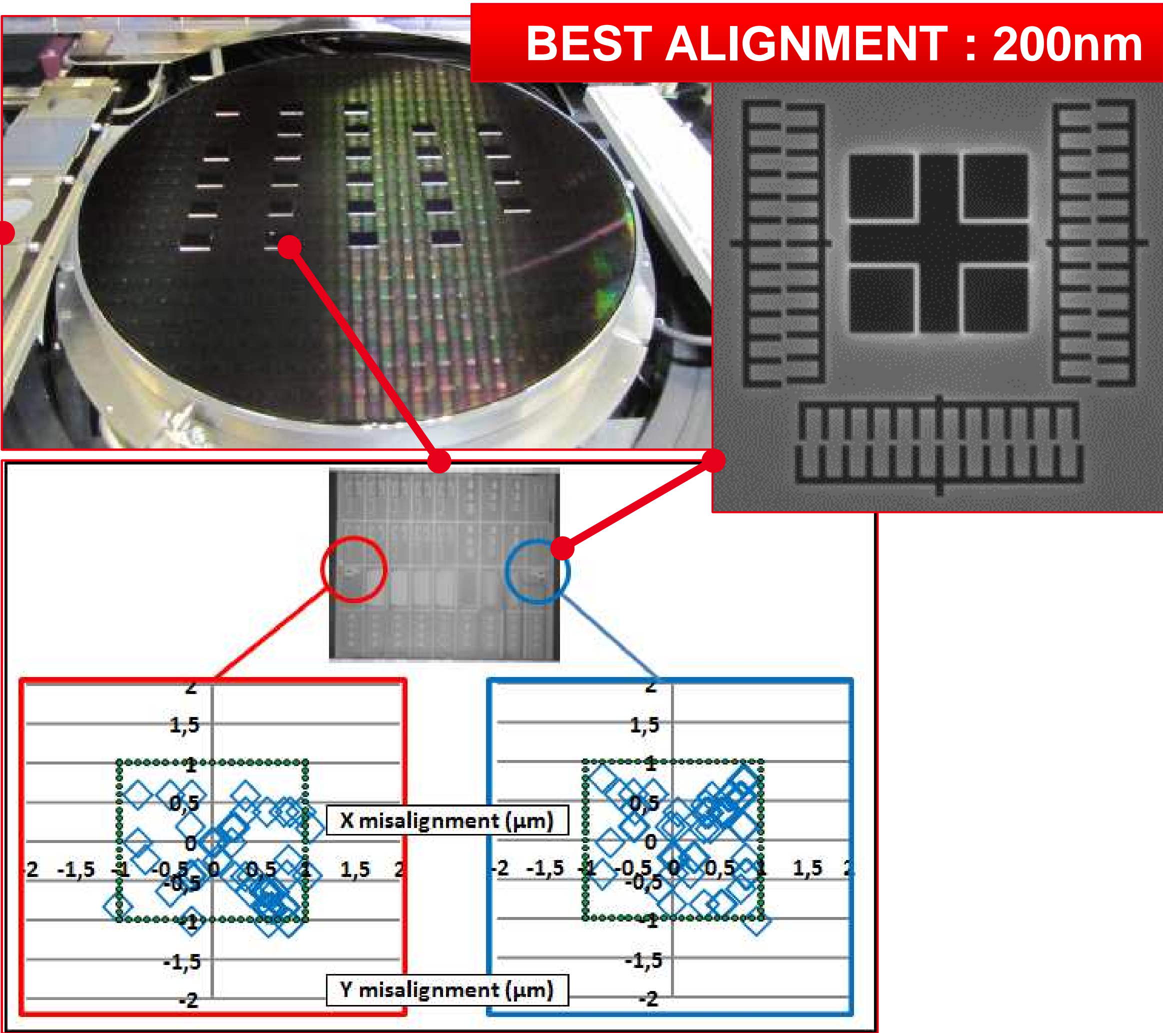
CHIP-TO-WAFER INTEGRATION PROCESS

FC300 bonding machine with ± 0.5µm post-bonding accuracy



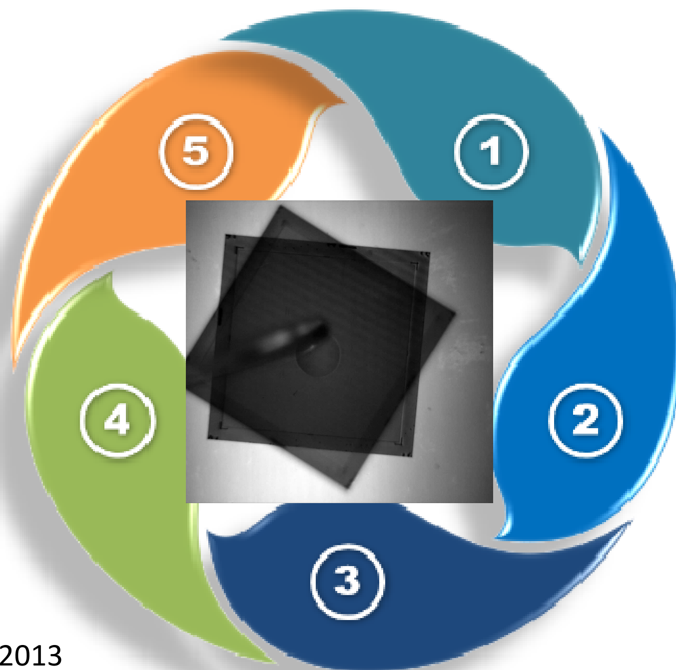
Y. Beillard, 3DIC 2013

SELF-ASSEMBLY FOR CHIP TO WAFER APPROACH

PRINCIPLE OF SELF-ASSEMBLY USING CAPILLARY FORCE

Phase 1 : Self-Alignment

- Leti's choice: capillary driven alignment
- Minimization of surface tension with capillary force



S. Mermoz, EPTC 2013

Phase 2 : Hybridation

- Leti's choice : Direct bonding

1 – LIQUID DEPOSITION ON SUBSTRATE OR DIE

2 – ROUGH PRE-POSITIONNING USING MECHANICAL TOOL

3 – REMOVAL OF THE TOP DIE

4 – SPONTANEOUS ALIGNMENT THANKS TO CAPILLARY FORCE

5 – LIQUID EVAPORATION AND HYBRIDATION

High Throughput | Collective Bonding

High Alignment Accuracy (< 1 µm) | Direct Bonding Compatibility

OUR ROADMAP FOR THE FUTURE

… Based on closed partnership with equipment suppliers

WtW alignment (@ 3σ)

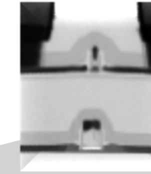
CtW alignment (@ 3σ)

Highly depend on throughput

WtW alignment (@ 3σ)	CtW alignment (@ 3σ)
+/-40nm	
+/-100nm	+/-500nm
+/-200nm	+/-1000nm
+/-1000nm	+/-2000nm

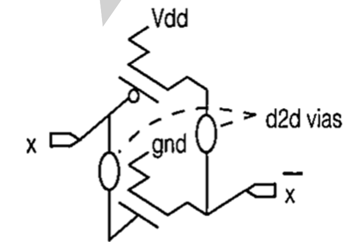
2015 2016 2017 2018

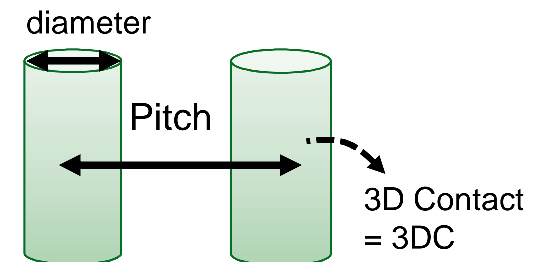
HIGH DENSITY 3D : A REAL ALTERNATIVE TO SCALING



M3D (CoolCube™) [3]
Pitch : 0.05-0.1 µm

10^8 3DC/mm²
=> Transistor level





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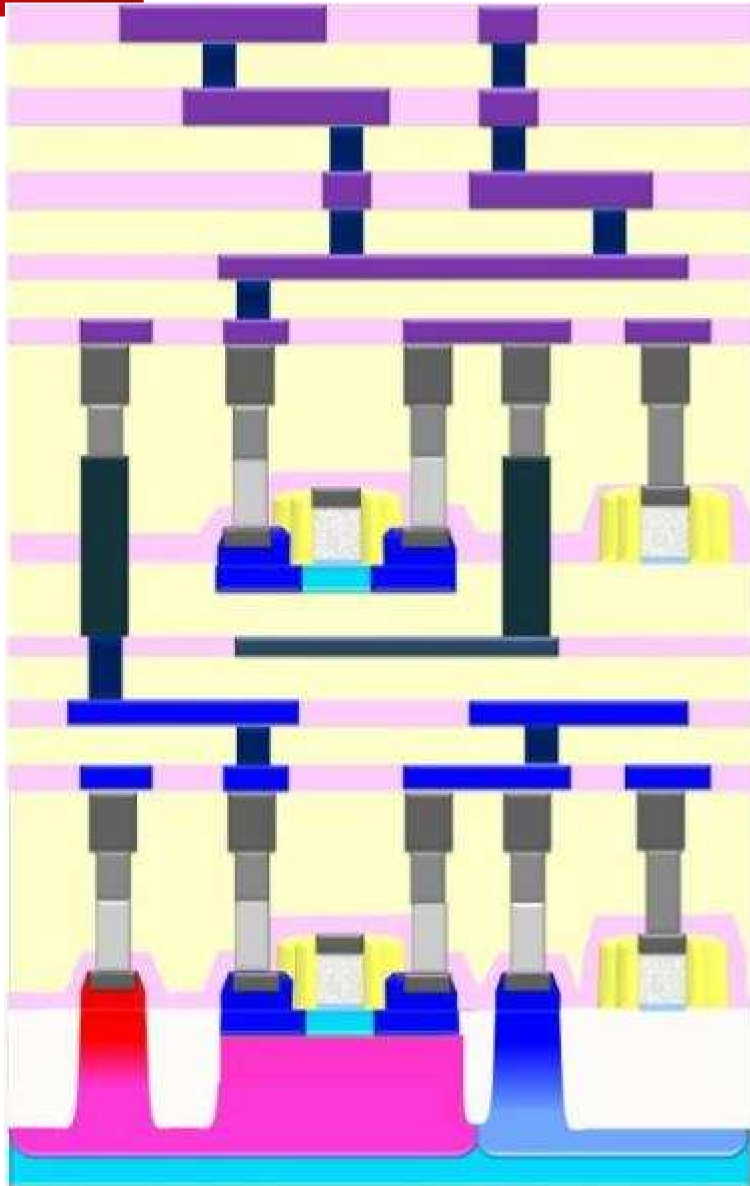
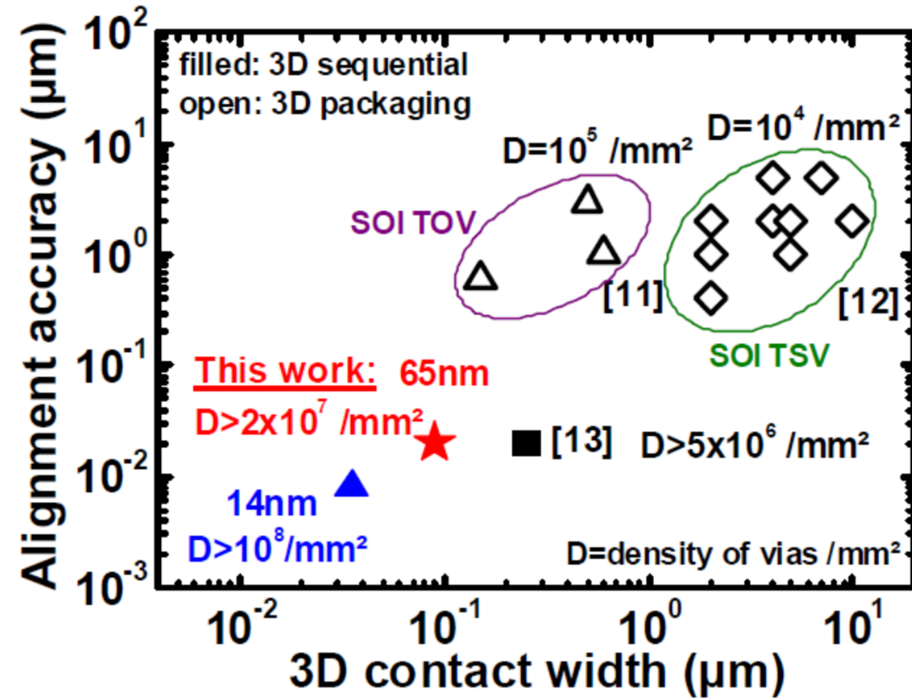
COOLCUBE™ TECHNOLOGY





Bottom transistor	top transistor
BULK	Trigate
FinFET	FinFET
FDSOI	FDSOI
Trigate	

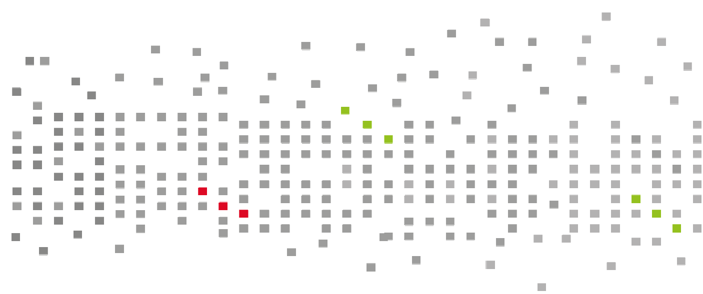
ex 2 (FinFET → Trigate)
ex 1 (BULK → FDSOI)

SUMMARY

- **Yes, 3D Can Help the Computing Roadmap!**
- **Early Demonstrations Done!**
- **LETI is Working Towards Several Disruptive Options Devoted to Fine Alignement and Fine Pitches**
  - Cu/Cu Hybrid Bonding to Achieve 1µm Pitch on Wafer to Wafer Approaches
  - Self-Assembly for Die to Wafer and high Troughputs
  - Coolcube^{TM} Technology for Transistor Level Connections

Part of this work was partly funded thanks to the French national program "Programme d'Investissements d'Avenir, IRT Nanoelec" ANR-10-AIRT-05.

Thank you for your attention



Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
www.leti.fr