Abundant-Data Computing:

The N3XT 1,000X

Subhasish Mitra

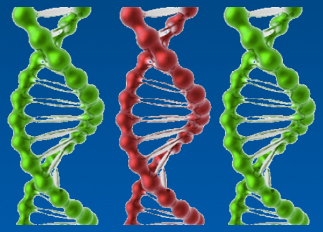


Department of EE & Department of CS

Stanford University

World Relies on Electronics

Genomics



Smart Cities



Military



Inte hing





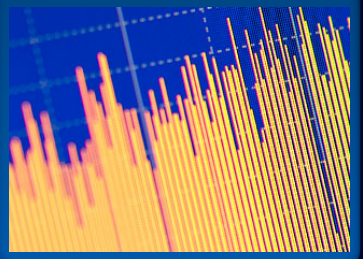


Computational demands *exceed* Processing capability

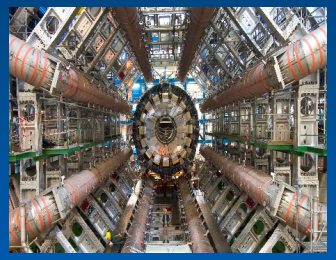
Security



Finance



Science





US National Academy of Sciences (2011)

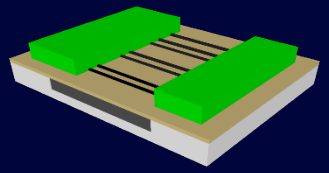
Solution: Nano*systems*

Transform new nanotech

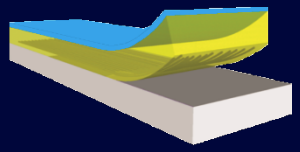
into new systems

enable new applications

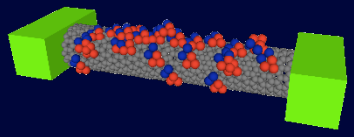
New devices



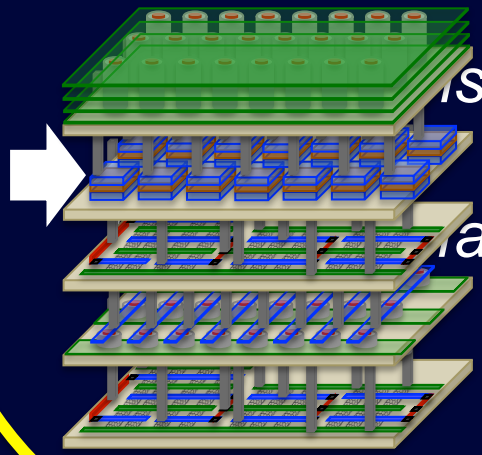
New fabrication



New sensors



New Architectures



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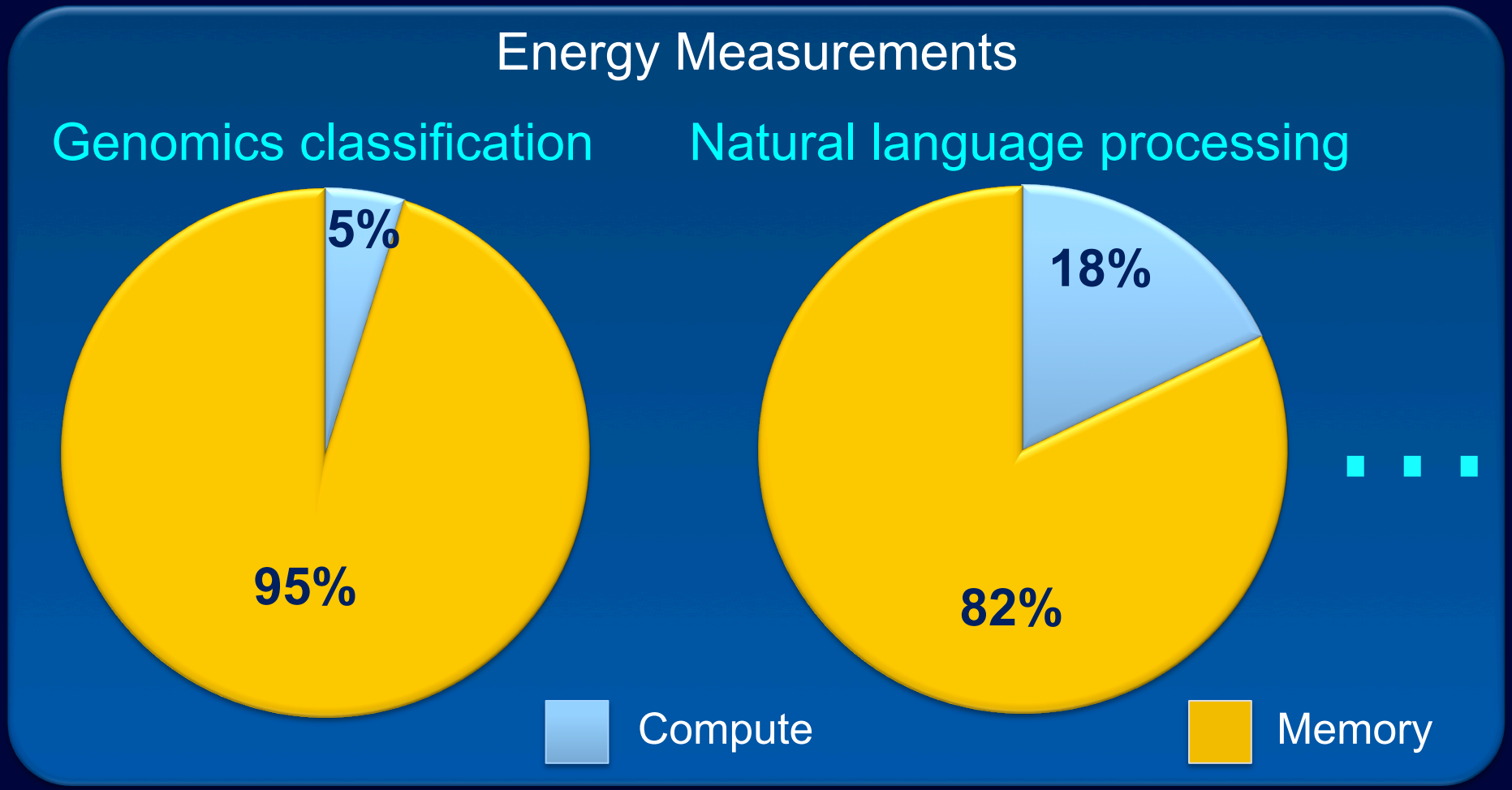
abricatio



Abundant-Data Applications

Huge memory wall: processors, accelerators



Intel performance counter monitors 2 CPUs, 8-cores/CPU + 128GB DRAM

Nano-Engineered Computing Systems Technology

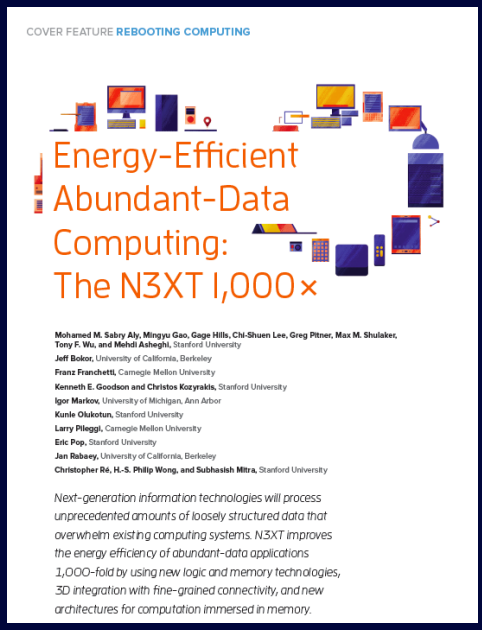








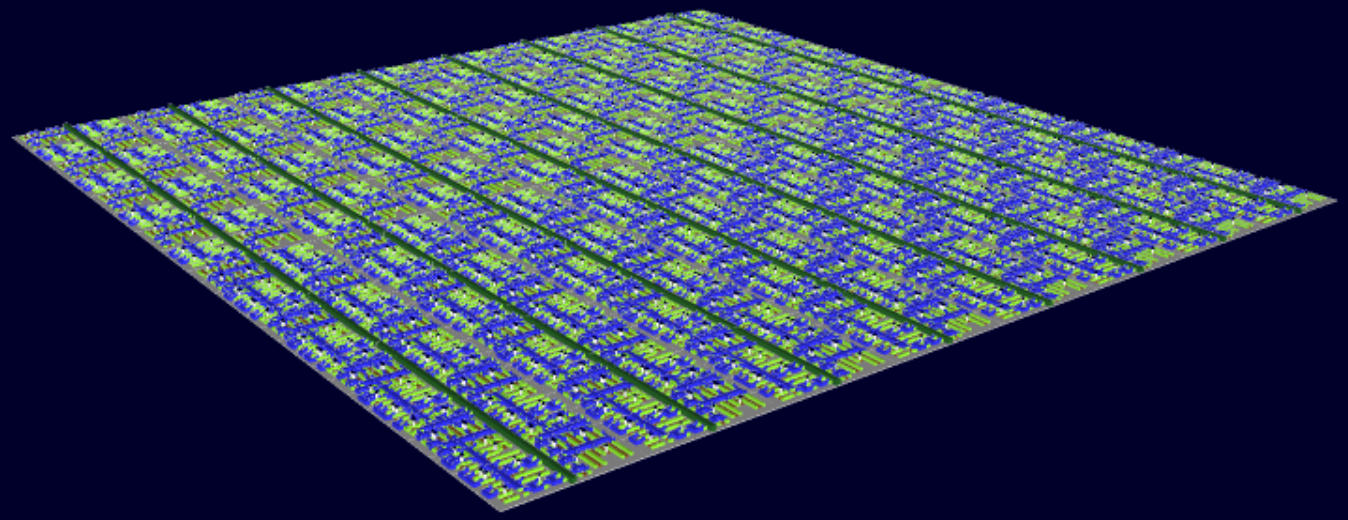




[Aly IEEE Computer 15]

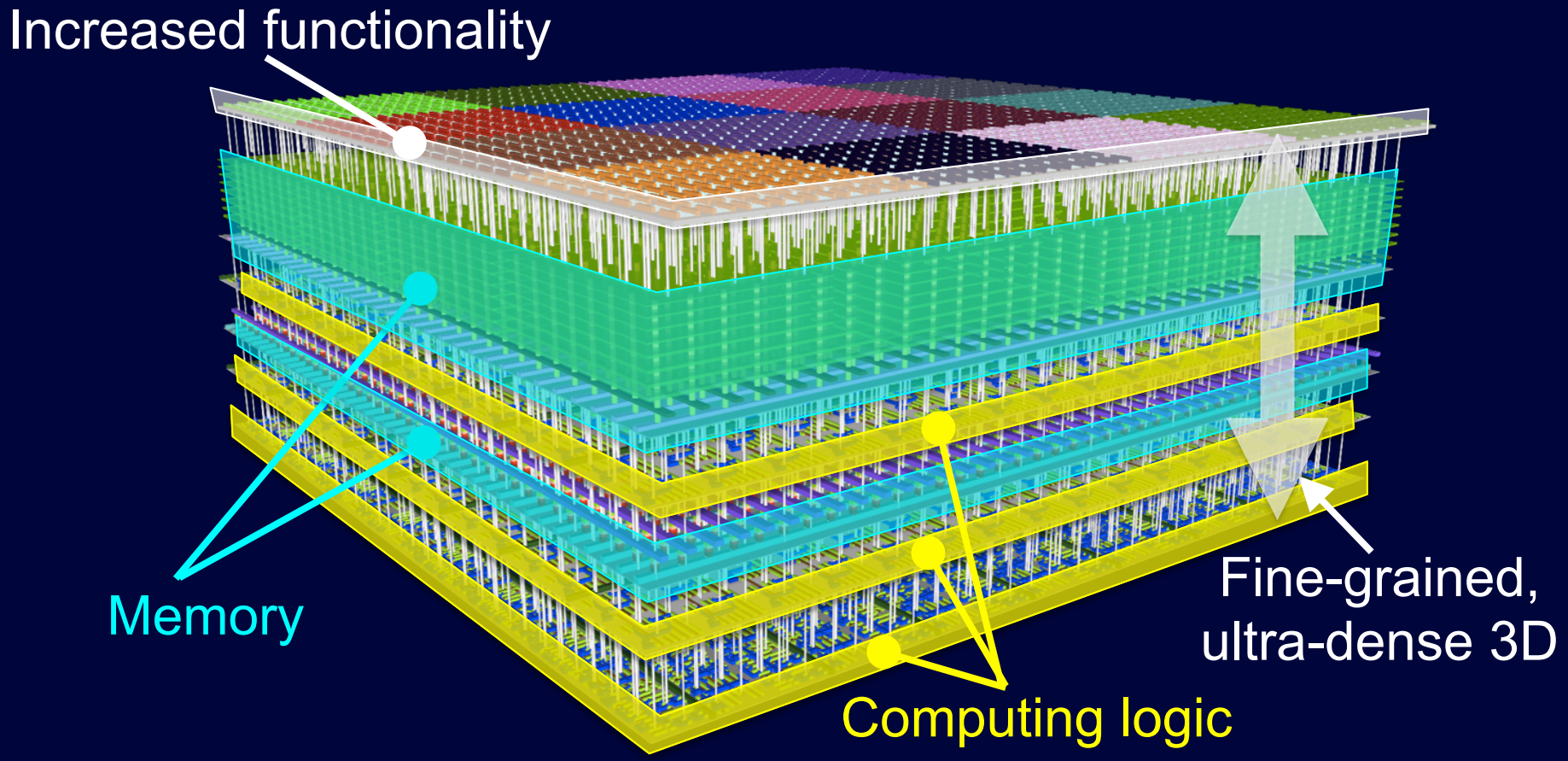
N3XT Nanosystems

Computation immersed in memory



N3XT Nanosystems

Computation immersed in memory



Impossible with today's technologies

N3XT Computation Immersed in Memory

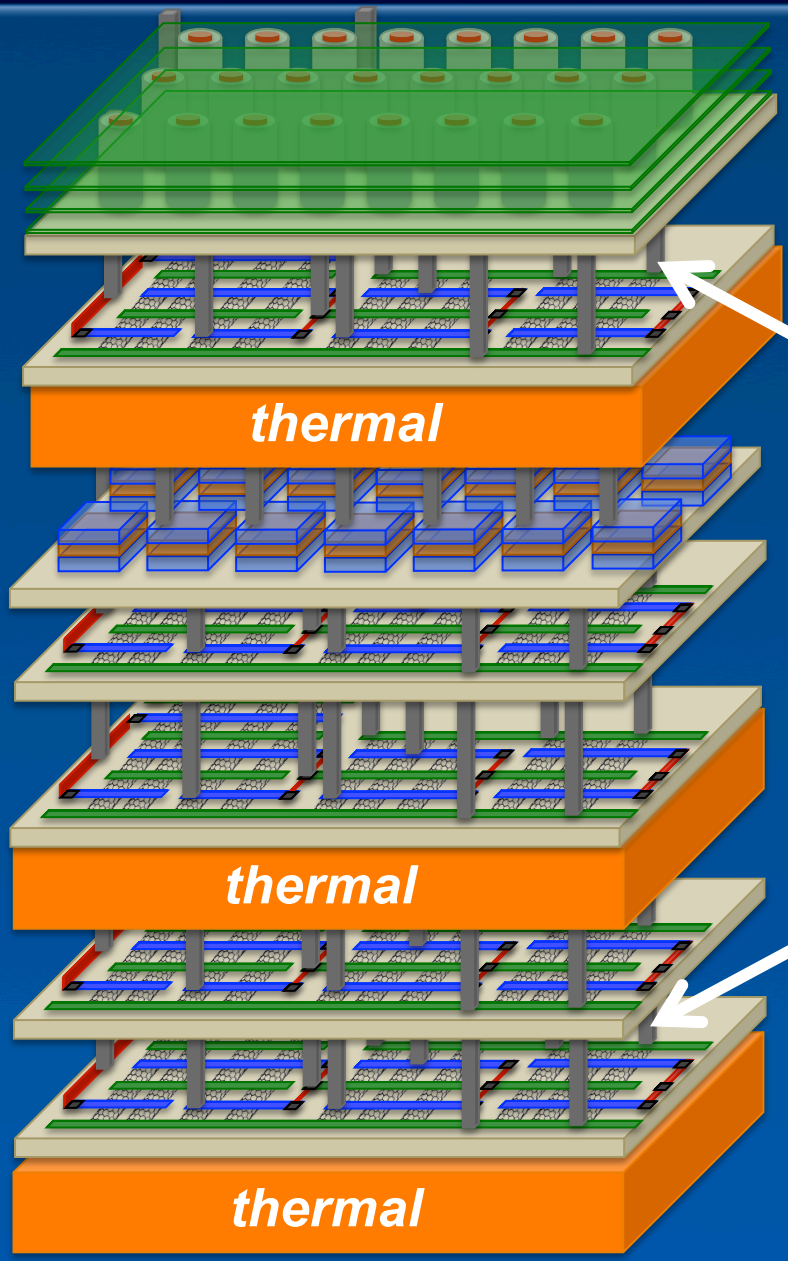
3D Resistive RAM
Massive storage

1D CNFET, 2D FET
Compute, RAM access

STT MRAM
Quick access

1D CNFET, 2D FET
Compute, RAM access

1D CNFET, 2D FET
Compute, Power, Clock

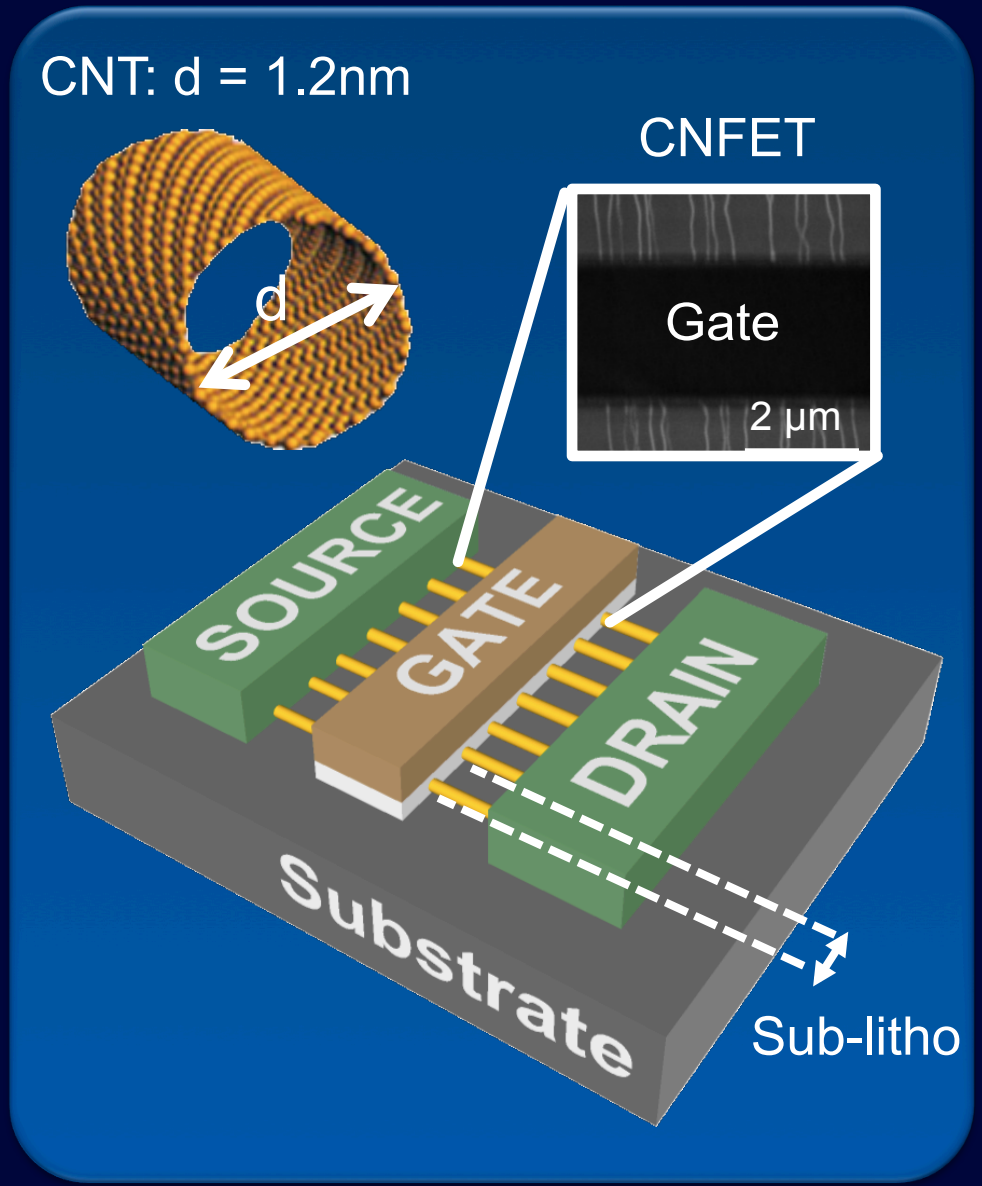


No TSV

Ultra-dense, fine-grained vias

Silicon compatible

Carbon Nanotube FET (CNFET)



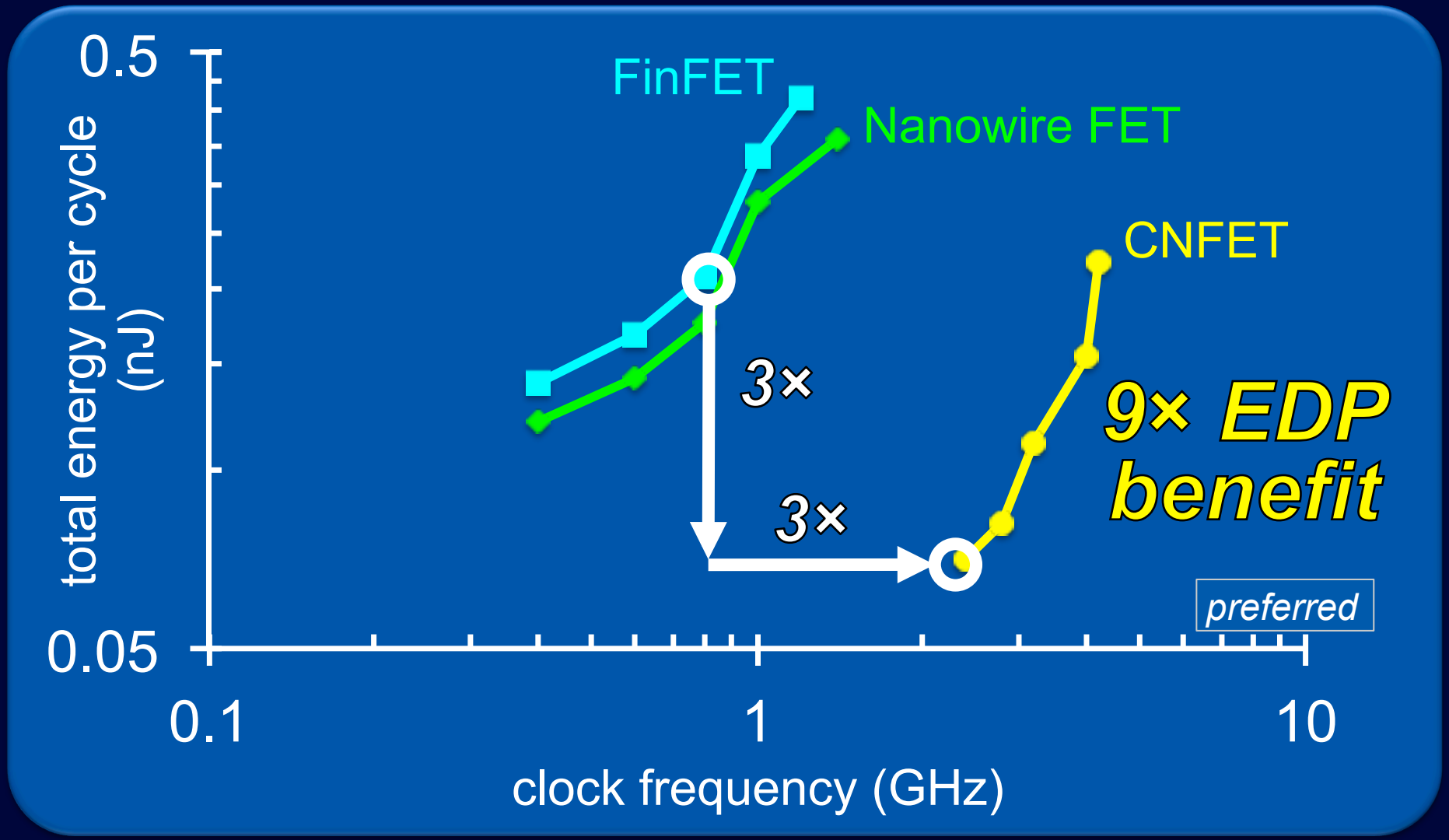
Energy **D**elay **P**roduct

- ~ 10X benefit

Full-chip case studies

[IBM, IMEC, Stanford]

Example: OpenSPARC T2



[Stanford + IMEC, Unpublished]

Many FAQs Answered

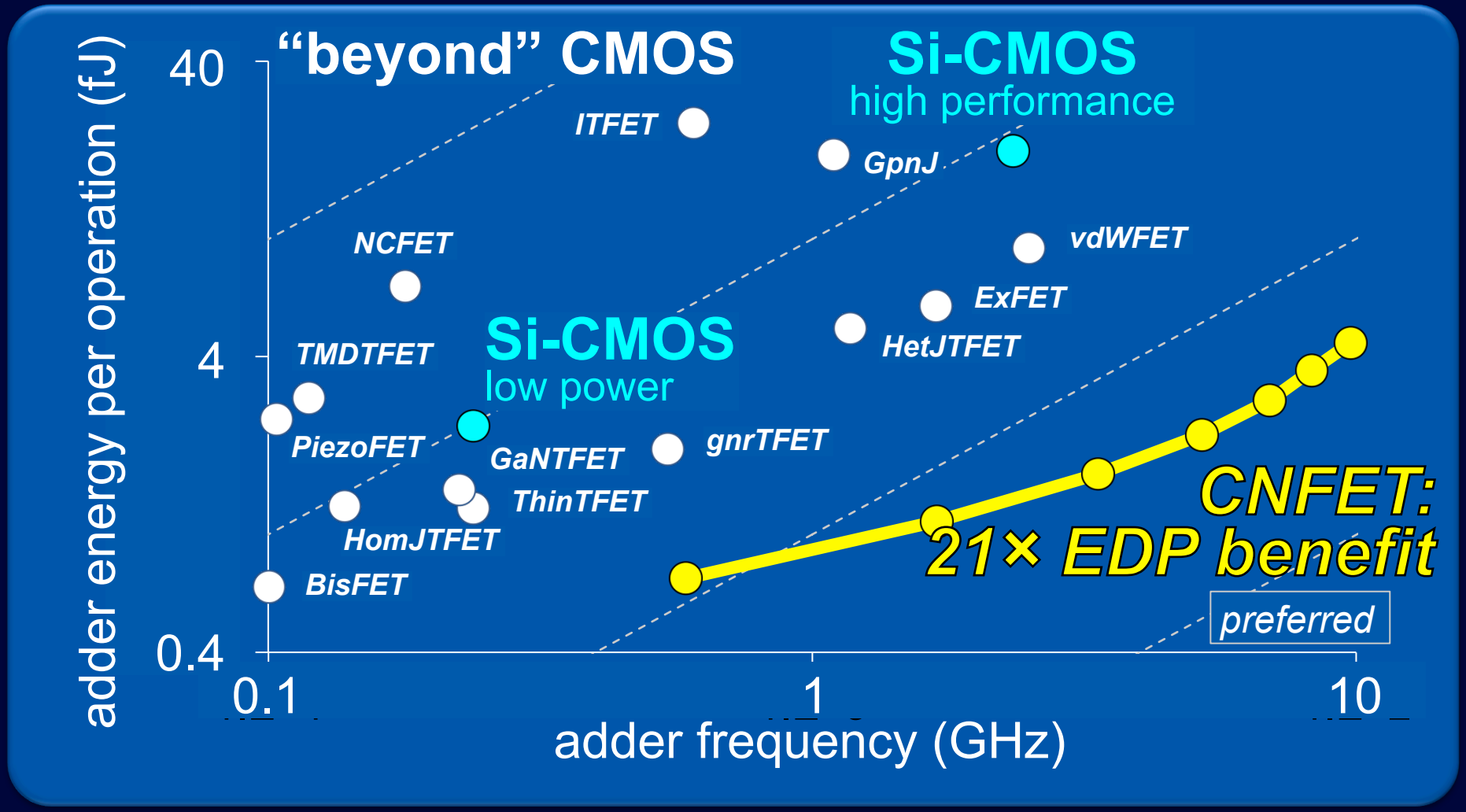

G. Hills


J. Zhang

1. Where do benefits come from ?
2. Wires limit performance ? Why research FETs ?
3. CNFET contact resistance ?
4. Aren't FETs good enough already ?
5. CNT variations ?

Putting into Perspective

- Existing technology benchmarking **+ CNFETs**

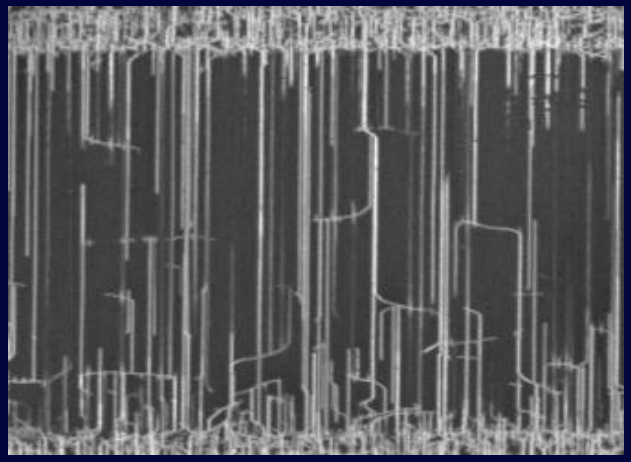


32-bit adder [Nikonov & Young, 2013 & 2015]

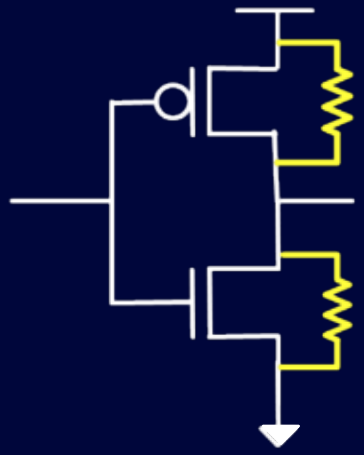
Big Promise, Major Obstacles

- Process advances alone inadequate

Mis-positioned CNTs



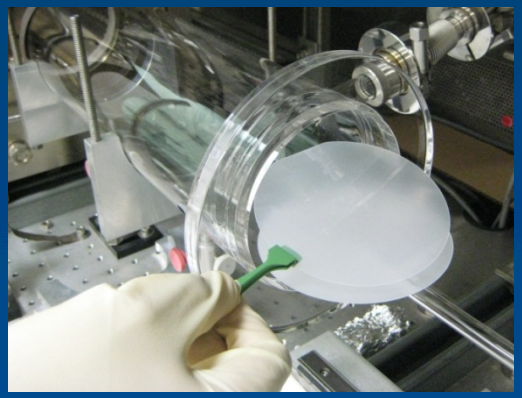
Metallic CNTs



Imperfection-immune paradigm

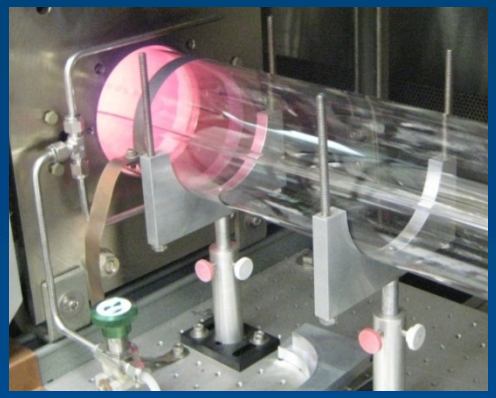
[Zhang IEEE TCAD 12]

First Wafer-Scale Aligned CNT Growth

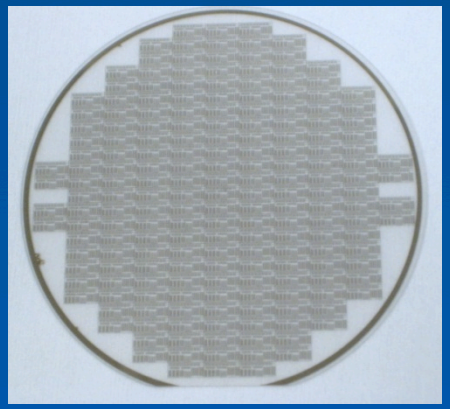


Quartz wafer
with catalyst

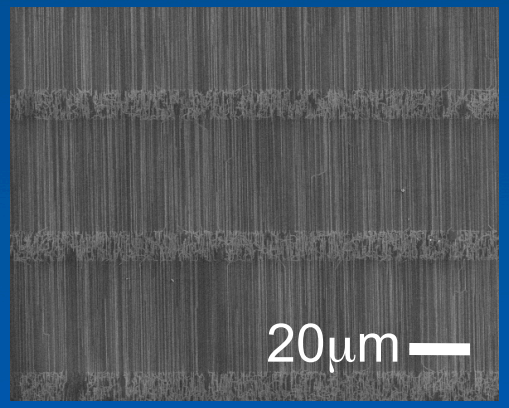
Aligned
CNT growth



Quartz wafer with CNTs



99.5% aligned CNTs



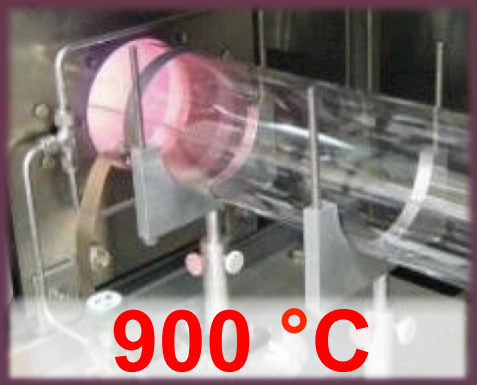
Stanford Nanofabrication Facility

[Patil VLSI Tech. 08, IEEE TNANO 09]

Wafer-Scale CNT Transfer

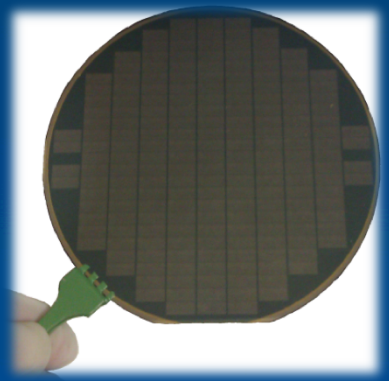
High-temperature CNT growth

Low-temperature circuit fabrication



CNT transfer

120 °C

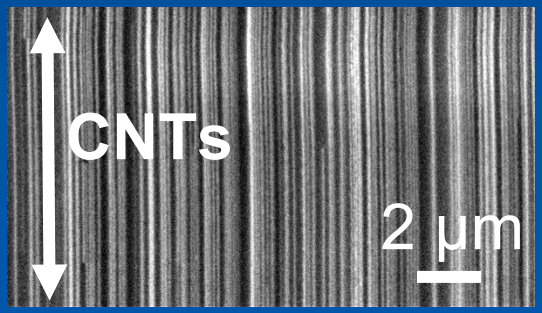


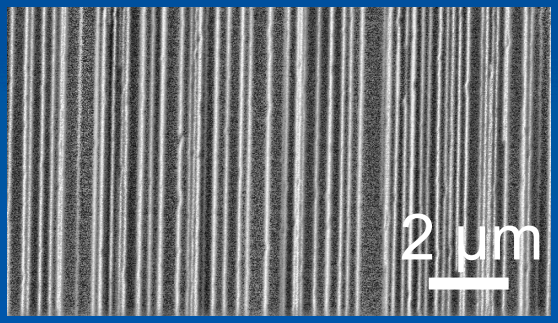
Before transfer

Quartz

After transfer

SiO_2/Si





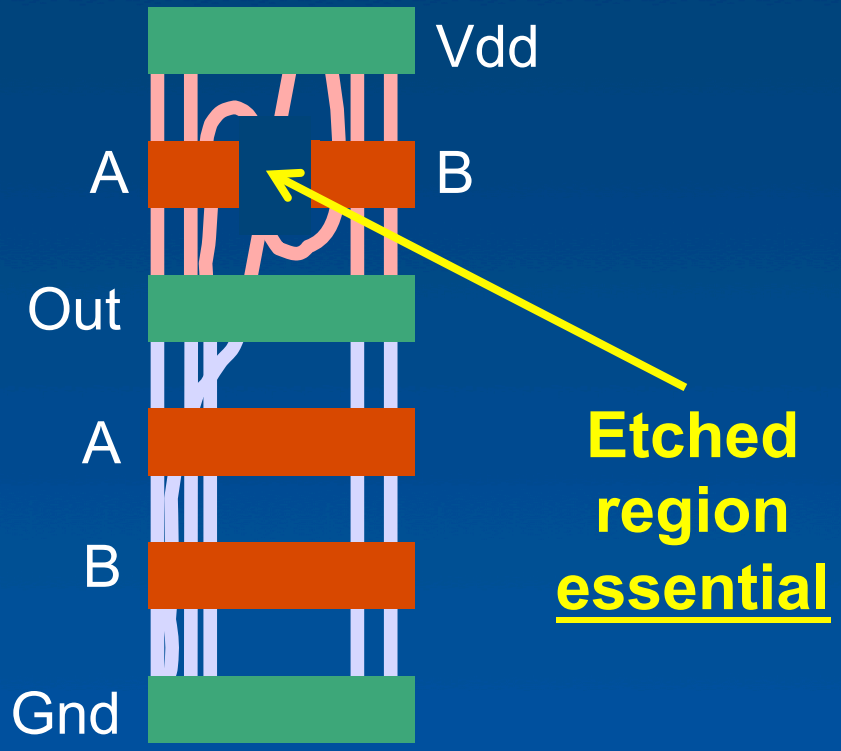
[Patil VLSI Tech. 08, IEEE TNANO 09]

Imperfection-Immune



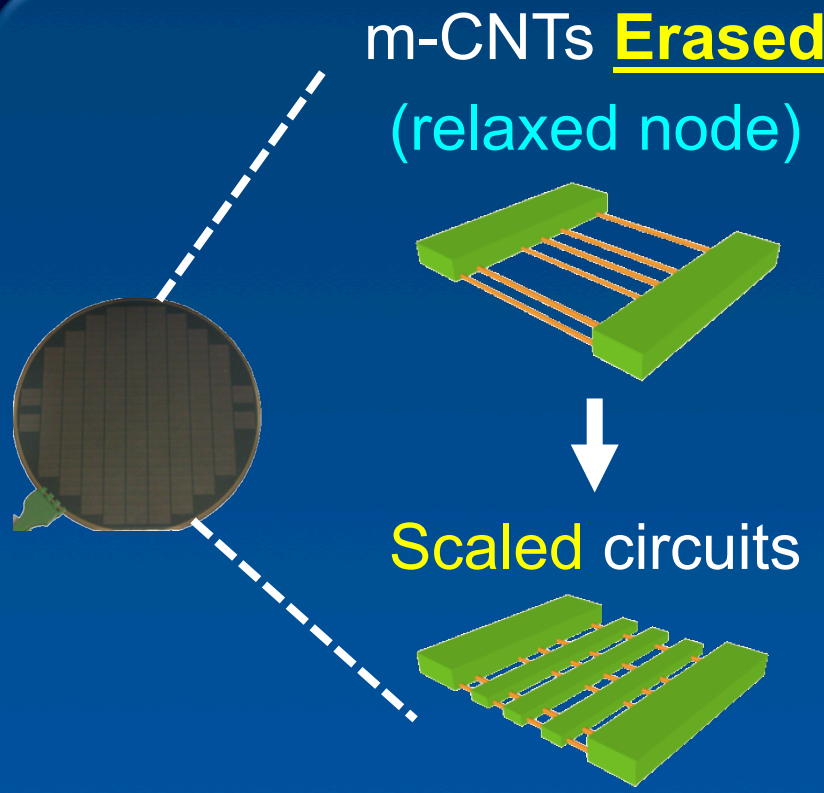
N. Patil

Mis-positioned CNTs



- Arbitrary logic functions

Metallic CNTs



- Scalable m-CNT Removal

[Patil Symp. VLSI Tech. 08, TCAD 09, Shulaker IEDM 15]

Most Importantly

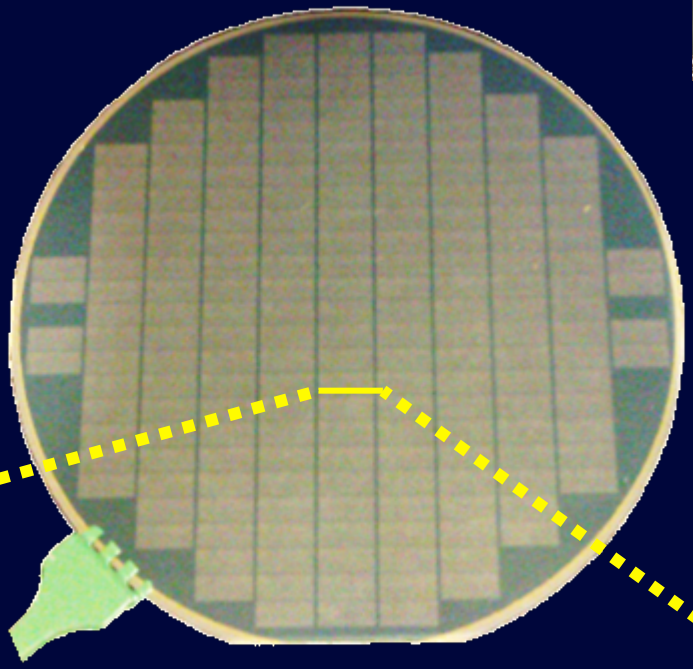
- VLSI processing
  - No per-unit customization
- VLSI design
  - Immune CNT library

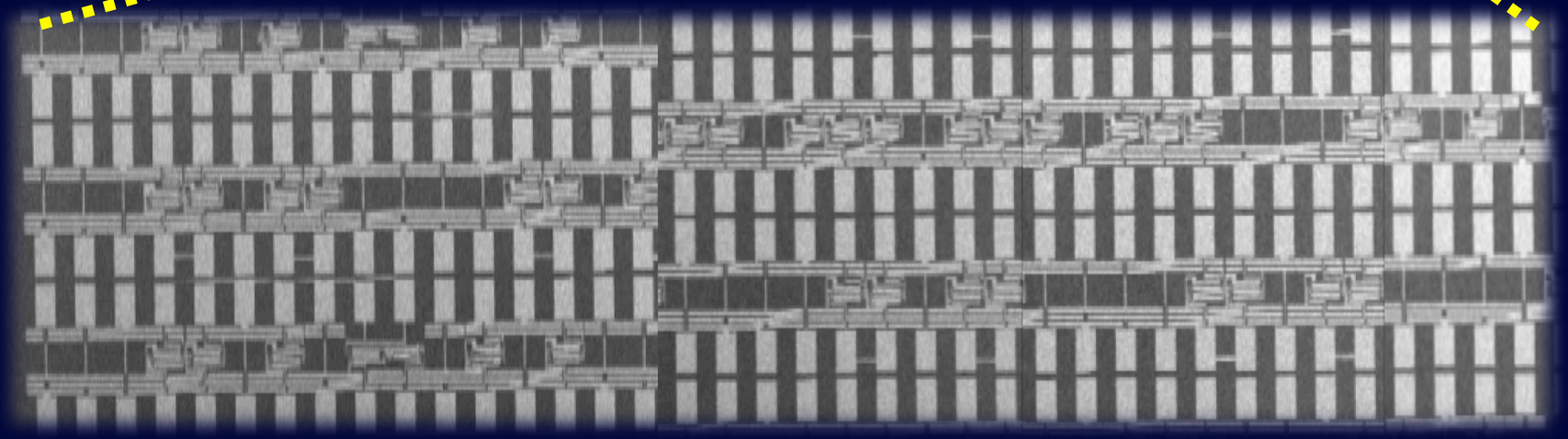
CNT Computer



Prof. M. Shulaker, MIT







[Shulaker Nature 13]

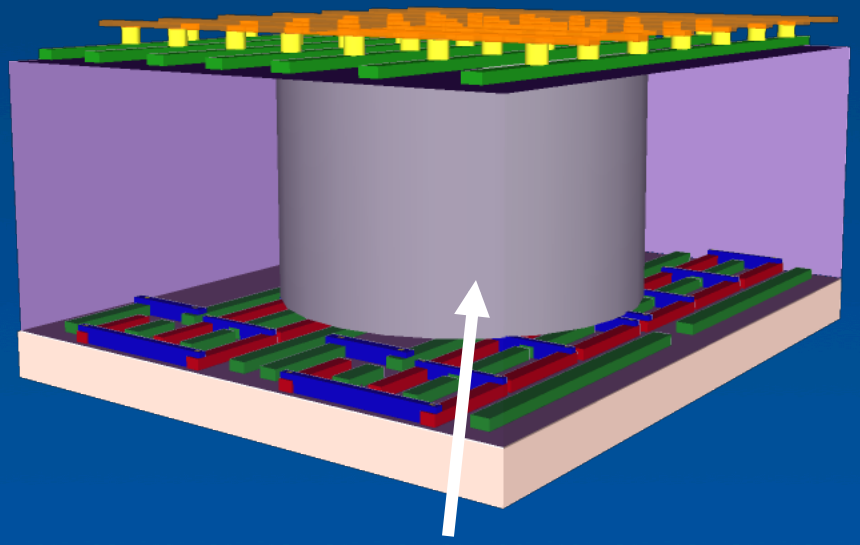
10X EDP, BUT…

How can we do better ?

3D Integration

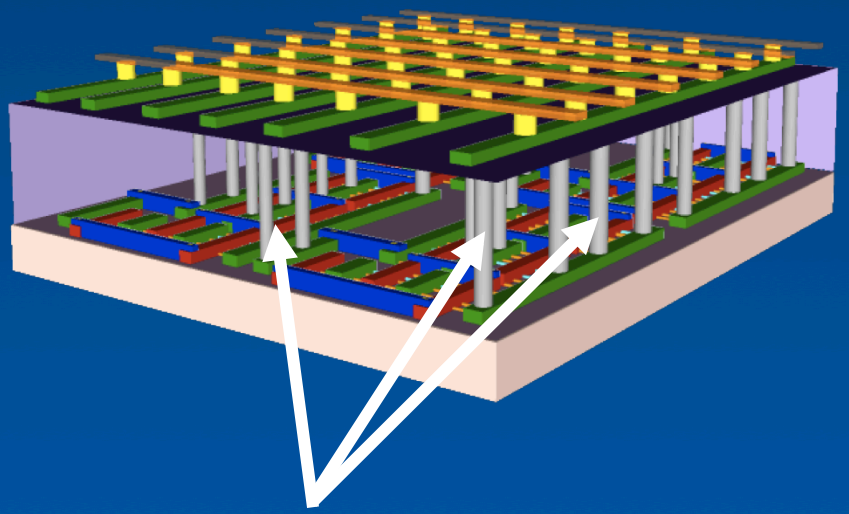
- Massive ILV density >> TSV density

TSV (chip stacking)



Through silicon via (TSV)

Dense, e.g., monolithic



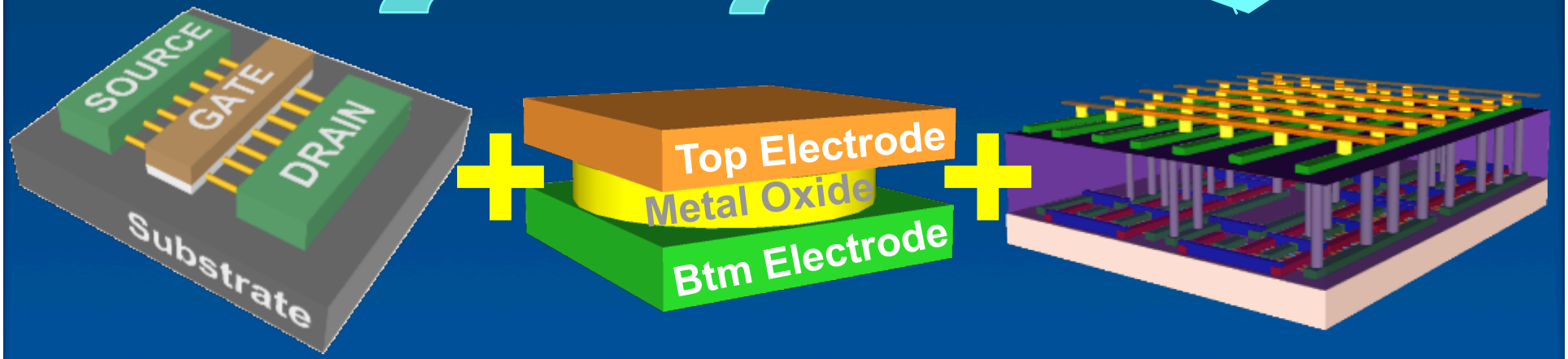
Nano-scale inter-layer vias (ILVs)

Realizing Monolithic 3D

- Low-temperature fabrication: **< 400 °C**

Device + Architecture Benefits

Naturally enabled



Emerging logic

Emerging memory

Monolithic 3D integration

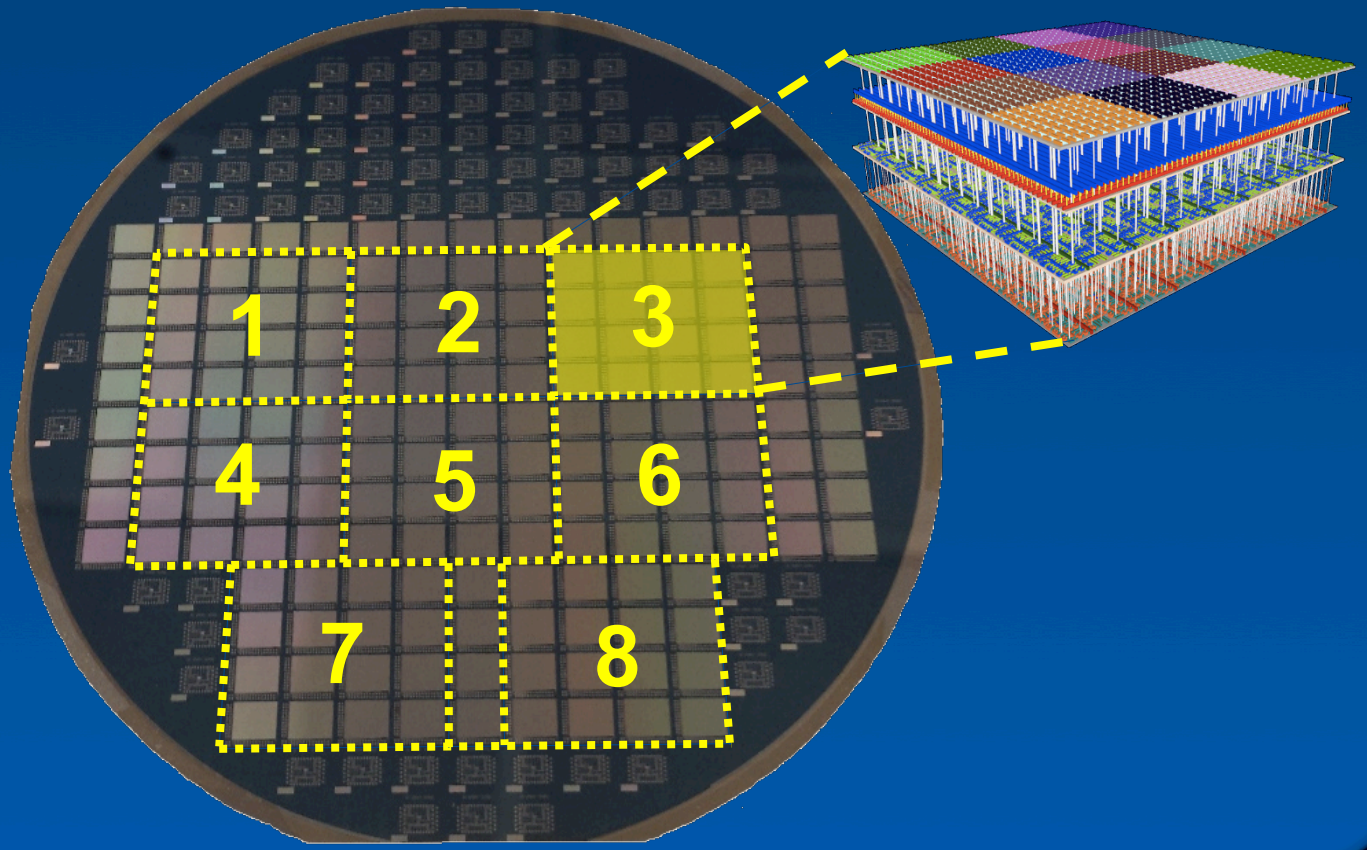
[Wei IEDM 13, Shulaker VLSI Tech 14]

3D NanoSystem



M. Shulaker

Wafer-scale design + fabrication



N3XT Framework



M. Aly

- Heterogeneous nanotechnologies
- Architecture design space
- Physical design
- Integrated thermal analysis
- Yield, reliability

Sweet Spot: Abundant-Data Apps.

IBM graph analytics

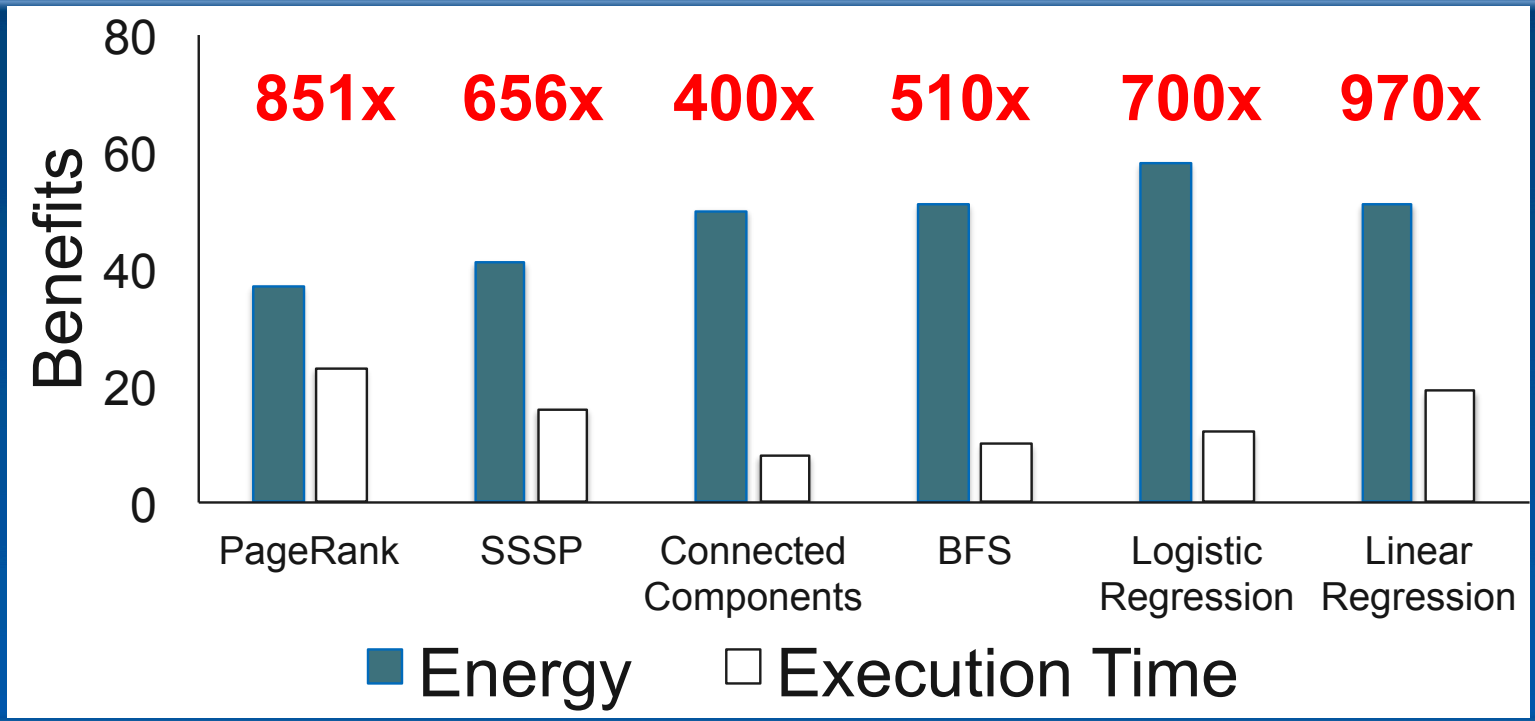
DeepDive

BigDataBench

TensorFlow

intel

~1,000X benefits, existing software



Sweet Spot: Abundant-Data Apps.

IBM graph analytics

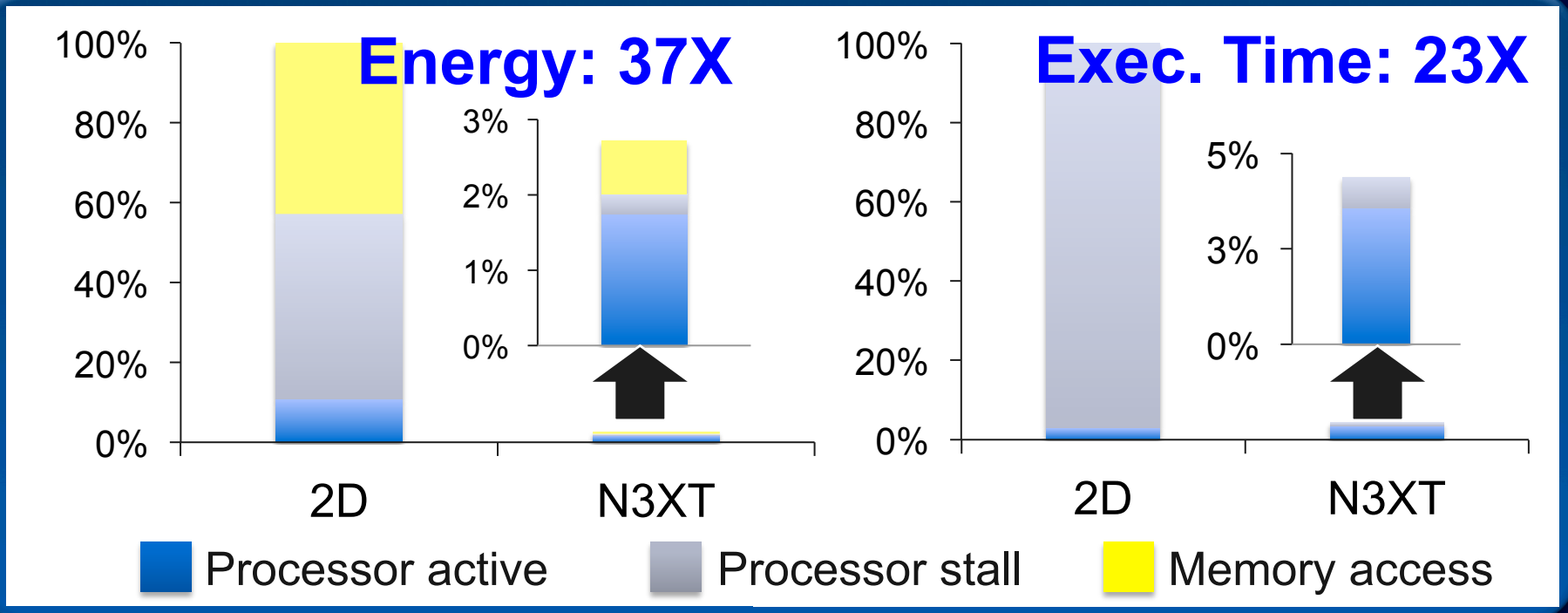
DeepDive

BigDataBench

TensorFlow

intel

851X benefits (vs. 4X: silicon 2.5D)



PageRank app.

More Opportunities

Accelerators

Neuro-inspired

Technology innovations

Students, Sponsors & Collaborators

C2S2 Center for Circuit & System Solutions

Bridging The Gap DARPA Powered by Ideas

FENA

GSRC

IBM

imec

leti ceatech

NEEDS needs.nanoHUB.org

NSF

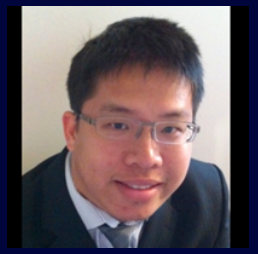
SONIC

SRC

STARnet

SUPERCELL

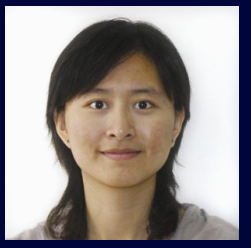
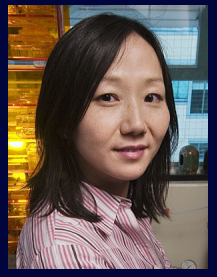
















Conclusion

- **Nanosystems today**
- **Game ON, to the** 

era
- ***N3XT 1,000X***
  - Compute + memory + sensing
  - Densely interwoven