

ADVANCED 3D TECHNOLOGIES FOR INNOVATIVE 3D ARCHITECTURE

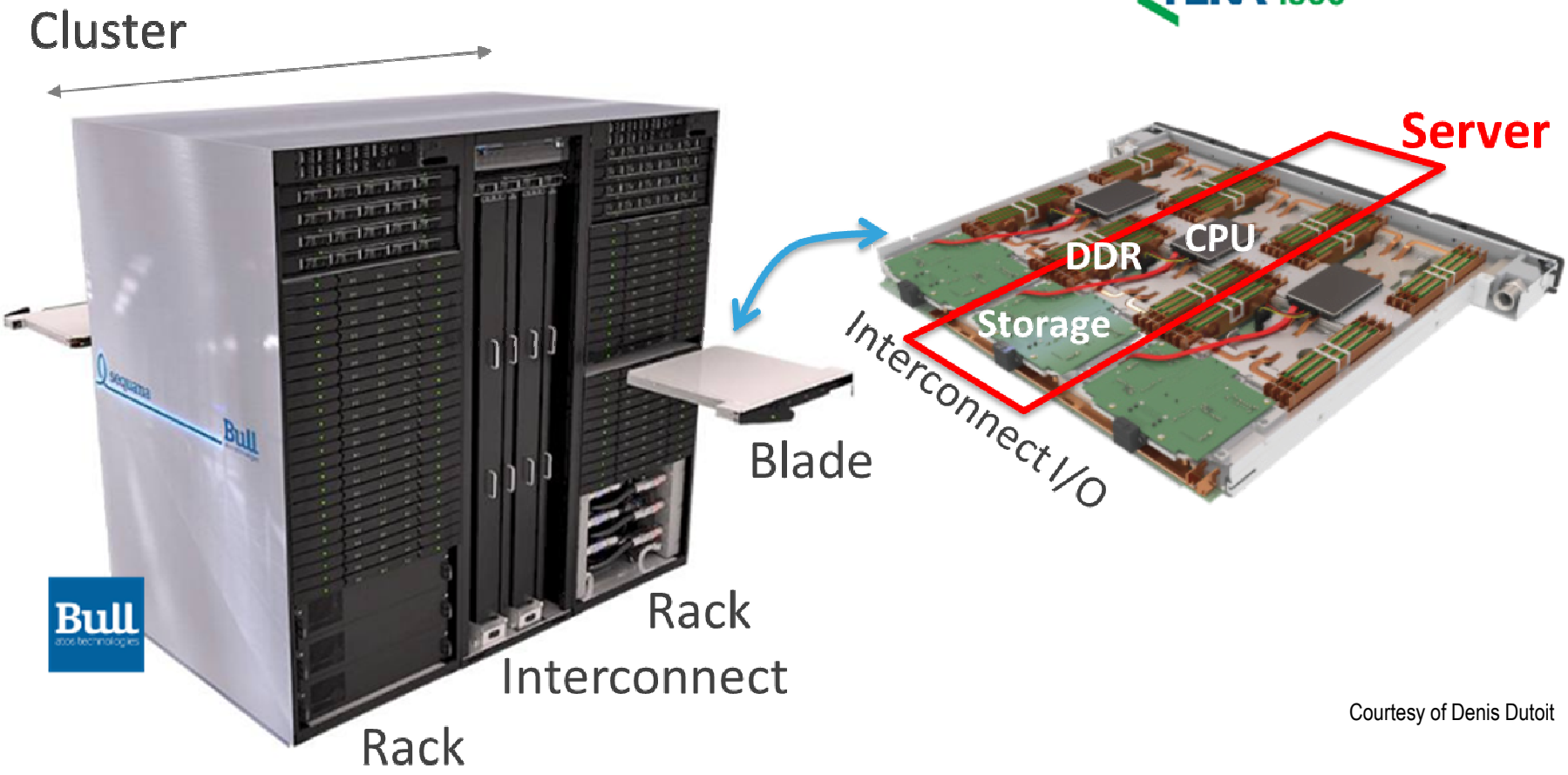
D43D | Séverine Chéramy | June, 27th, 2017

AGENDA

1. Top challenges for Computing
2. How 3D can help?
3. Our options towards fine pitch 3D technologies
4. Summary

A SUPERCOMPUTER TODAY

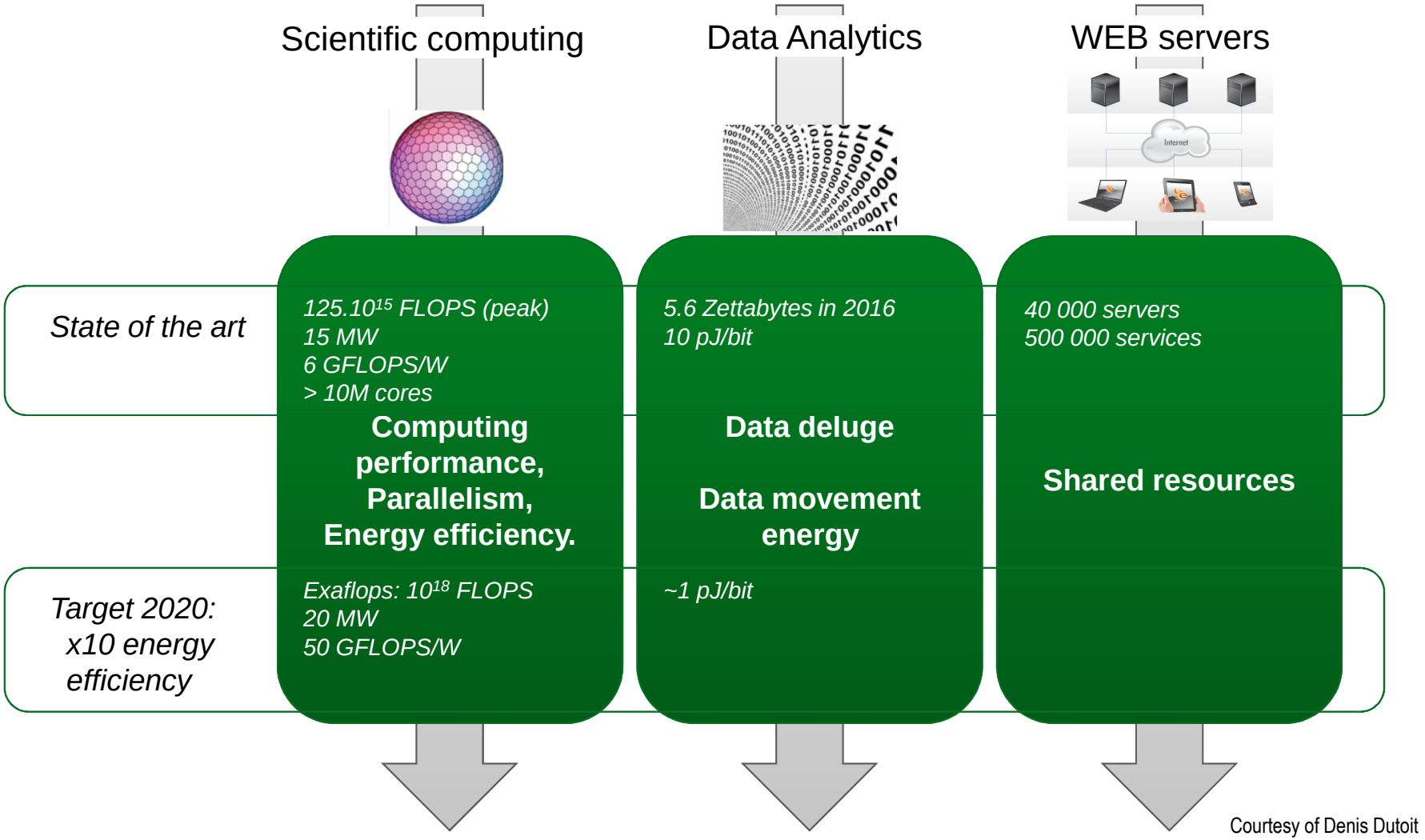




Courtesy of Denis Dutoit

See D. Dutoit presentation at 11:00

APPLICATION LANDSCAPE AND ASSOCIATED CHALLENGES



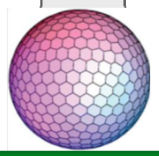
GIGA	TERA	PETA	EXA	ZETTA
10^9	10^{12}	10^{15}	10^{18}	10^{21}

SERVER SYSTEM ARCHITECTURE

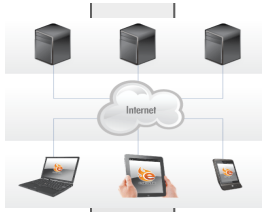
Scientific computing

Data Analytics

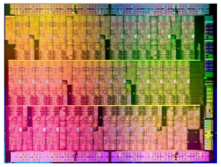
WEB servers



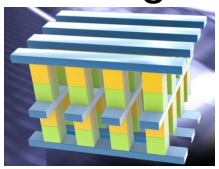




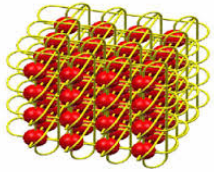
Processor



Memory / Storage



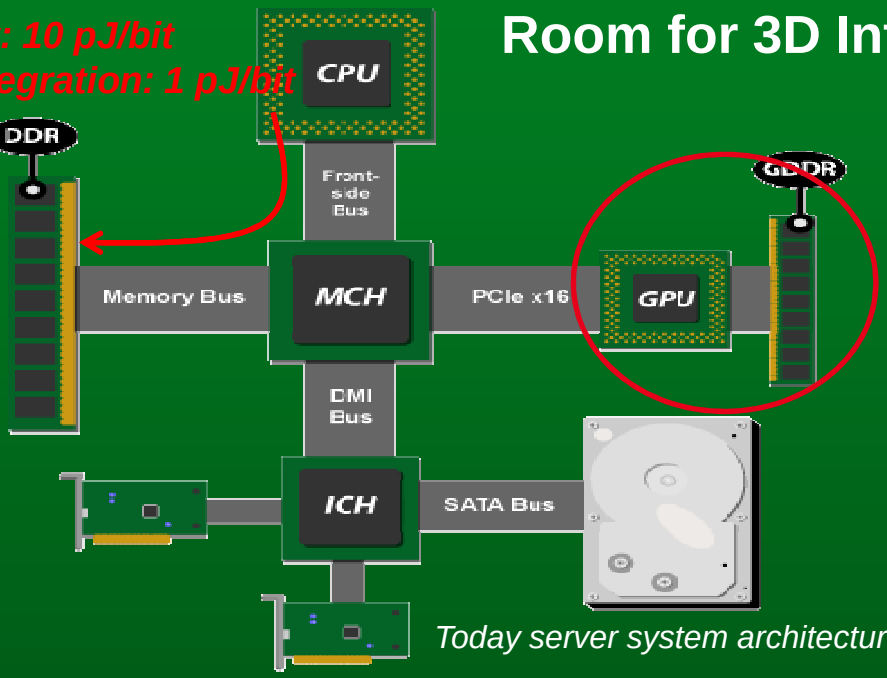
Interconnect



Today: 10 pJ/bit
3D integration: 1 pJ/bit

Room for 3D Integration ?

YES

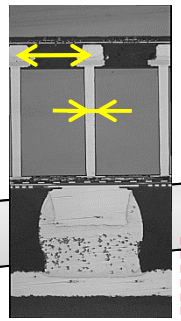


Today server system architecture

Courtesy of Denis Dutoit

3D INTEGRATION LANDSCAPE AT CEA-LETI

3D Contact :
Die-to-die through-Silicon-Via (TSV)

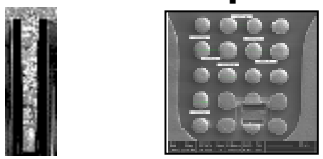


Pitch
Diameter

3D Density of Integration ↗

See P. Battude presentation at 14:00

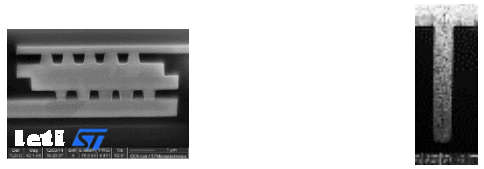
TSV + µBump
Diameter: 10 µm
Pitch : 20 µm



~10^3 3D Contacts / mm²

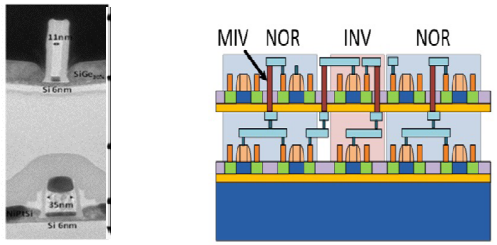
Cu-Cu
Diameter : 1.7 µm
Pitch : 3.4 µm

HD-TSV
Diameter : 0.85 µm
Pitch : 1.75 µm



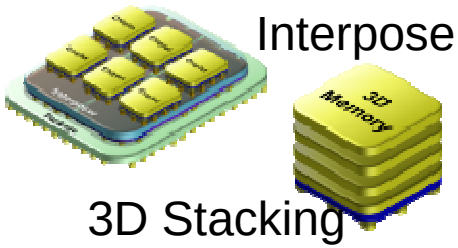
~10^5 3D Contacts / mm²

Monolithic 3D (CoolCube™)
Diameter: 0.05 µm
Pitch : 0.11 µm



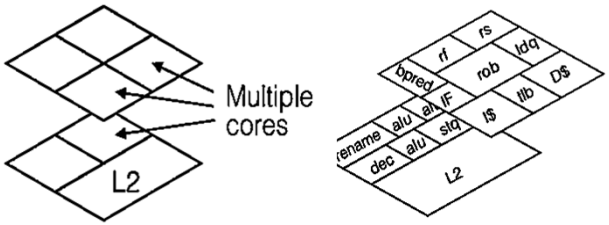
10^8 3D Contacts / mm²

SoC Level Integration

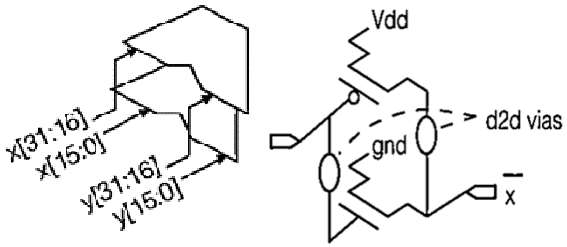


Courtesy of Denis Dutoit

Core-/Block-Level Integration

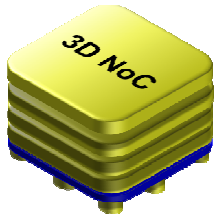


Gate-/Transistor- Level Integration



Core of this prezentation

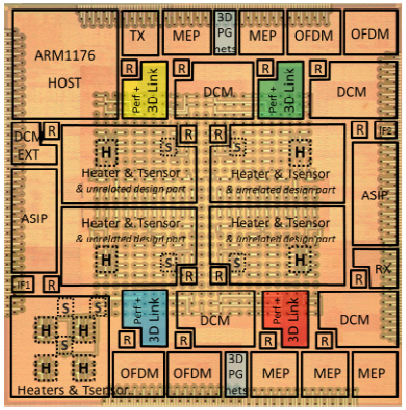
How 3D can help?



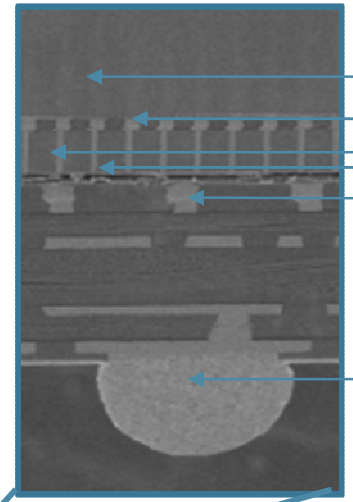
Extending Network-on-Chip to the third dimension

- **Die-to-die energy efficiency :**
  - Die on package on board: 10 pJ/b
  - 3D Stacking with 3D NoC: 0.66 pJ/b

Cmos Process	65nm STMicroelectronics, Low-Power, Multi-VT
3D Tech.	TSV middle (AR 1:8) CEA-LETI µ-bumps, 50µm x 40µm pitch Face2Back stacking, Die2Die assembly
Package	12x12x1.2 flip-chip package, 4 layers substrate
Complexity	1.63 Mbyte SRAM, 228 Mtransistors, 276 IOs

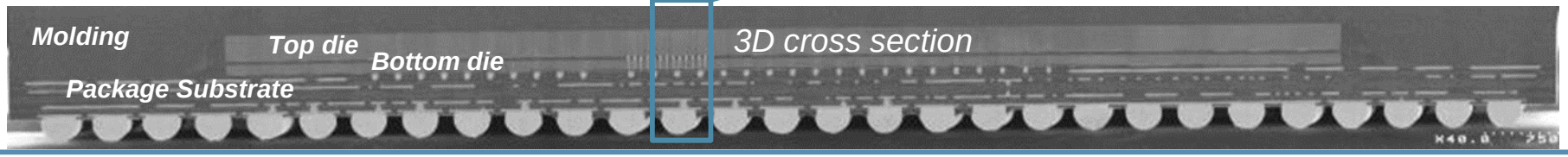


Bottom die photo (72 mm²)



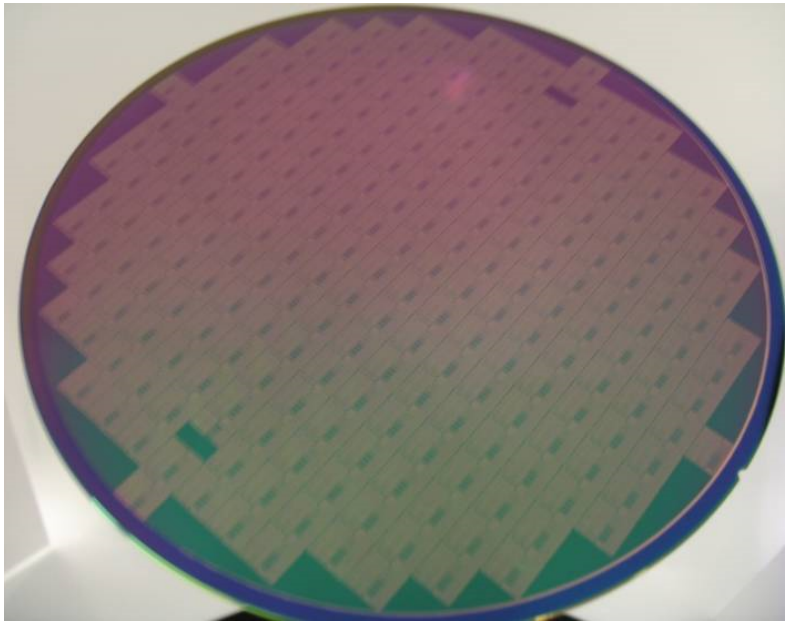
BEOL top die
µ-bump
TSV *AR 1:8*
BEOL bottom die
C4 bump
Package ball

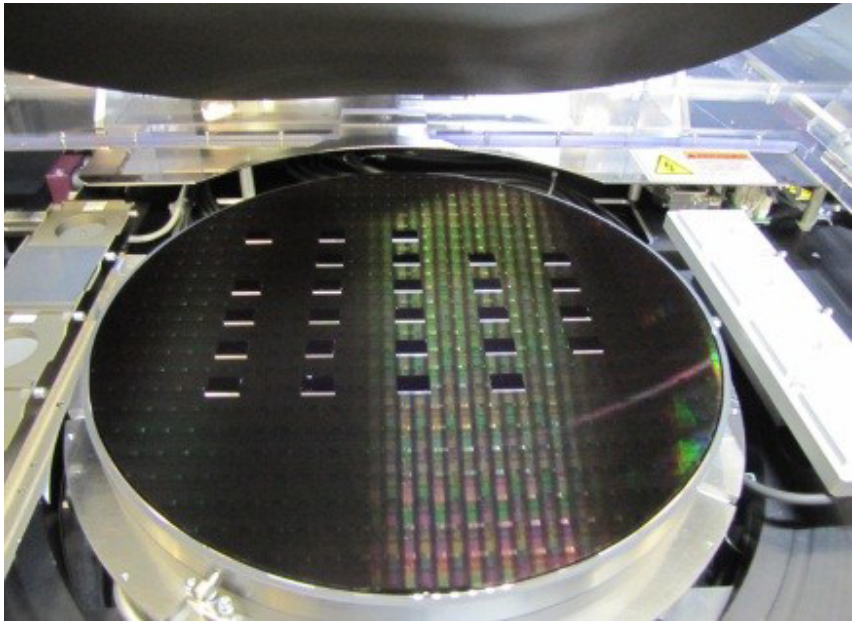
3D TSV pitch, 40µmx40µm



P. Vivet, et al, "A 4x4x2 Homogeneous Scalable 3D Network-on-Chip Circuit with 326 MFlit/s 0.66 pJ/bit Robust and Fault Tolerant Asynchronous 3D links", IEEE Journal of Solid-State Circuits,

3D FINE PITCH TECHNOLOGIES FOR HIGH PERFORMANCES 3D SYSTEMS





Wafer-to-wafer

Objectives:

- Ultra fine pitch
- Throughput

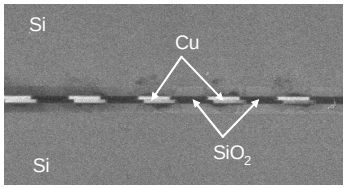
Chip-to-wafer

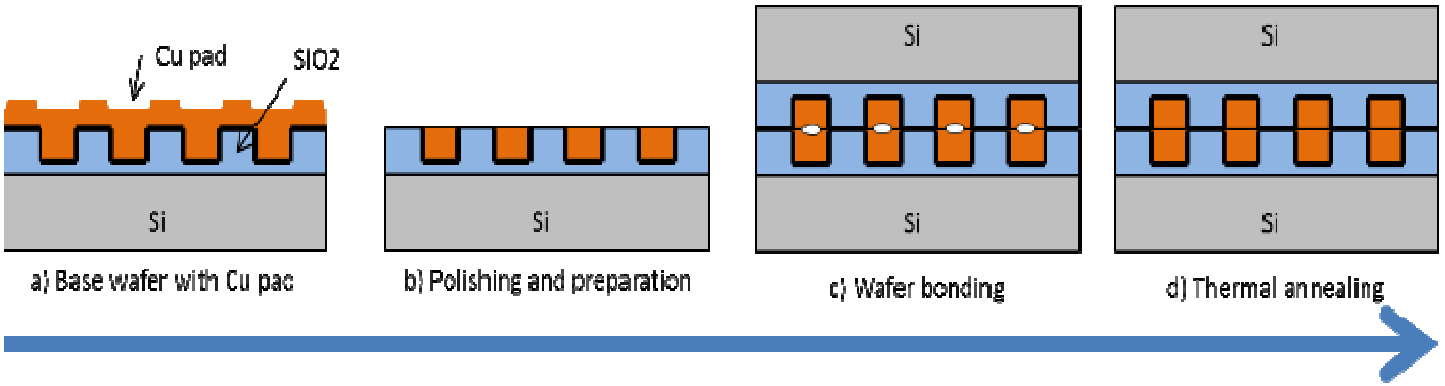
Objectives:

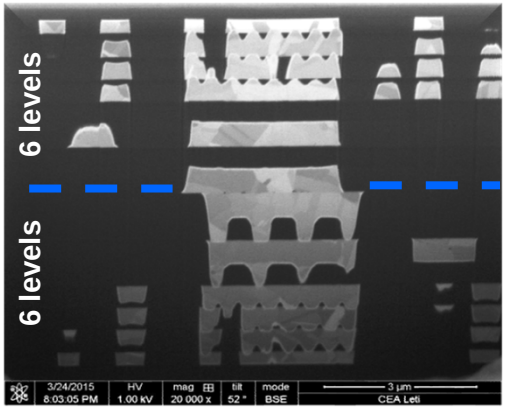
- Heterogeneity
- Multi dies Stacking
- Low yield devices stacking

CU/CU BONDING : PRINCIPLE

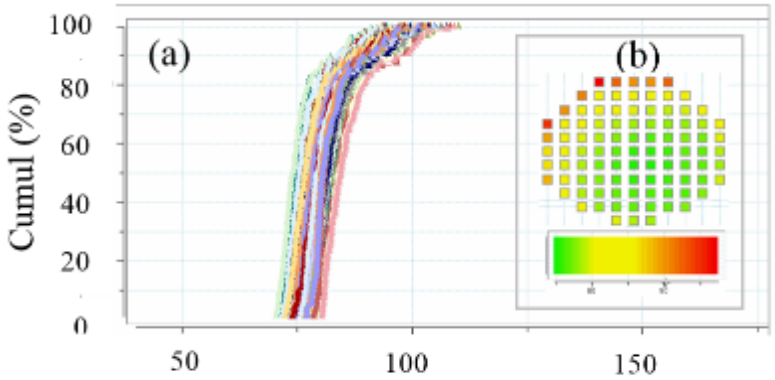
Maximize chip-to-chip connection density







- ✓ No adhesive (underfill), No pressure, Room T° process: high throughput
- ✓ From 200°C to 400°C annealing
- ✓ Pitch : **5-10µm (2015) => 1-2µm (2017)**

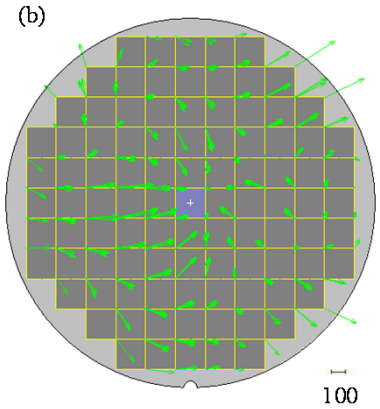


L. Benaissa et al, EPTC 2015
S. Lhostis et al, ECTC2016

Demonstration done on Wafer to Wafer

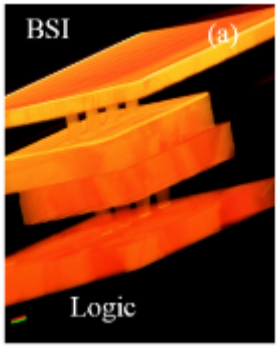
DIRECT BONDING WTW: SOME RESULTS

Alignment

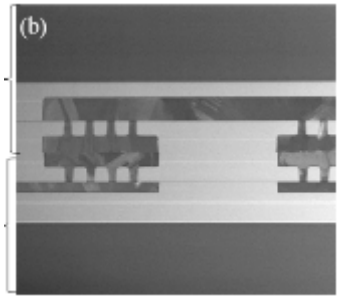


Max overlay @ 250nm proven on EVG NT40 tool

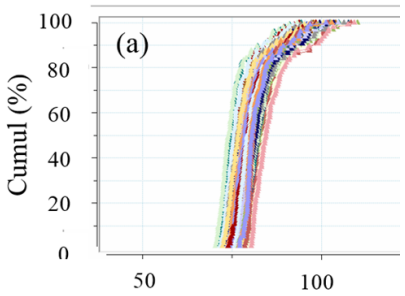
Pad integrity



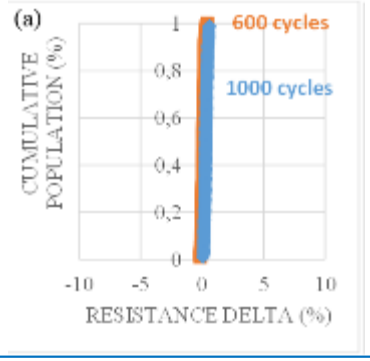
Pad quality : no voids @ Cu-Cu and Ox-ox



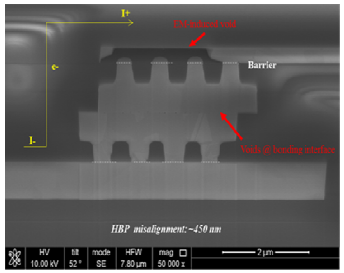
Electrical data



30K daisy chain resistance and Thermal cycling: high repeatibility & stability



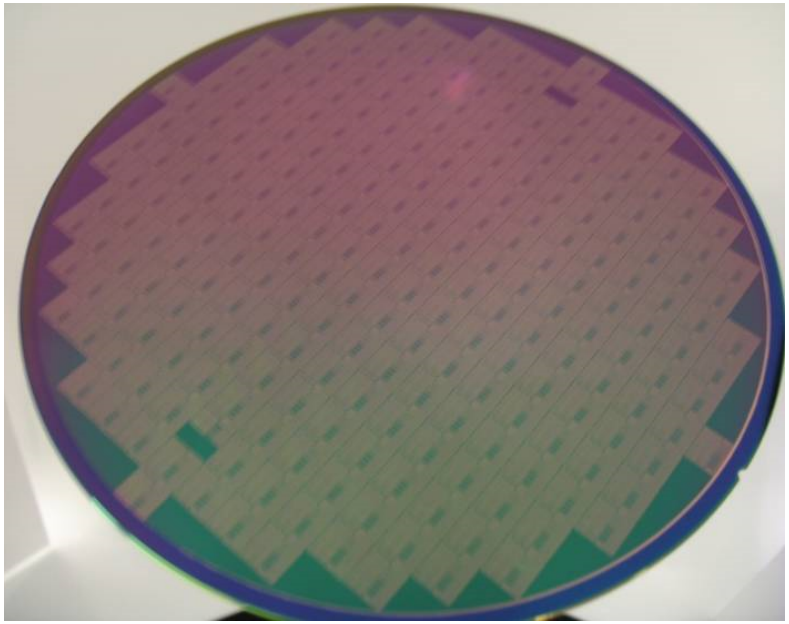
Reliability - EM

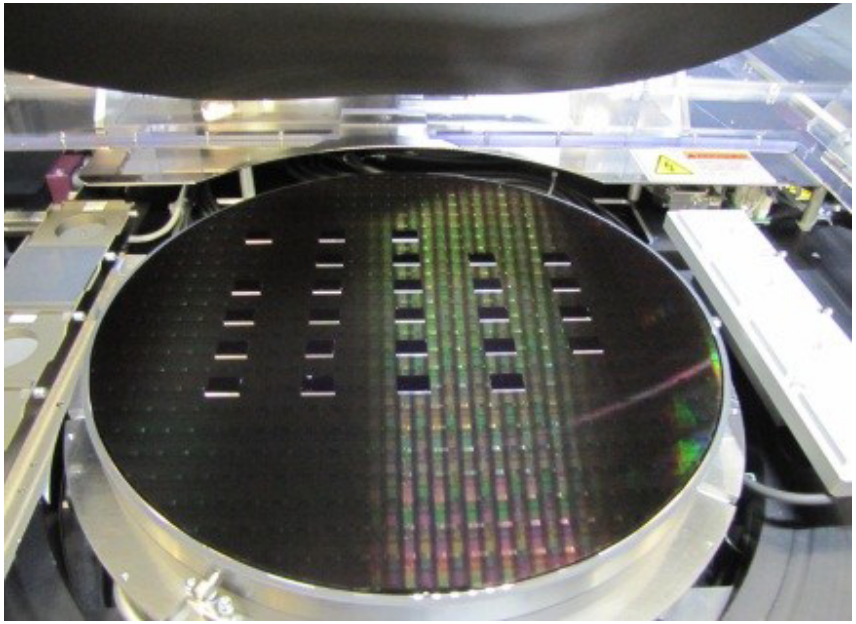


Weakest path is BEoL – no specific failure induced by hybrid bonding

Courtesy of ST, ECTC 2016

HYBRID BONDING: A CHIP-TO-CHIP TECHNO ENABLER FOR HIGH PERFORMANCES





Wafer-to-wafer

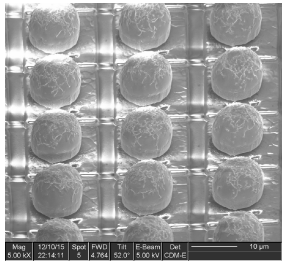
Objectives:
- Ultra fine pitch
- Throughput

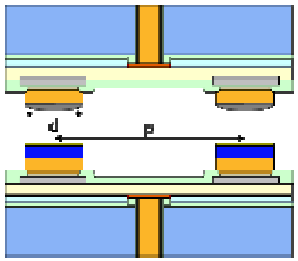
Chip-to-wafer

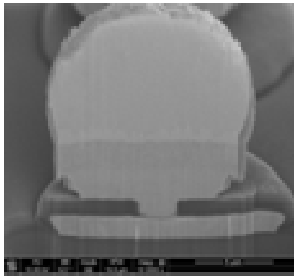
Objectives:
- Heterogeneity
- Multi dies Stacking
- Low yield devices stacking

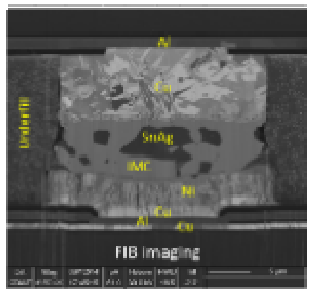
COPPER PILLAR FINE PITCH 20µm

- Copper pillar
  - Pitch 20µm
  - Pre-Applied Underfill
  - Thermo-compression
  - Die to Wafer

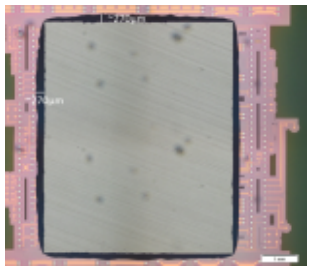


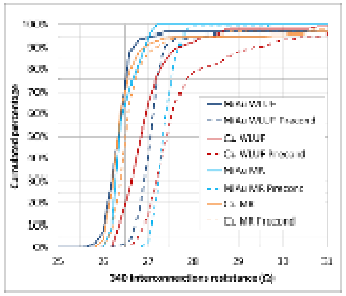


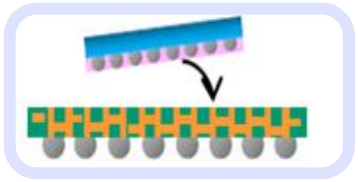




Copper pillar Φ 10µm

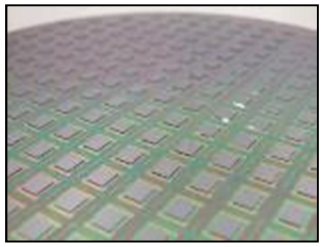






Pre-applied Underfill NCP or Film

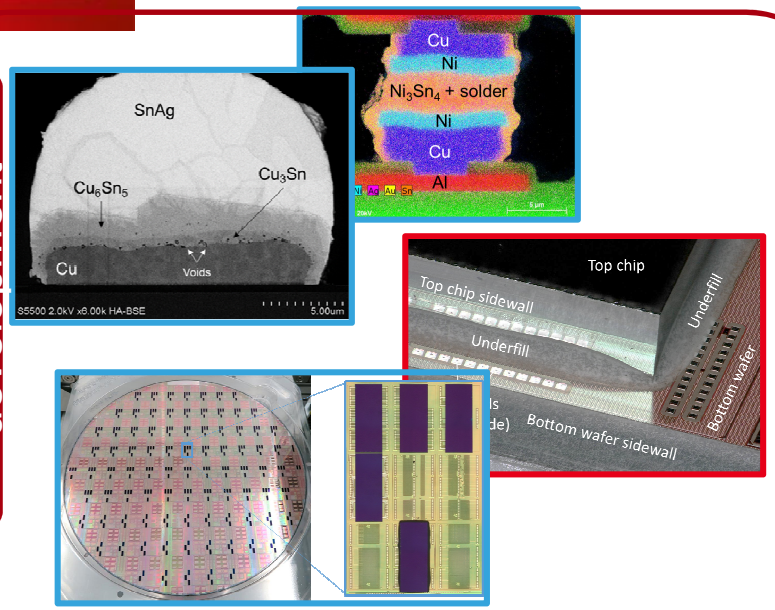
X2 density
X2 connection top/bottom with a similar R



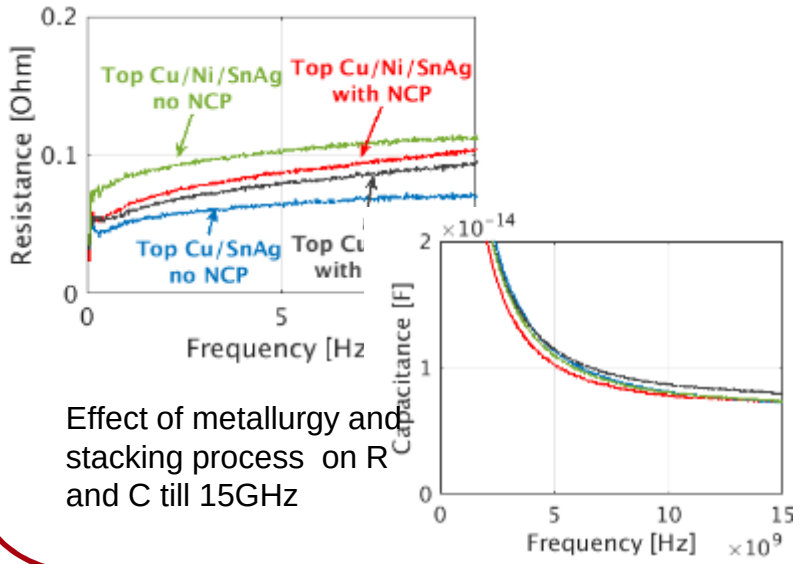
Die to Wafer

Copper pillar fine pitch 20µm: Performance assessment

Process development

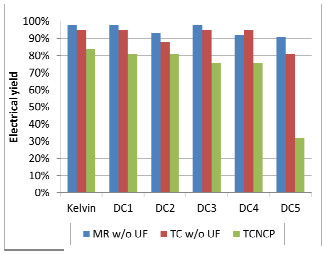


RF characterization



Effect of metallurgy and stacking process on R and C till 15GHz

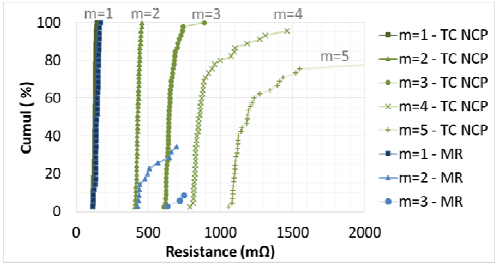
Electrical perf (DC)



Daisy chain resistance and yield

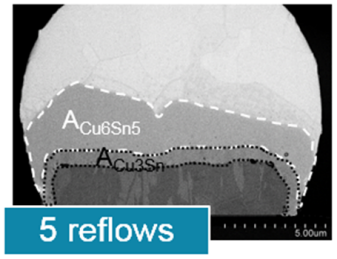
Stacking process impact

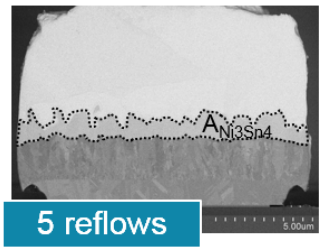
Effect of misalignment on resistance

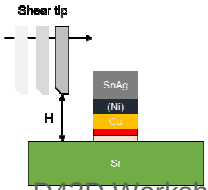


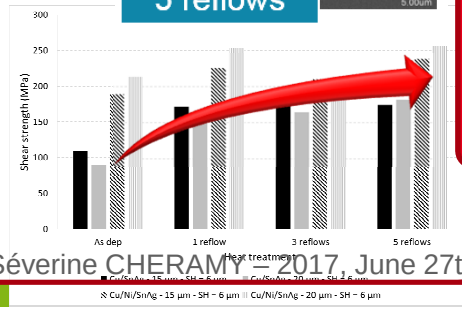
Ageing

Metallurgy and shear strenght relationship

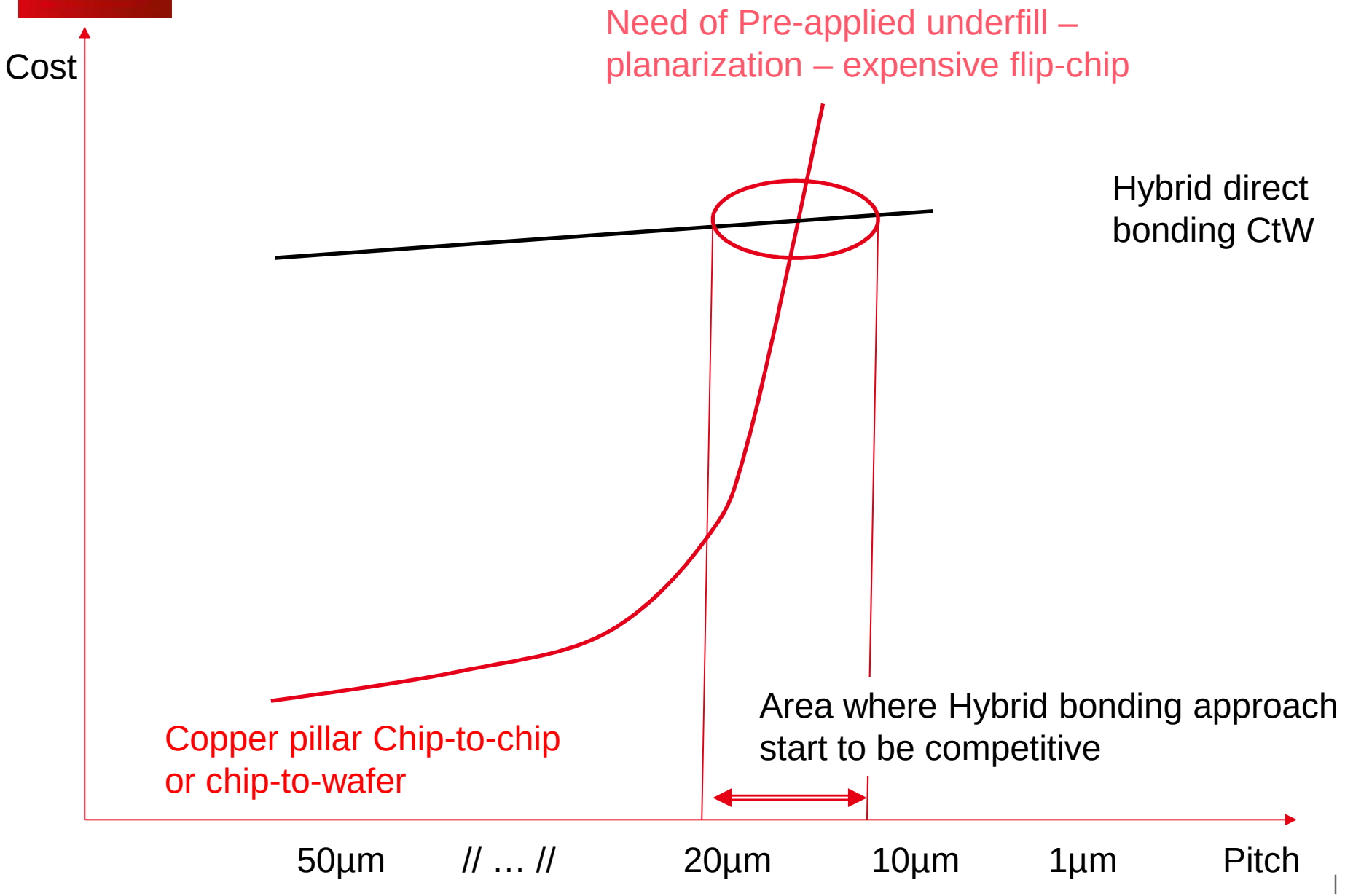








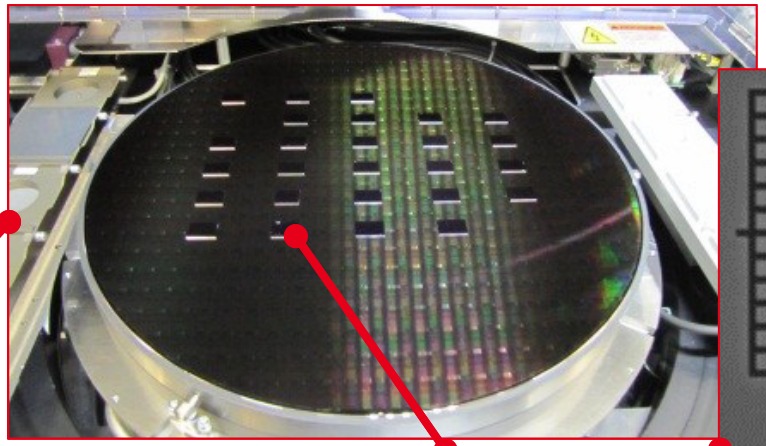
FINE PITCH COMPARISON PROCESS ONLY - TREND

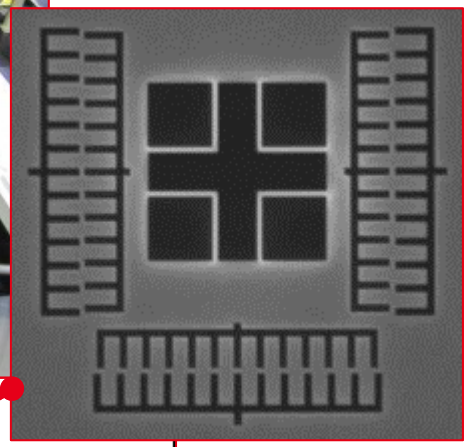


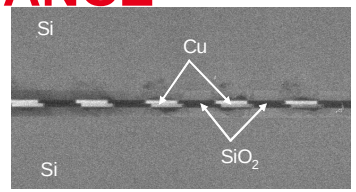
DIRECT BONDING CTW: ALIGNMENT PERFORMANCE

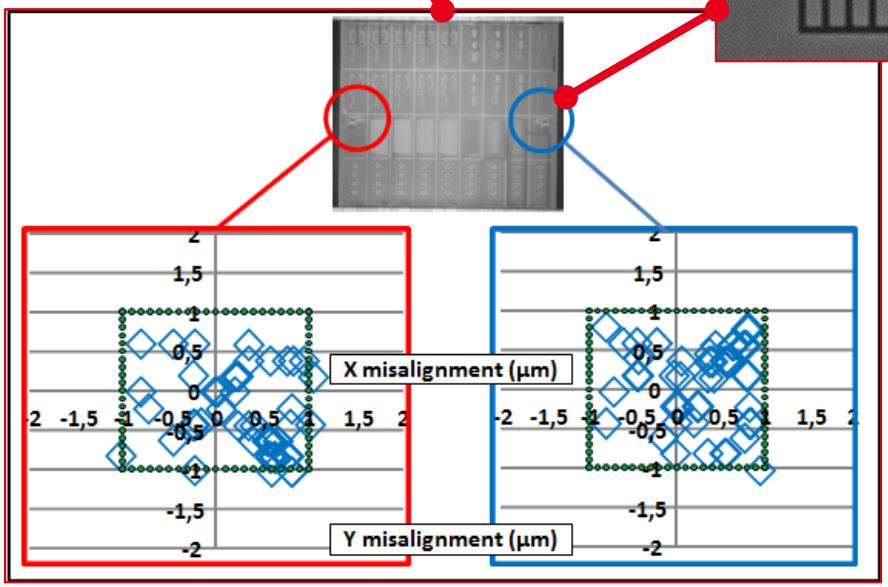
FC300 bonding machine with ± 1µm post-bonding accuracy





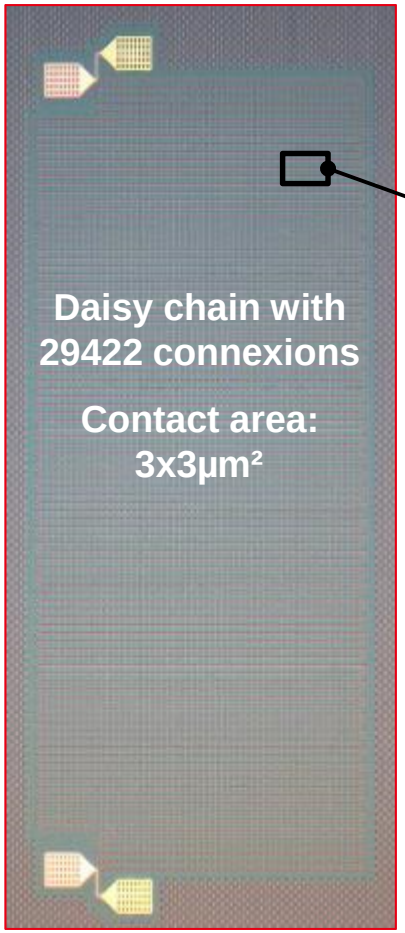


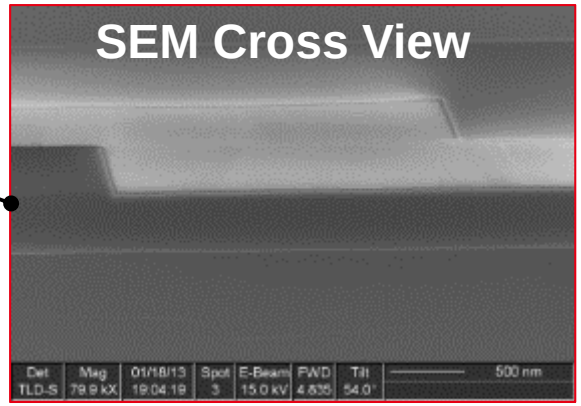




Y. Beillard, 3DIC 2013

DIRECT BONDING CTW: ELECTRICAL DATA





300mm CTW process is compatible with high interconnection density

Theoretical Res.	**2265.5Ω**
Wafer to Wafer	
Global resistance	**2340Ω**
Chip to Wafer	
Global resistance	**2297Ω**

Y. Beillard, 3DIC 2013

HIGH PRECISION CHIP TO WAFER STACKING

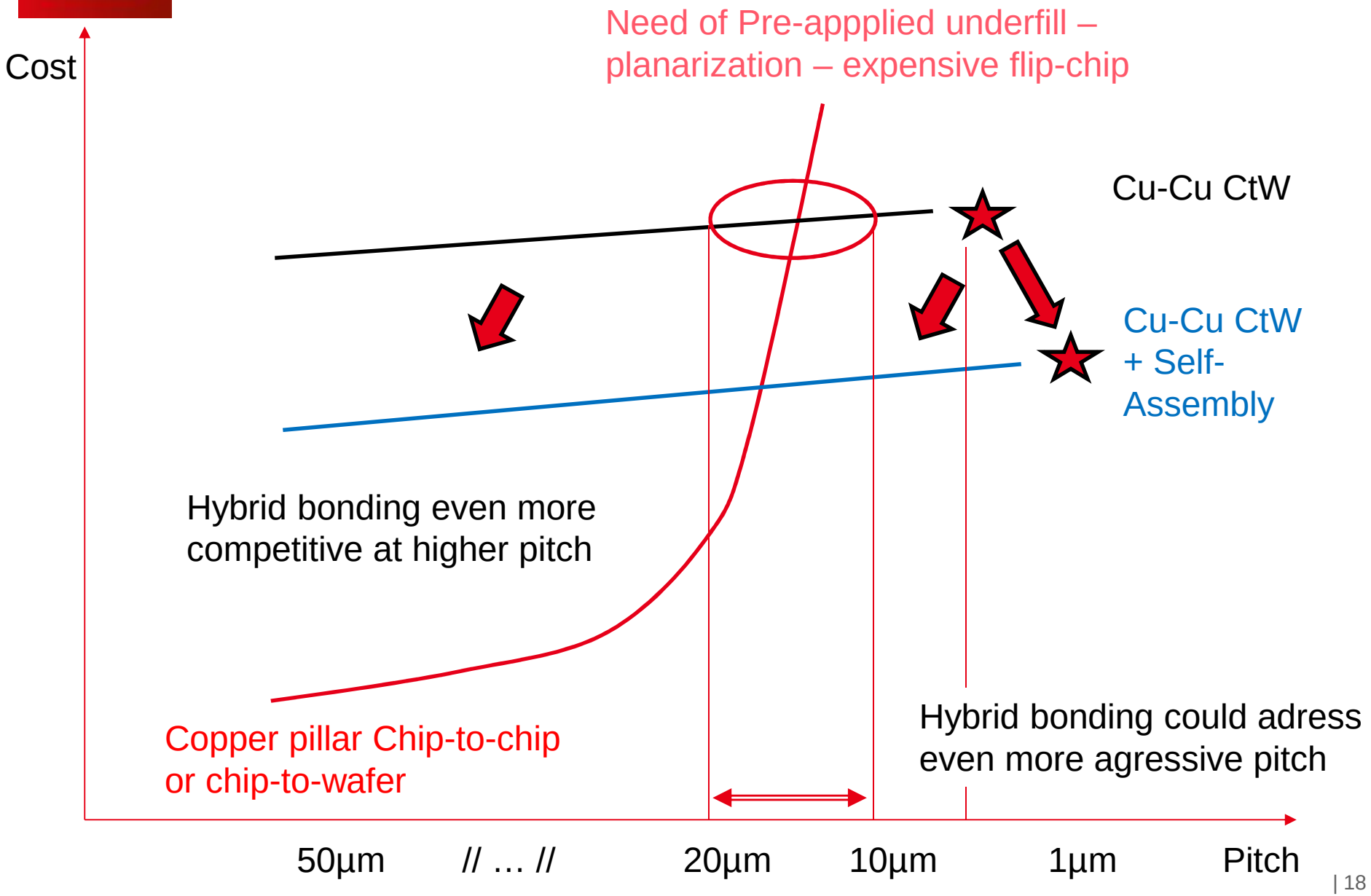
FC300 bonding machine with ± 1µm post-bonding accuracy
Compatible with Cu-Cu process requirement



New equipment SET FC1
Combining similar accuracy
&
Higher throughput

Additionnal work to be published at Imaps IWLPC 2017

FINE PITCH COMPARISON PROCESS ONLY - TREND

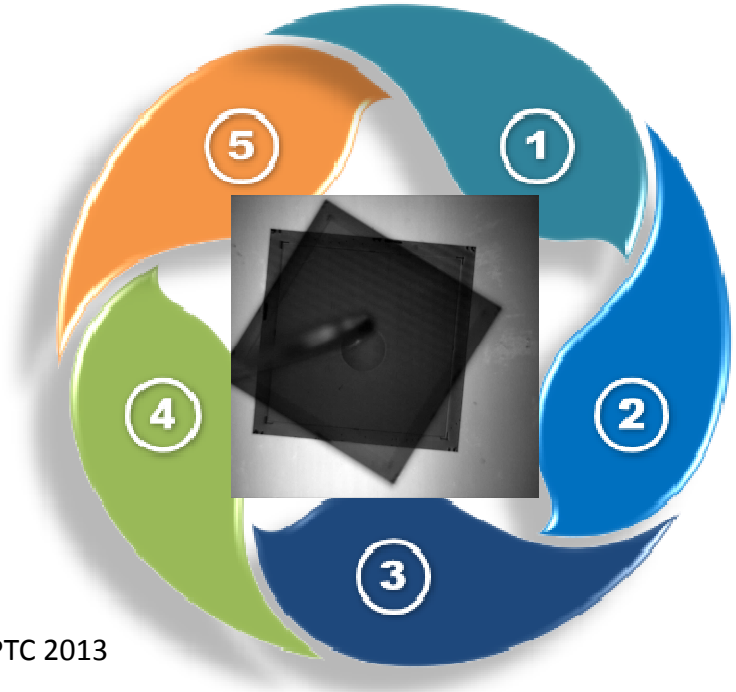


SELF-ASSEMBLY AS FINE-PITCH ENABLER WITH CTW APPROACH

PRINCIPLE OF SELF-ASSEMBLY USING CAPILLARY FORCE

Phase 1 : Self-alignment

- Leti's choice: capillary driven alignment
- Minimization of surface tension with capillary force



S. Mermoz, EPTC 2013

Phase 2 : Hybridation

- Leti's choice : Direct bonding

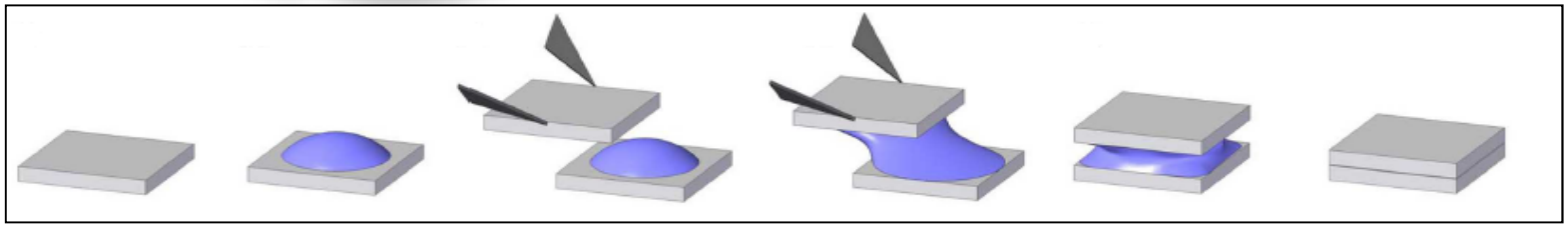
1 – LIQUID DEPOSITION ON SUBSTRATE OR DIE

2 – ROUGH PRE-POSITIONNING USING MECHANICAL TOOL

3 – REMOVAL OF THE TOP DIE

4 – SPONTANEOUS ALIGNMENT THANKS TO CAPILLARY FORCE

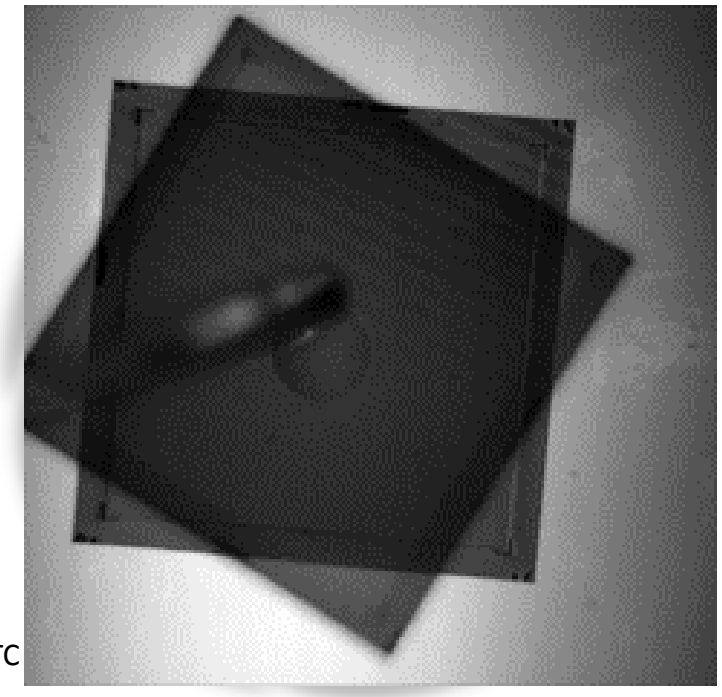
5 – LIQUID EVAPORATION AND HYBRIDATION



SELF-ASSEMBLY AS FINE-PITCH ENABLER WITH CTW APPROACH

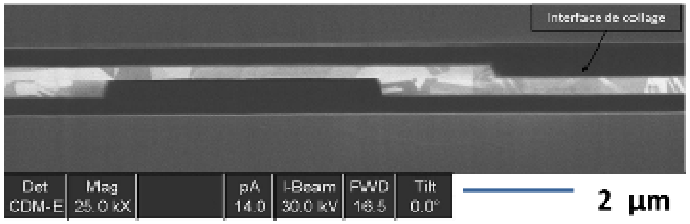
PRINCIPLE OF SELF-ASSEMBLY USING CAPILLARY FORCE

Phase 1 : Self-alignment



S. Mermoz, EPTC

Phase 2 : Hybridation



Hybridation process	C2W (S-A)
Contact area (µm²)	340 x 5
Experimental Res. (Ω)	5,1
Theoretical Res. (Ω)	5,09
Variation (%)	**+ 0,19**

Very good matching

High Throughput

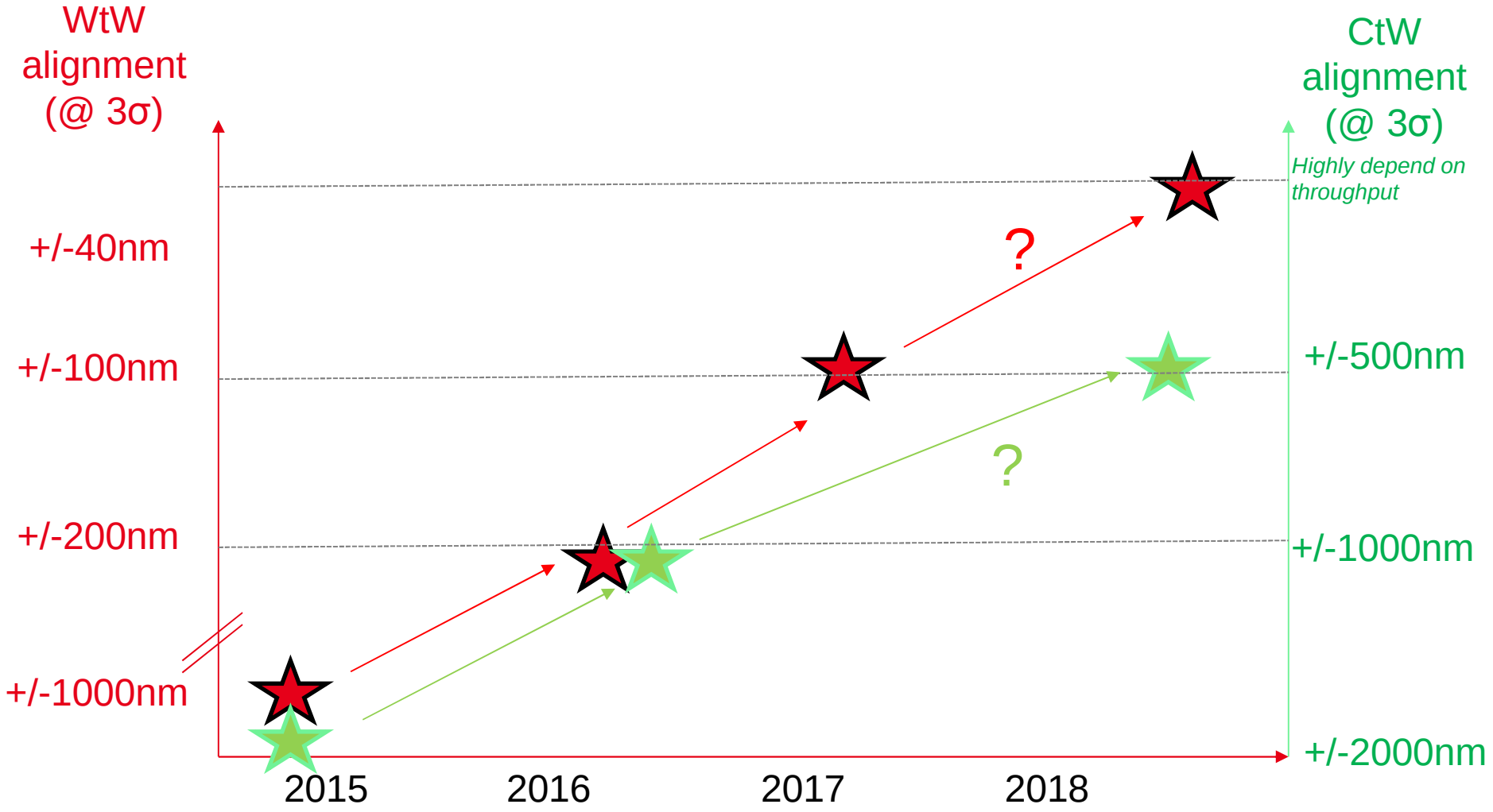
Collective Bonding

High Alignment Accuracy (< 1 µm)

Direct bonding Compatibility

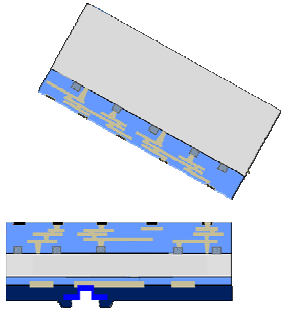
ROADMAP FOR ALIGNMENT POSSIBILITY AT CEA-LETI (EQUIPMENT CAPABILITY)

…Based on closed partnership with equipment suppliers

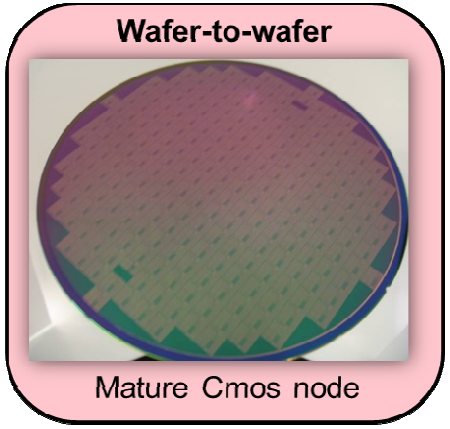


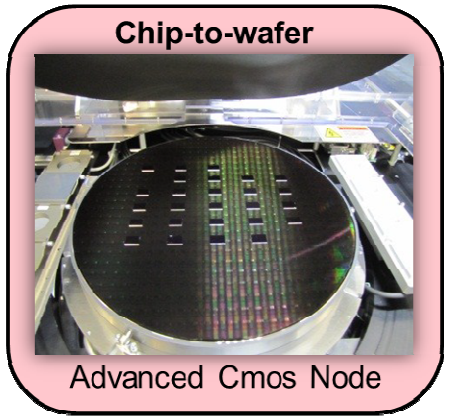
…AND 3RD LAYER

2-layers…

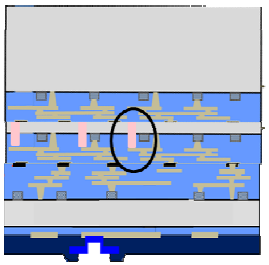


Hybrid bonding ultra fine pitch



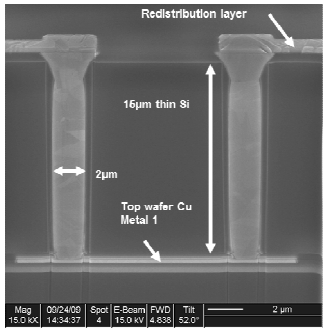


….And more

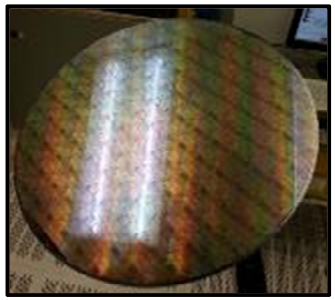


TSV high density Face-To-Back

2µm diameter TSV, 15µm thin Si



Ultra silicon thinning on a stop layer



Investigation on TSV impact on 65nm CMOS devices and circuits
H. Chaabouni, M. Rousseau, P. Leduc et al., IEDM 2010

3D STACKING ALSO ADDRESSING IMAGE SENSOR CHALLENGES …

PERFORMANCES

High bandwidth between dies (high speed)

Optimized pixel array & logic independently

Design flexibility

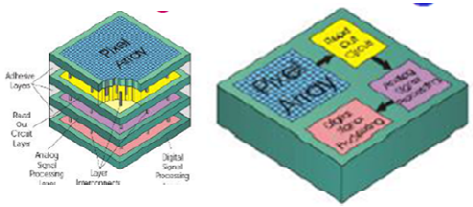
Added logic functions

ADVANCED IMAGING

Smaller X-Y size

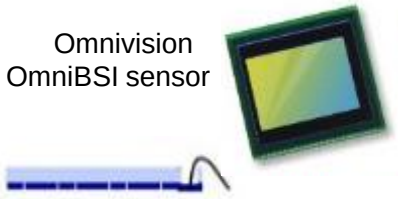
COST
Production & maintenance

"SIZE, WEIGHT & POWER"



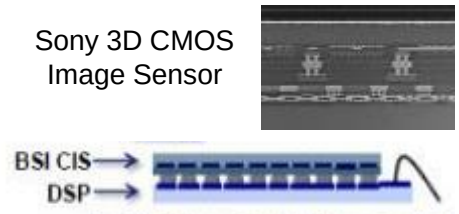
Reduced interconnect delay and energy consumption (low power)

Omnivision
OmniBSI sensor



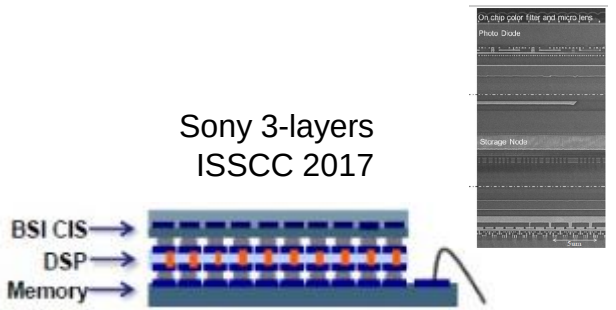
Monolithic BSI

Sony 3D CMOS
Image Sensor



Dual-stack 3D BSI

Sony 3-layers
ISSCC 2017



Three-stack 3D BSI

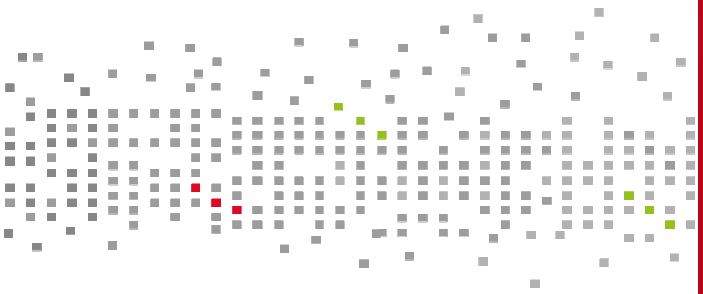
Hybrid bonder as enabler for compact, low efficiency and high performance imager

SUMMARY

- **Yes, 3D can help the computing and imaging roadmap, and offer lattitude to designers!**
- **Early Demonstrations done!**
- **LETI is working towards several disruptive 3D stack options devoted to fine alignement and fine pitches**
  - Cu/Cu Hybrid bonding to achieve 1µm pitch on Wafer to Wafer approaches
  - Die to Wafer and high throughputs
- **Techno-To-Design remaining challenges to be commonly adressed**
  - Thermal management
  - Die-to-die coupling
  - 3D dedicated CAD Tool

Part of this work was partly funded thanks to the French national program "Programme d'Investissements d'Avenir, IRT Nanoelec" ANR-10-AIRT-05.

Thank you for your attention



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