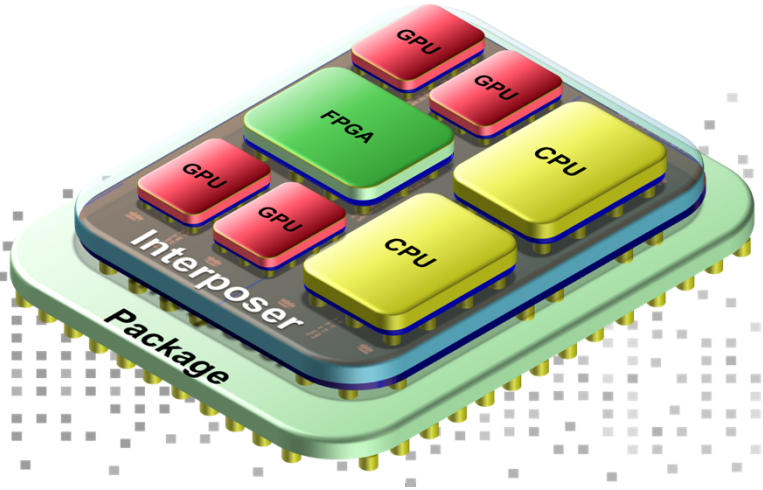
Session 4:
3D for High Performance Computing



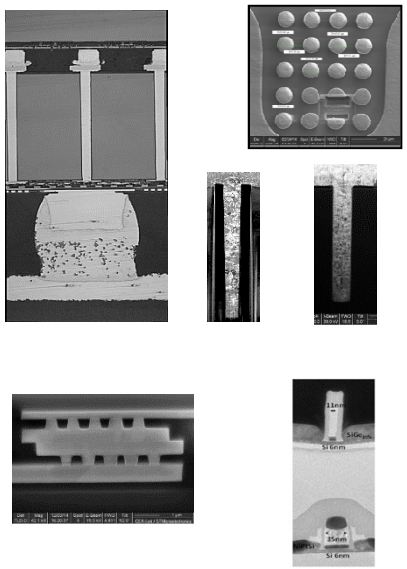
EMERGING ARCHITECTURES FOR COMPUTING WITH 3D SILICON INTEGRATION

Denis DUTOIT – CEA-Leti

D43D Workshop, Grenoble, June 27th 2017

EMERGING ARCHITECTURES FOR COMPUTING WITH 3D INTEGRATION

3D Integration



How 3D will contribute to scale for higher performances

More parallelism
More cores
More memory per core
More data bandwidth
Less data latency

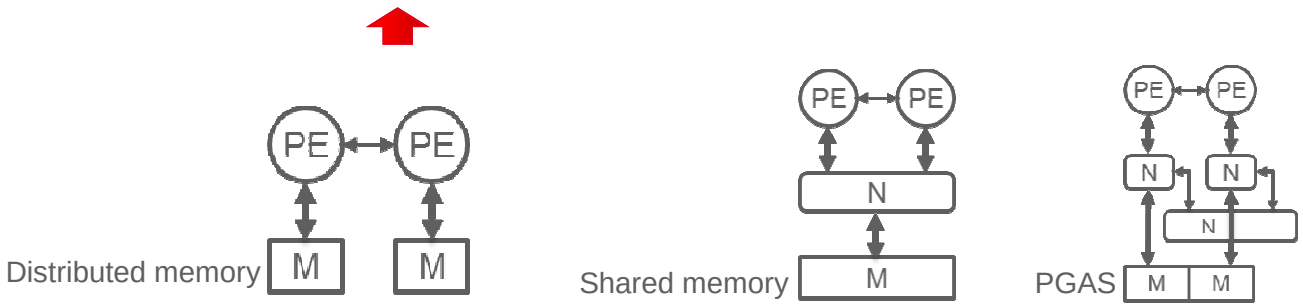
within limits ?

Power
Cost

Computing applications



Computing model



OUTLINE

How 3D will contribute to scale for higher performances

More parallelism
More cores
More memory per core
More data bandwidth
Less data latency

1
Computing application landscape

2
3D integration @ Leti

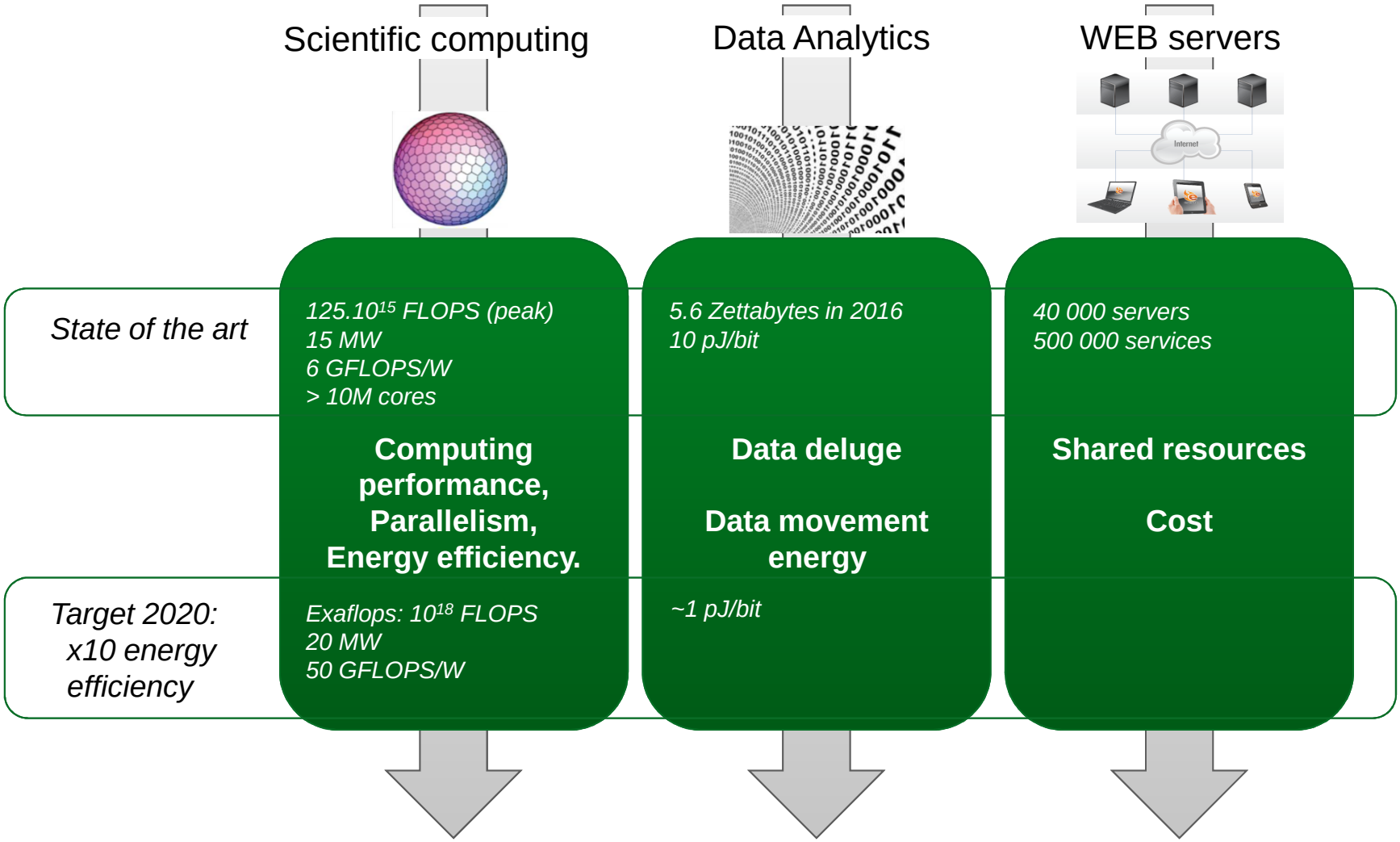
within limits ?

Power
Cost

3
3D integration leverages new computing architectures:

- **Server on a chip with System-in-Package**
- **Partitioned Global Address Space with active interposer**
- **Shared memory with active interposer and photonic interposer**

APPLICATION LANDSCAPE AND ASSOCIATED CHALLENGES



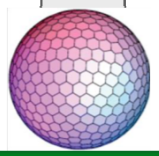
GIGA	TERA	PETA	EXA	ZETTA
10^9	10^{12}	10^{15}	10^{18}	10^{21}

SERVER SYSTEM ARCHITECTURE

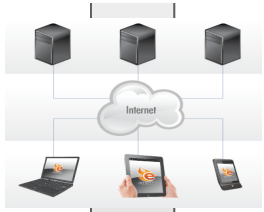
Scientific computing

Data Analytics

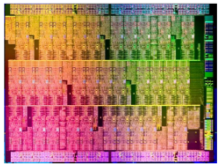
WEB servers



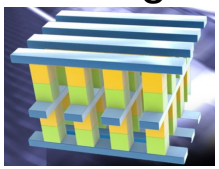




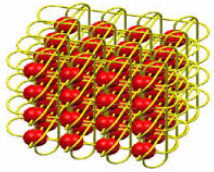
Processor



Memory & Storage



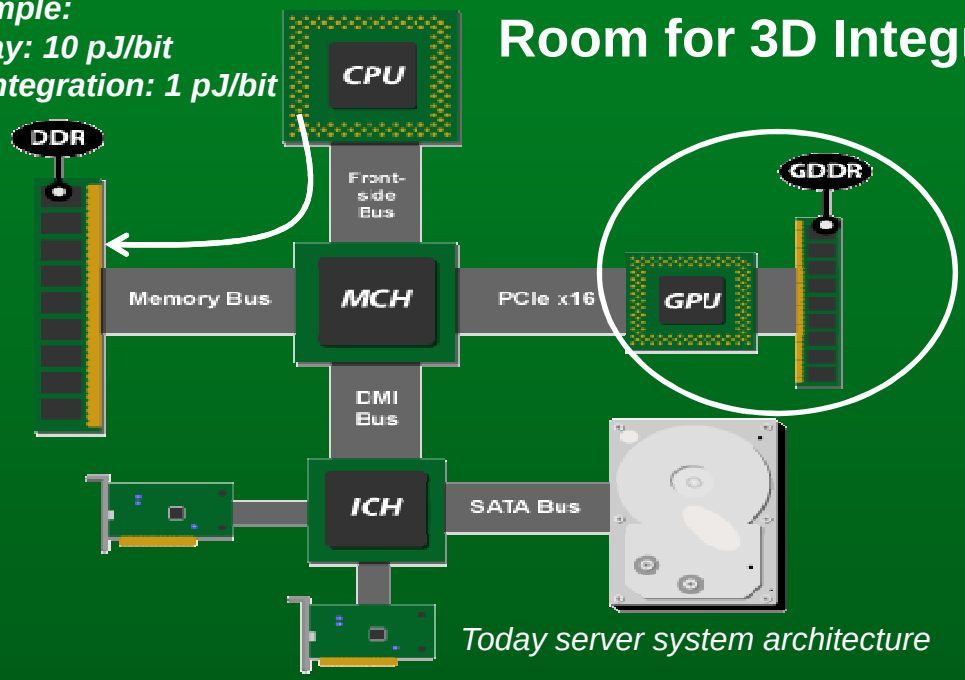
Interconnect



Example:
Today: 10 pJ/bit
3D integration: 1 pJ/bit

Room for 3D Integration ?

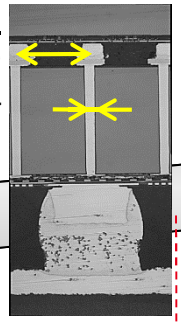
YES



Today server system architecture

3D INTEGRATION LANDSCAPE @ LETI

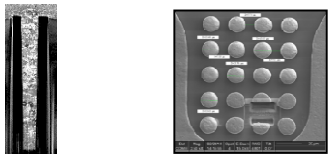
3D Contact :
Die-to-die Through-Silicon-Via (TSV)



Pitch
Diameter

3D Density of Integration ↗

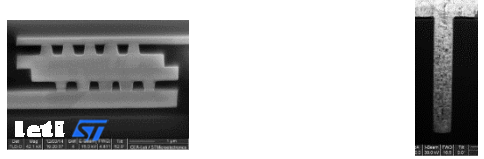
TSV + µBump
Diameter: 10 µm
Pitch : 20 µm



~10^3 3D Contacts / mm²

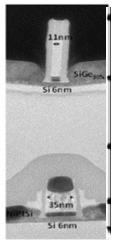
Cu-Cu
Diameter : 1.7 µm
Pitch : 3.4 µm

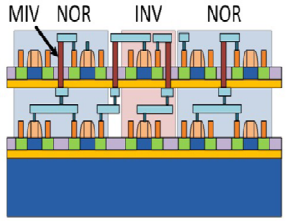
HD-TSV
Diameter : 0.85 µm
Pitch : 1.75 µm



~10^5 3D Contacts / mm²

Monolithic 3D (CoolCube™)
Diameter: 0.05 µm
Pitch : 0.11 µm

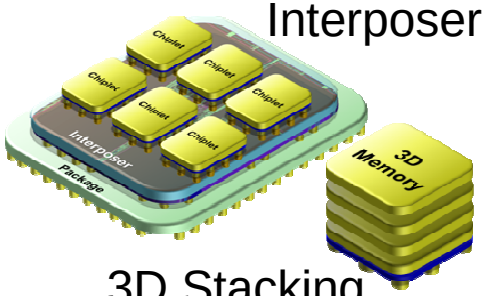




10^8 3D Contacts / mm²

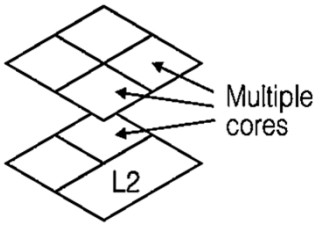
SoC Level Integration

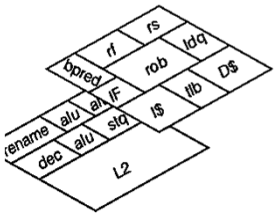
Interposer



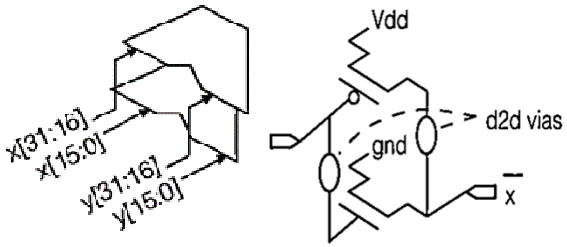
3D Stacking

Core-/Block-Level Integration



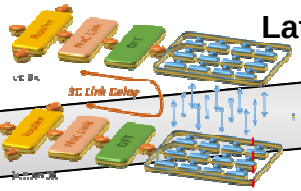


Gate-/Transistor- Level Integration



3D ARCHITECTURE & DESIGN SOLUTIONS @ LETI

3D Plug :
Chip-to-chip

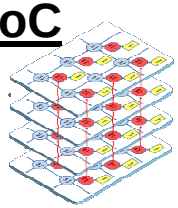


Area, Throughput, Latency

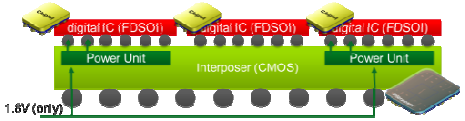
3D Density of Integration ↗

Advanced architecture exploration

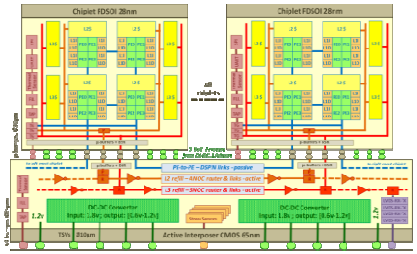
3D-NoC



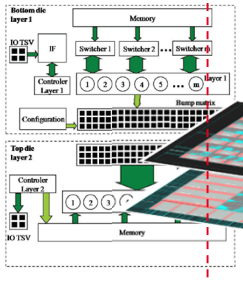
Power Mngt.



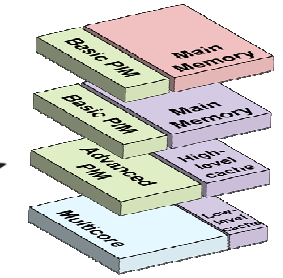
Many-core Computing



Processing-in-Memory



Neuromorphic



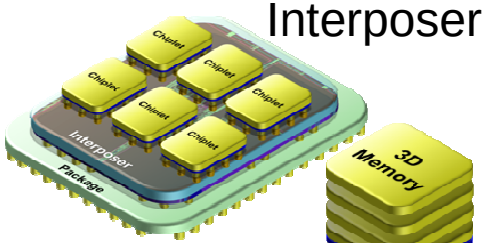
~10^3 3D Contacts / mm²

~10^5 3D Contacts / mm²

10^8 3D Contacts / mm²

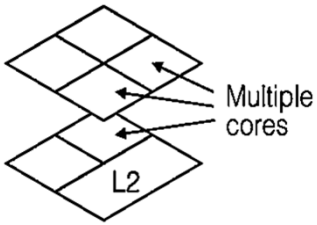
SoC Level Integration

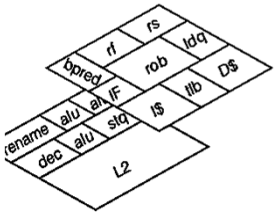
Interposer



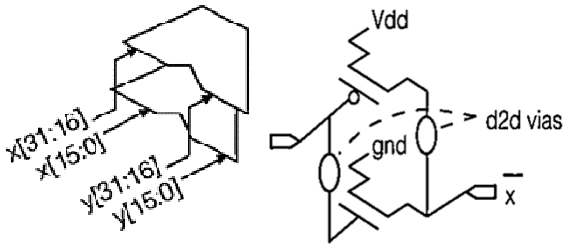
3D Stacking

Core-/Block-Level Integration





Gate-/Transistor- Level Integration



WHERE IS 3D IN COMPUTING LANDSCAPE ?

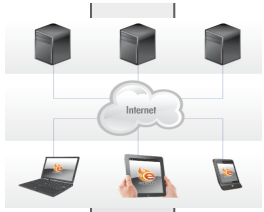
Scientific computing

Data Analytics

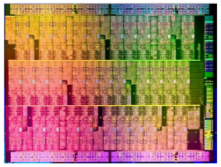
WEB servers



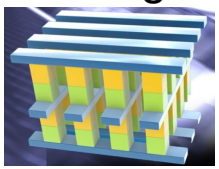




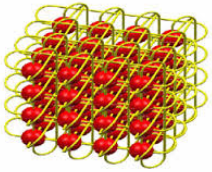
Processor



Memory & Storage



Interconnect



Many-cores, Heterogeneity (GPU, FPGA).

→ Interposer integration

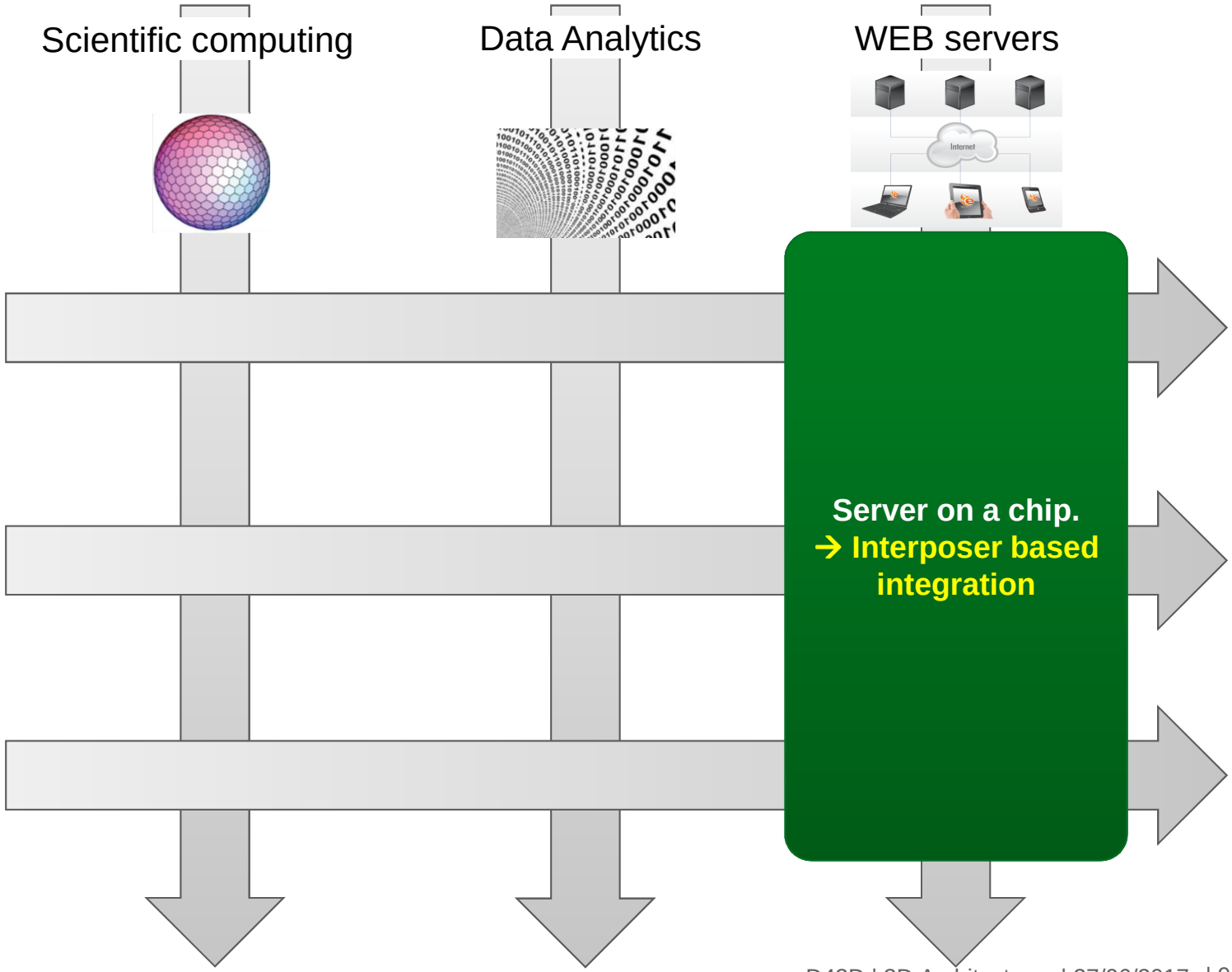
3D Memories.
→ 3D stacking

Neuromorphic, Processing in Memory (PIM).
→ High density 3D and monolithic 3D

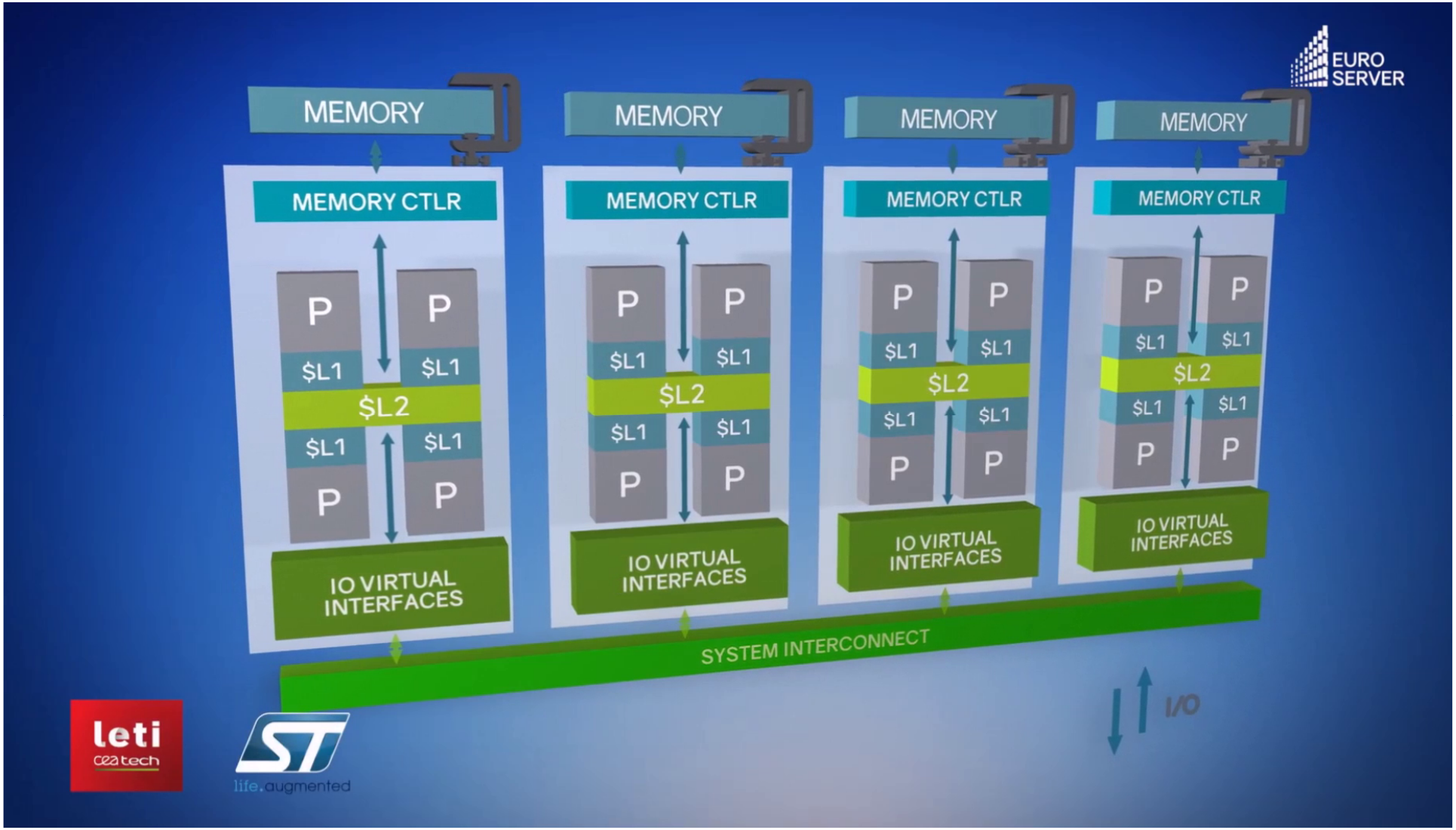
Server on a chip.
→ Interposer based integration

From rack-to-rack to chip-to-chip.
→ Photonic interposer integration

SERVER ON A CHIP

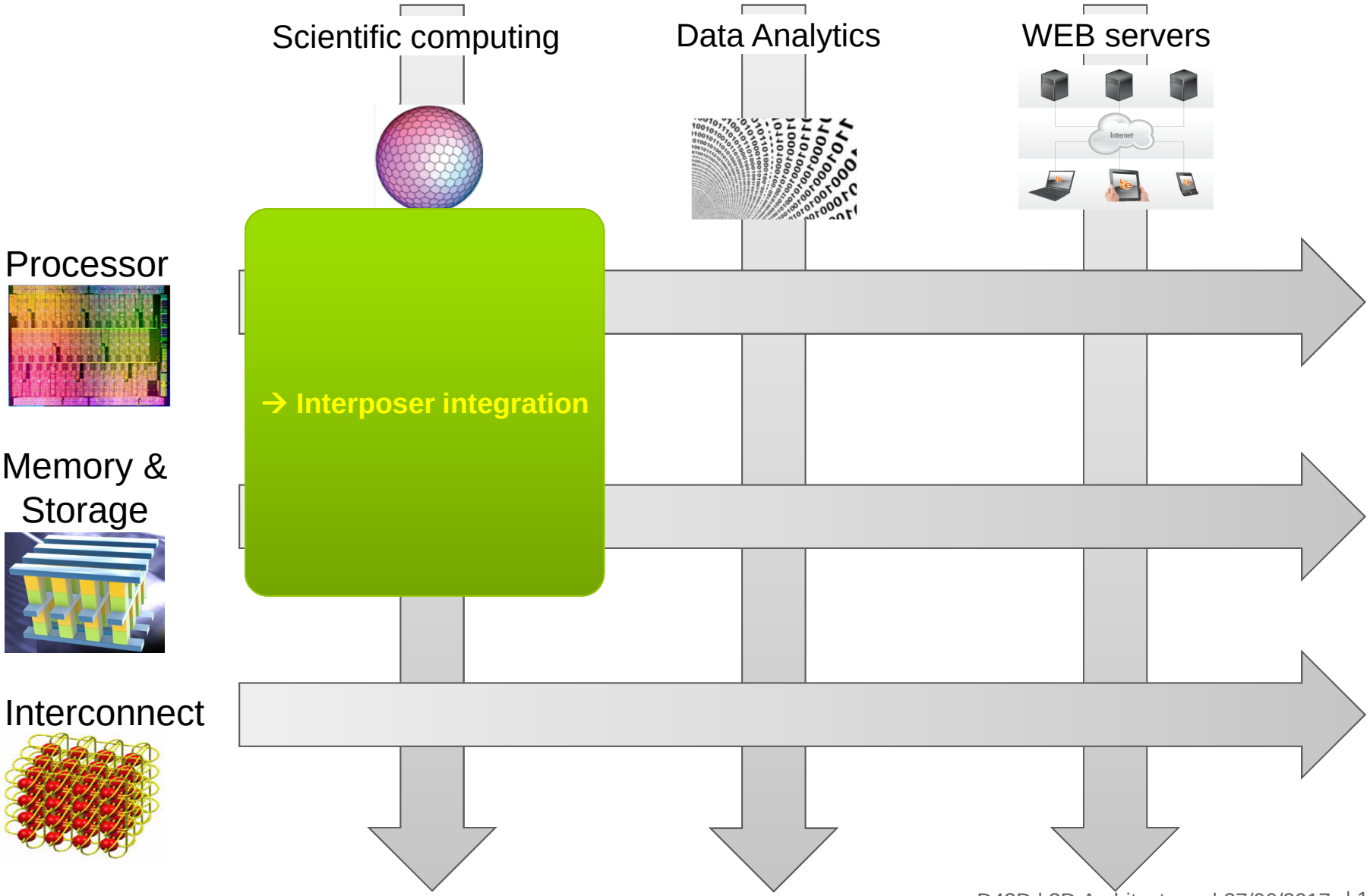


EUROSERVER ARCHITECTURE



https://youtu.be/2EnEKoZ2Tp0

INTERPOSER BASED INTEGRATION



PARALLEL PROGRAMMING MODELS FOR COMPUTING

Programming Model

Distributed Memory

Shared Memory

Partitioned Global Address Space (PGAS)

PE Processing element (up to LLC)
M Memory
N Network-on-Chip

SW Partitioning

MPI

OpenMP

MPI
OpenMP

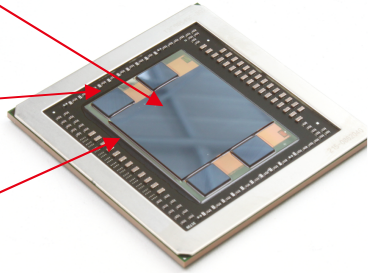
Thread

Silicon die

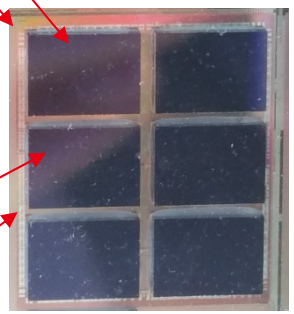
Interposer

3D Physical Partitioning

AMD Radeon™ R9 Fury X



NANOELEC
IRT 3D



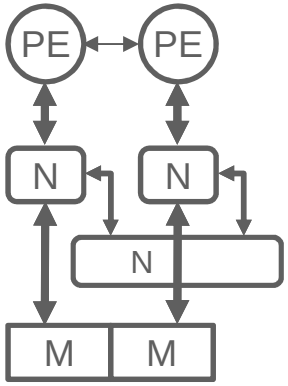
ExaNoDe

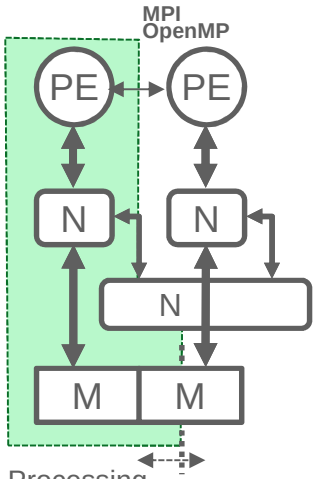
MPI Message Passing Interface **OpenMP** Open Multi-Processing

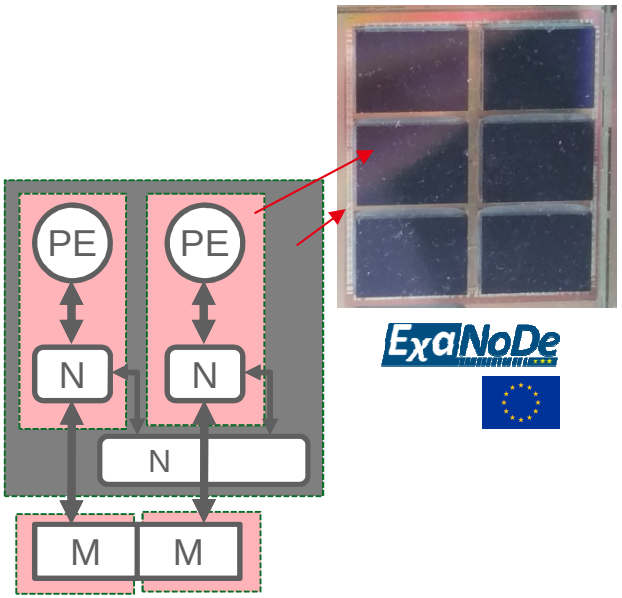
PGAS

Programming Model SW Partitioning 3D Physical Partitioning

Partitioned Global Address Space (PGAS)





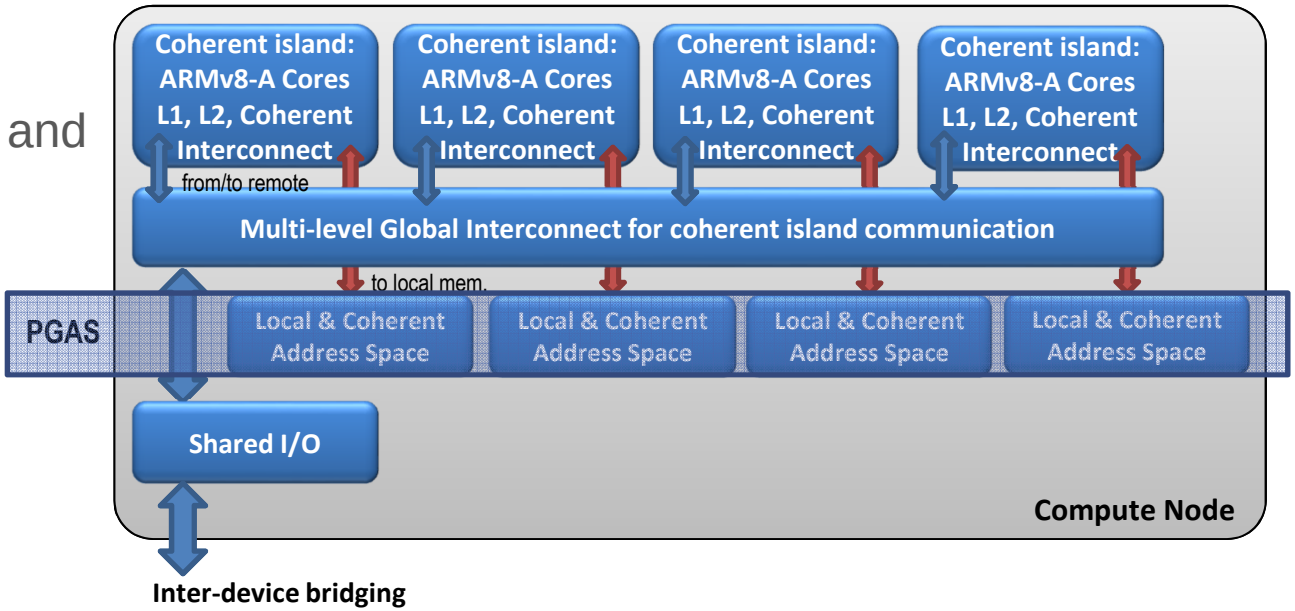


MPI Message Passing Interface **OpenMP** Open Multi-Processing

ExaNoDe PGAS architecture

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

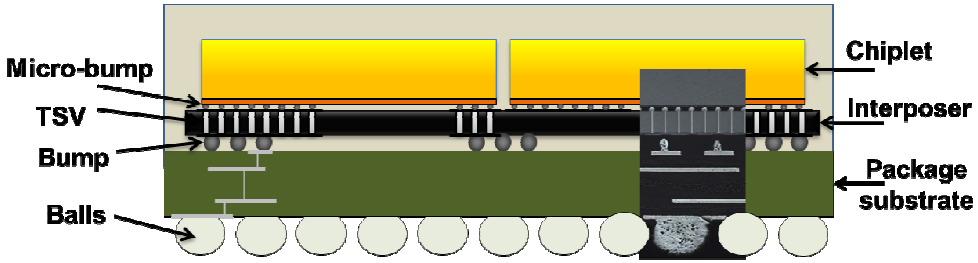
- **Coherent Island:** EUROSERVER
  - Many ARMv8 processors
  - Local coherent interconnect
  - Path to local memory
  - Path "to remote" memory locations
  - Path "from remote" compute units
- **Compute Node:**
  - Scale-out with "from" and "to" remote port connections to global network
- **Memory scheme:**
  - Partitioned Global Address Space

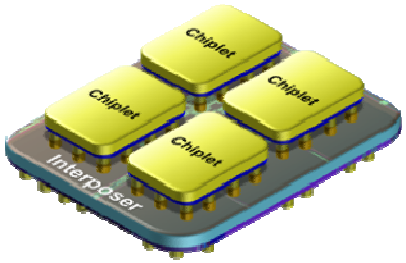


ExaNoDe integration approach

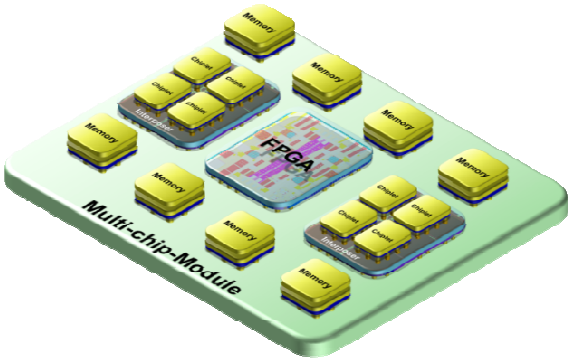
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

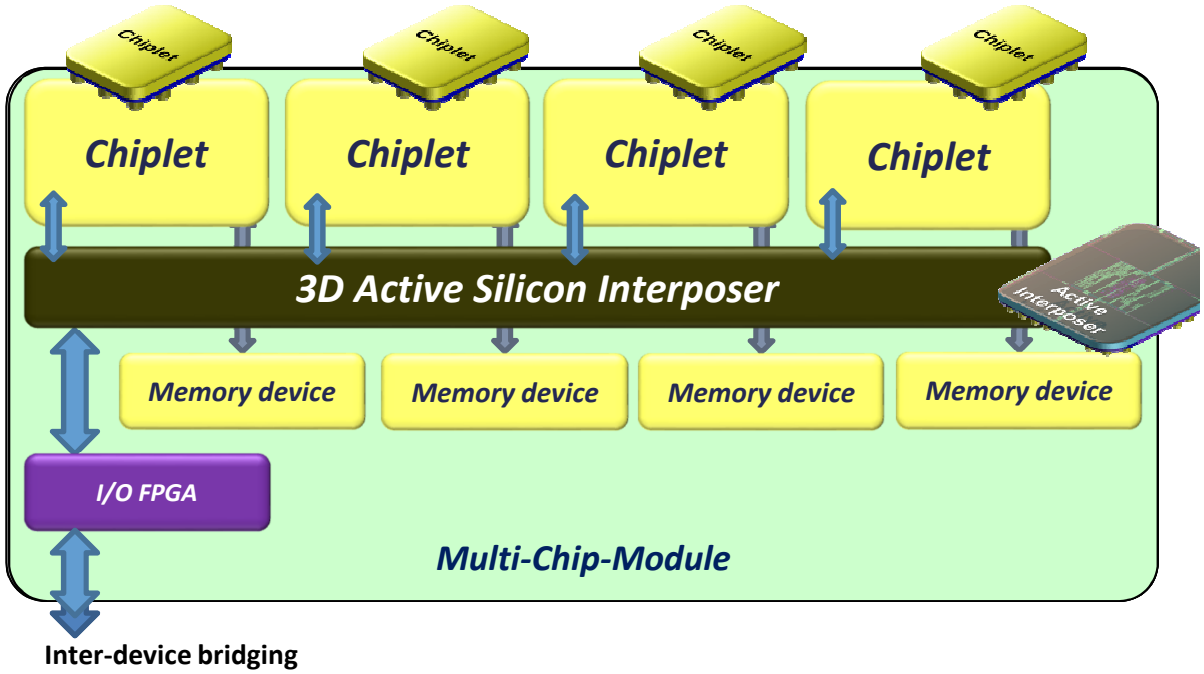
- 3D integration with active silicon interposer and chiplets.





- Multi-chip-Module integration for bare dies.





ExaNoDe: 3D Integration for PGAS

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

ExaNoDe

European Exascale Processor Memory Node Design

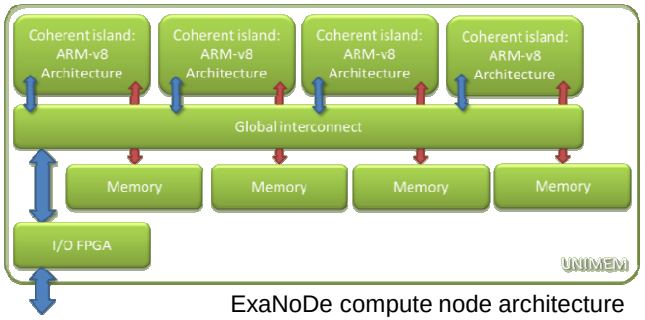
EC PROGRAMME: H2020-FETHPC-2014, HPC Core Technologies

Key words: High Performance Computing (HPC), Low Power Processors, Memory, Accelerators, 3D-integration, OS, Runtime, Message Passing Interface (MPI), Virtualization

Web site: www.exanode.eu



ExaNoDe targeted application: High Performance Computing



ExaNoDe compute node architecture

PROJECT AT AGLANCE

Coordinator:
CEA-LETI (FR)
13 partners

Budget: € 8.6 m
EC Contribution: € 8.6 m

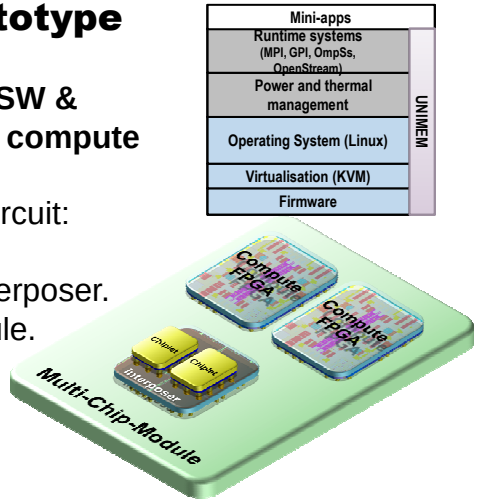
Duration: 36 months
(Oct.2015 – Sept. 2018)

Main objectives

ExaNoDe investigates and develops the building blocks for a highly integrated, high-performance, heterogeneous System-on-a-Chip (SoC) aimed towards exascale computing

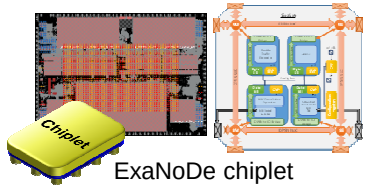
Project's prototype

- **Integrated HW/SW & heterogeneous compute node:**
  - 3D Integrated Circuit:
    - Chiplet,
    - Active interposer.
  - Multi-Chip-Module.
  - Software stack.

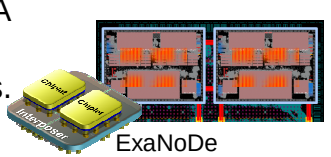


Leti's outcomes

- **3D Integrated Circuit:**
  - Chiplet design with communication infrastructure.
  - Interposer design with FPGA interface.
  - Interposer 3D process steps.
  - Chiplets on interposer assembly.



ExaNoDe chiplet

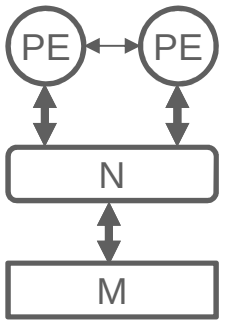


ExaNoDe
3D Integrated Circuit

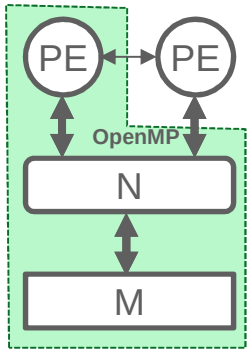
SHARED MEMORY

Programming Model

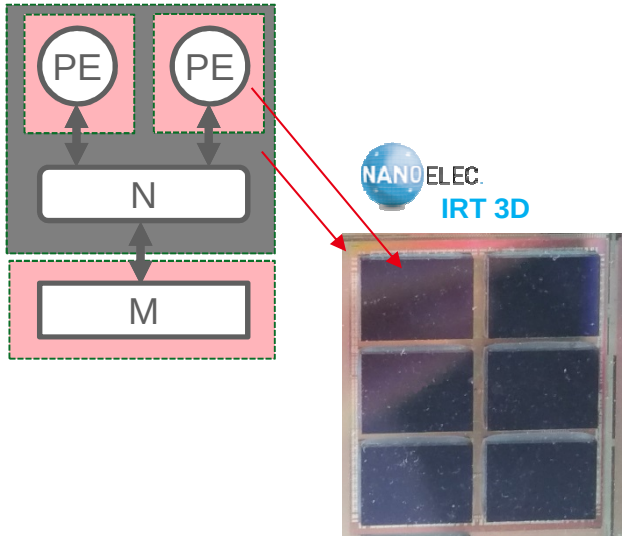
Shared Memory



SW Partitioning

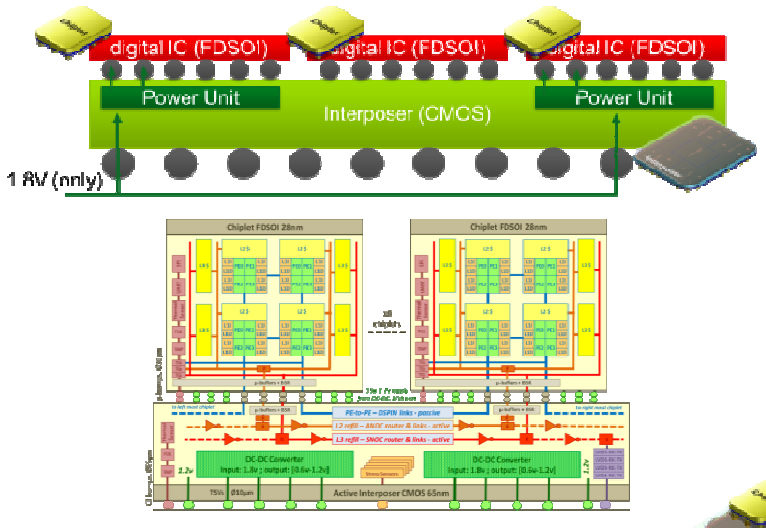


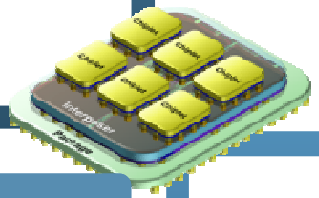
3D Physical Partitioning



INTACT: 3D INTEGRATION FOR SHARED MEMORY

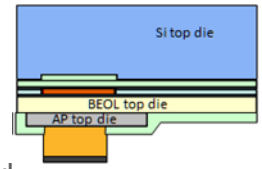
➡ **Active Interposer for computing: 28nm FDSOI Chiplets 3D-Stacked on a 65nm active interposer offering a 96 cores cache coherent compute fabric**

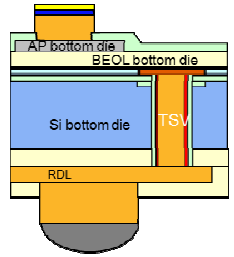




3D partitioning for high energy efficiency and reduced cost

- 28nm FDSOI chiplets (x6)
  - Low Power Compute Fabric
  - Wide Voltage Range (0.6V – 1.2V)
  - Body Biasing for logic boost & leakage ctrl
- 65nm Active Interposer
  - Power unit (Switched Cap DC-DC conv.)
  - Interconnect (Network-on-Chip)
  - Test, clocking, thermal sensors, etc

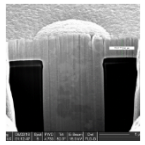




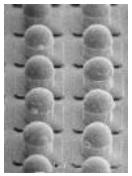
- **Performance Targets**
  - **100 GOPS**
  - **10 GOPS/Watt**
  - **25 Watts total**

Symposium'2016
3DIC'2015
ISVLSI'2015

- Cache Coherent Compute Fabric
  - 96 cores (MIPS-32bit)
  - L1/L2/L3 coherent caches
  - Implemented with 3D-Plugs
  - Full support of Linux OS



TSV
Ø 10µm
Height 100µm



µ-bumps
Ø 10 µm
Pitch 20 µm

- Application Targets
  - Big Data
  - Networking
  - High Performance Computing



INTACT MOTHER BOARD : A “SERVER” NODE



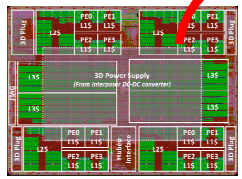




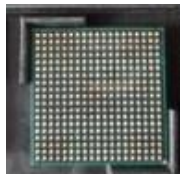


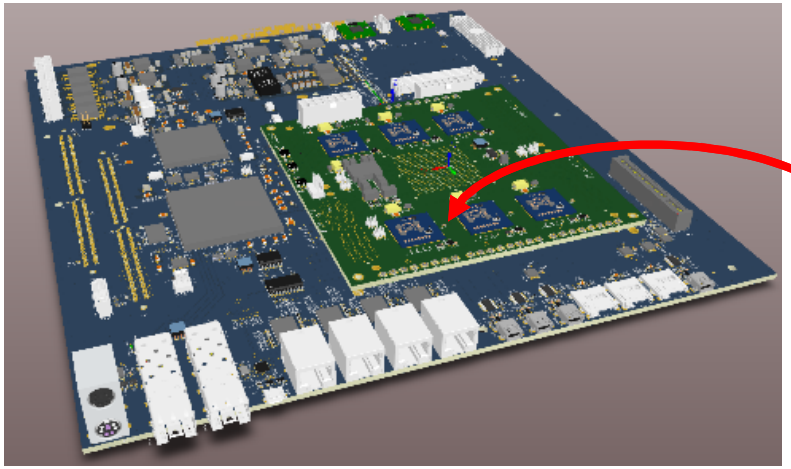
- **INTACT Demonstration, as a “Server” Node**
  - Design of a « Server » box, executing full Linux onto 96 cores
  - 2 FPGAs to handle all circuit IOs & bridges
  - Ethernet 4 x 1 Gb/s, 2 x 10 Gb/s
  - PCI Express
  - 32 Gbyte SDCard
  - 32 GByte DDR4 memory
  - HDMI, USB2, UART, keyboard, mouse, etc
  - Power supplies & monitors for power measurements
- ***Integrate either 1 Chiplet (Standalone version) or INTACT (Active Interposer with 6 chiplets)***

- **Application Targets**
  - Big Data
  - Cloud Computing
  - Networking
  - High Performance Computing











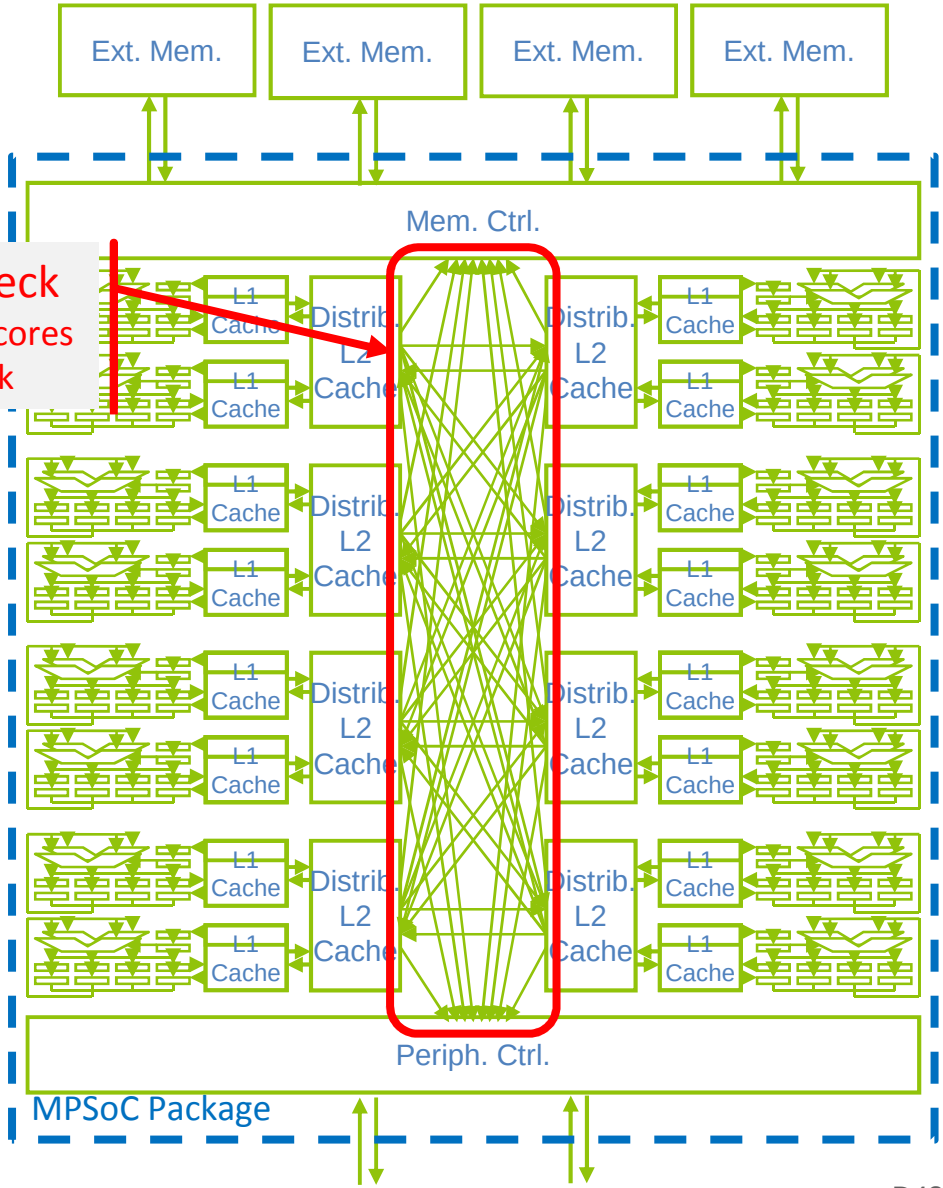


1st Version : Chiplet std-alone

- *Linux OS booting*
- *Starting circuit measurements*

COMMUNICATION BOTTLENECKS IN MANYCORES

Internal Com. Bottleneck
Quadratic BW increase w. #cores
Constant throughput per link



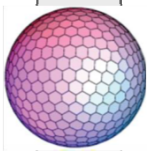
(2015)[NOCS] Thonnart, Y.

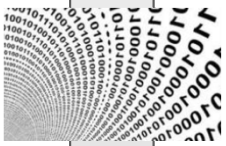
3D INTEGRATION LEVERAGES NEW COMPUTING ARCHITECTURES

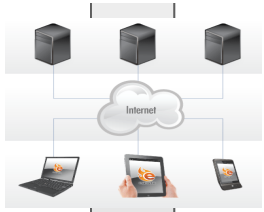
Scientific computing

Data Analytics

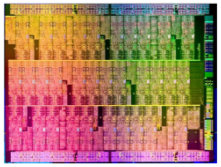
WEB servers



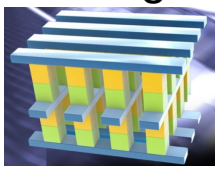




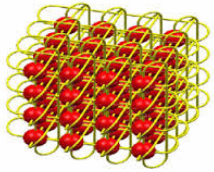
Processor



Memory & Storage



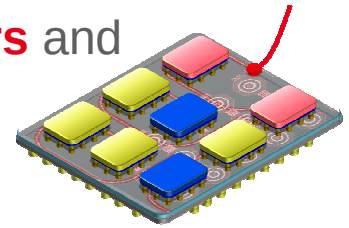
Interconnect



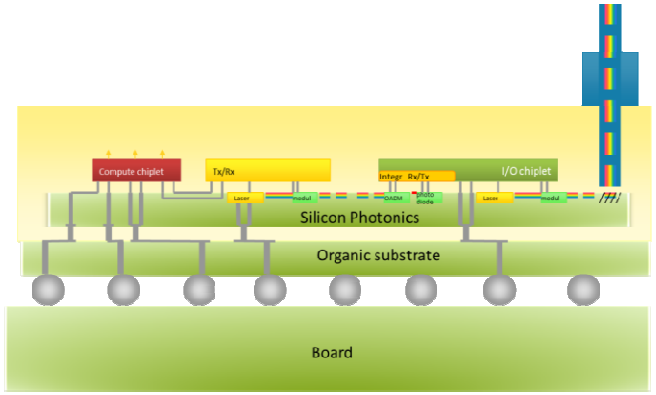
From rack-to-rack to chip-to-chip.
→ Photonic interposer integration

HUBEO+ : PHOTONICS FOR MANY-CORES

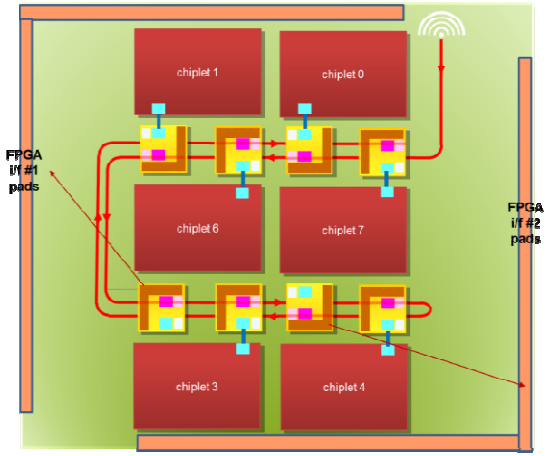
- **Optical network-in-package** to interconnect **microprocessors** and **memories** integrated in a **silicon photonics interposer**
- **Convergence of 3D and Photonics technologies**



On-going design of a large system with 6 chiplets, 96 cores, 8 transceivers



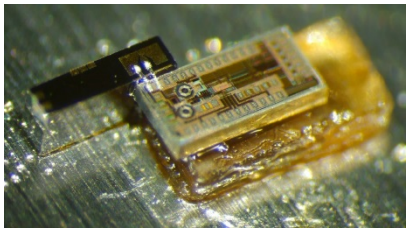
Cross section



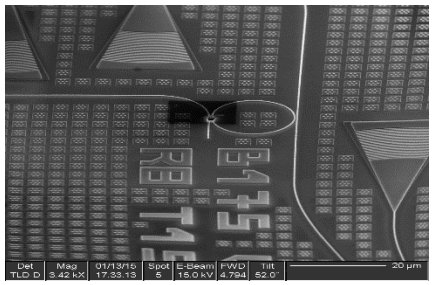
Top view

Design Challenges ?

- Thermal Control of WDM devices
- High-density high-performance integration
- E/O co-design of drivers
- Optimized short-range optical WDM system, devices and protocols



Preliminary integration of E/O transceiver and photo-diode



Photonic Interposer

Demonstrator planned for 2018

INSTITUT CARNOT CEA LETI

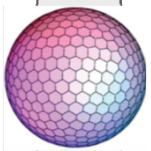
[unpublished]

PERSPECTIVES FOR 3D INTEGRATION

Scientific computing

Data Analytics

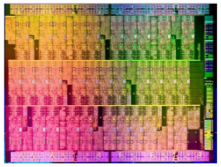
WEB servers



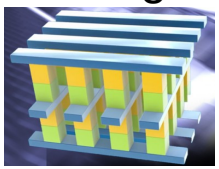




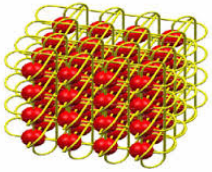
Processor



Memory & Storage



Interconnect



Neuromorphic, Processing in Memory (PIM).
→ High density 3D and monolithic 3D

CONCLUSION

- **Computing applications are various with specific challenges:**
  - Cost for WEB servers,
  - Parallelism for Scientific Computing,
  - Data movement energy for Data Analytics.

- **New architectures are emerging:**
  - Server-on-a-chip to handle cost for WEB servers,
  - New programming models with advanced Network-on-Chip fabric to handle parallelism with Scientific Computing,
  - Disruptive architectures (Neuro, PIM) to bring compute close to data for Data Analytics.

- **Advanced packaging enables system architecture specialization:**
  - System-in-Package for server on a chip,
  - Silicon Interposer for new NoC fabric,
  - High density 3D and Monolithic 3D for disruptive architectures.

ACKNOWLEDGMENTS

- **CEA-LETI design & technology teams :**
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  - S. Cheramy, D. Lattard, L. Arnaud, F. Bana, A. Garnier, A. Jouve, T.Mourier

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- **Our Partners**





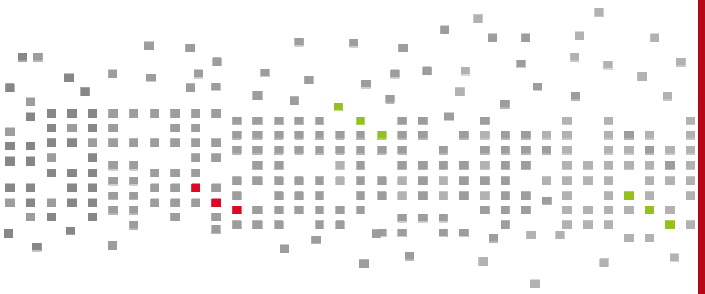
SAVE THE DATE

LETI INNOVATION DAYS AT GRENOBLE
JUNE 28-29, 2017

Leti, **50** years of pioneered innovations

Leti Day, **2** days of discovery, innovation & networking

Leti Gala Evening, **1** VIP Event for our partners & prospects



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