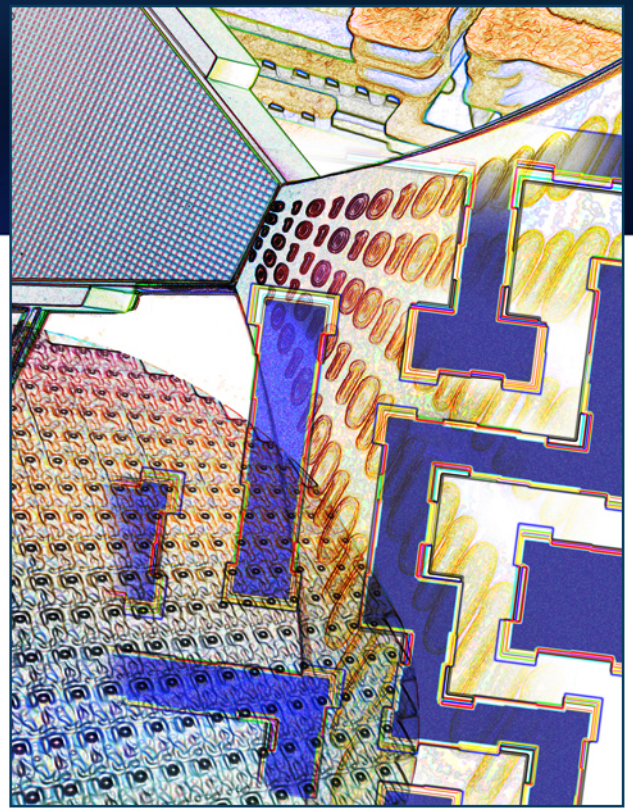
Modeling Challenges in Electrical Design of 3DIC based Systems



Dusan Petranovic

Interconnect Modeling Technologist
Design2Silicon Division

Mentor Graphics®

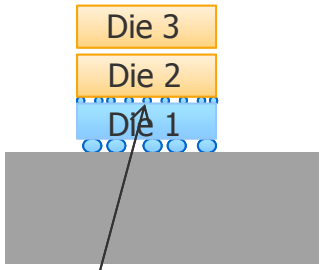
dusan_petranovic@mentor.com

Outline

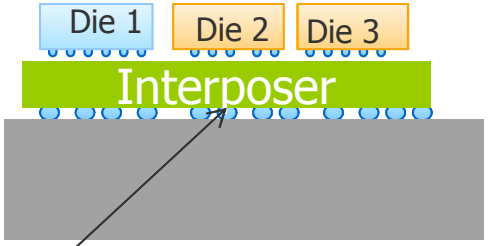
- Challenges in 3D Stack Modeling
  - Wide variety of stack configurations and components related to 3D Stacks
  - Parasitic Extraction Challenges
- 3D Stack Verification and Extraction
  - Stack verification flow
  - TSV extraction solutions
- Intra Die Component Interactions and Extraction
  - TSV to TSV
  - TSV to RDL
- Inter Die Interactions
  - Analysis of die-to-die capacitive coupling impact in F2F bonded dies
  - Inductive couplings

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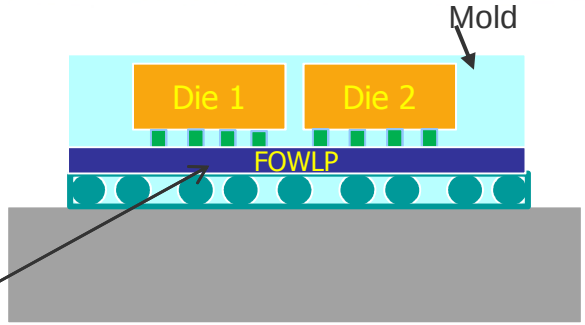
Stack Configurations and Components



3D



2.5D



FOWLP

dies,
interposers, package



TSVs
- on chip
- On interposer

Back side
metal stack

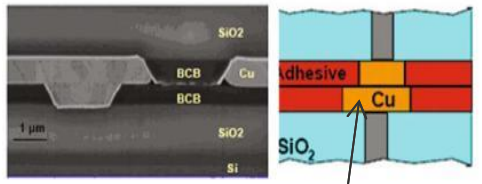


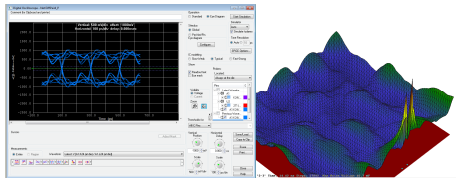
Fig. 1.35 A die-Stack using a combination of Cu-Cu and BCB adhesive bonding at RPI [14]

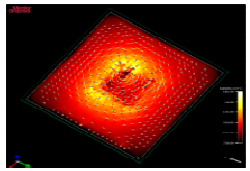
Interface:
- micro bumps, pillars
- direct Cu bonding

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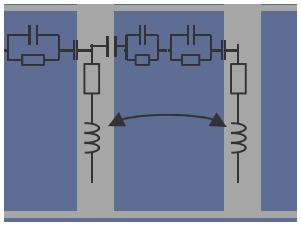
EDA Challenges in 3D Stack Modeling and Extraction

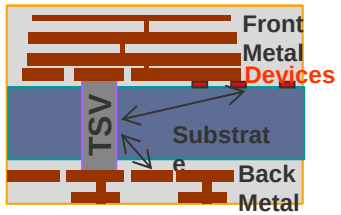
- **Modeling**
  - Different phenomena: electrical, thermal, mechanicals;
  - Interaction modeling
  - Tradeoff between needed accuracy and model complexity and flow integration
  - Consistency between different levels of abstraction

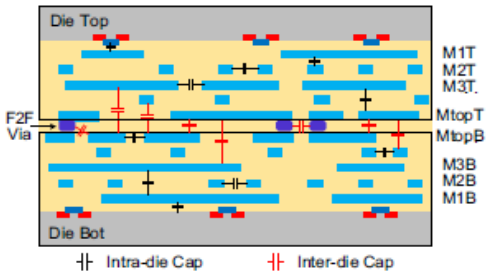




- **Parasitic Extraction**
  - What to extract
  - What interactions are important
  - Intra- die
    - TSV - to -TSV
    - TSV - to - RDL
    - TSV- to -Device
  - Inter-die
    - F2F bonded dies
    - FOWLP
  - What level of accuracy is needed?



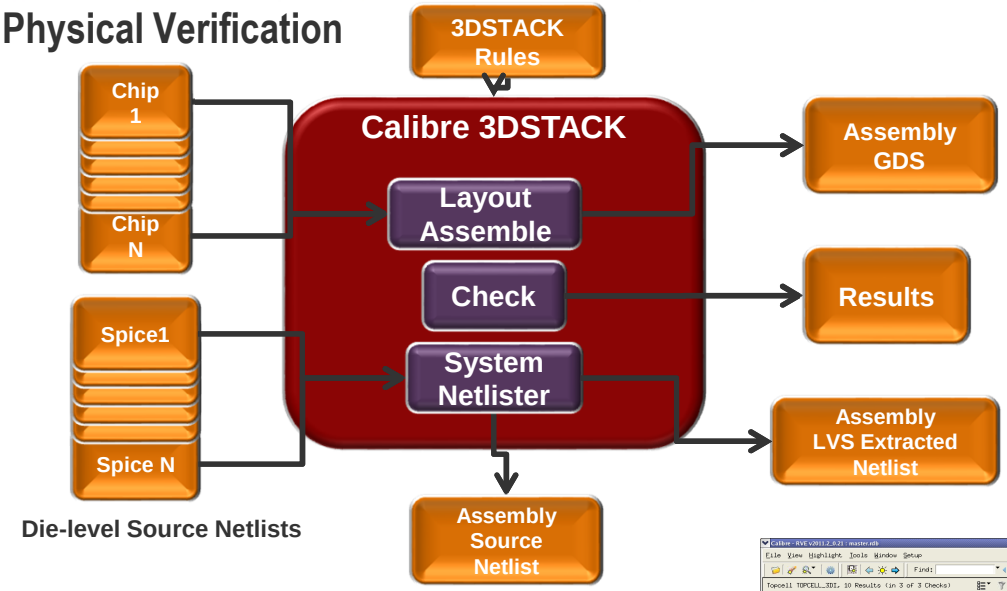


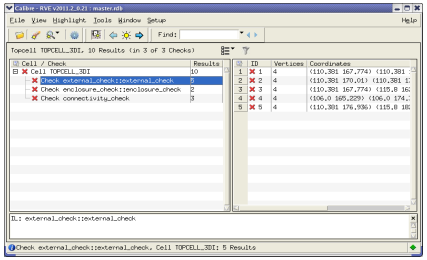


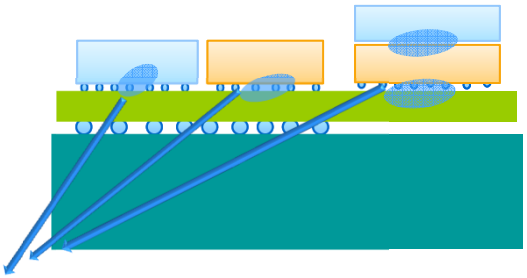
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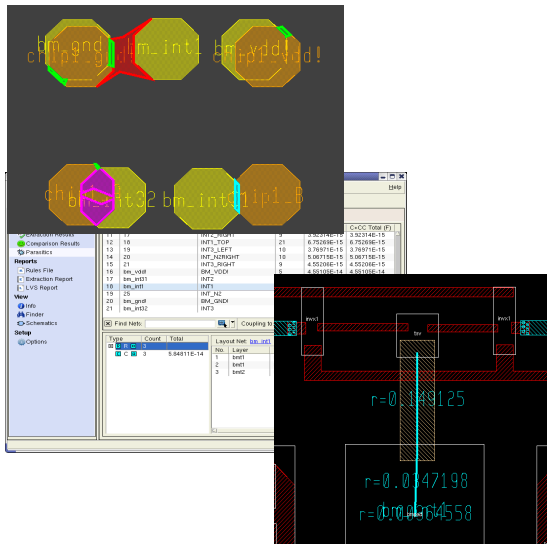
3D Stack Verification Flow

Physical Verification









- Verify micro-bumps ***physical alignment***
- Verify proper ***electrical connectivity*** through die/interposer interfaces

Parasitic Extraction

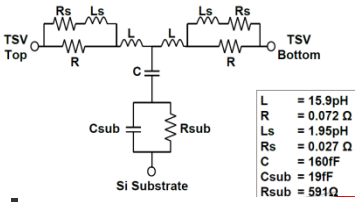
- Extract parasitics of the dies (front and ***back side*** metal stacks)
- ***Insert provided TSV*** circuit into integrated parasitics/TSV netlists, or
- ***Extract TSV*** and then integrate

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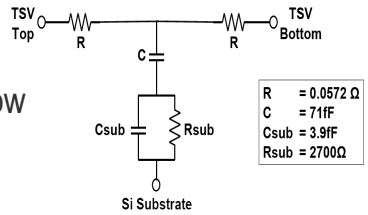
Extraction solutions: TSV Modeling Approaches

- **Stand Alone TSV models**
  - Advantage: Easy to integrate into a flow ; Sufficient in many situations
  - Challenges: Not adequate for high density, high frequency applications

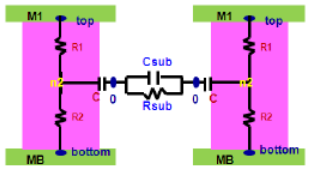
for analog flow



for digital flow

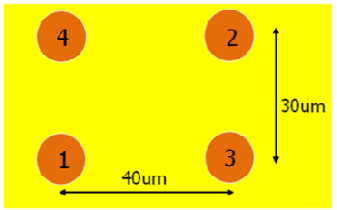


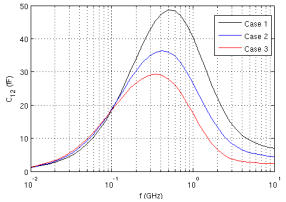
- **Compact parametrized models**
  - Advantage: Can account for some interactions; Faster than FS
  - Challenges: Hard to account for all situations, i.e. to parameterize for all important variables



t_{dis}	t_1	t_2	t_3	t_4	t_5	…	t_{max}
C_{sub}	C_1	C_2	C_3	C_4	C_5	…	C_{max}
R_{sub}	R_1	R_2	R_3	R_4	R_5	…	R_{max}

Case 1: TSV 3 and TSV 4 are not present in layout
Case 2: TSV 4 is not present in layout
Case 3: All 4 of the TSV's are present



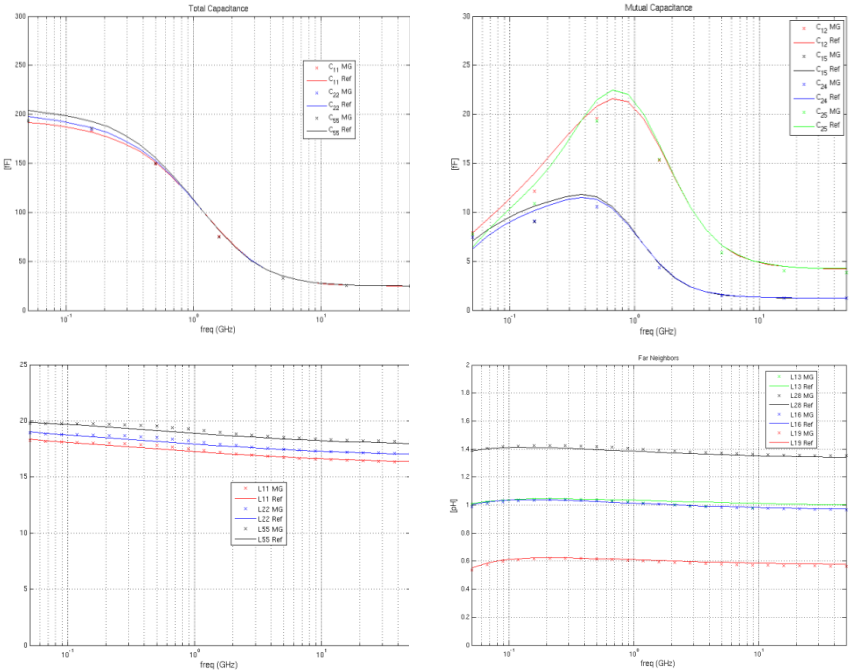


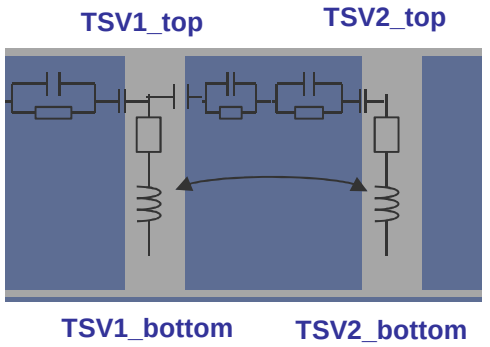
- **Field solver approach**
  - Advantage: Most accurate
  - Challenges: Performance; Integration

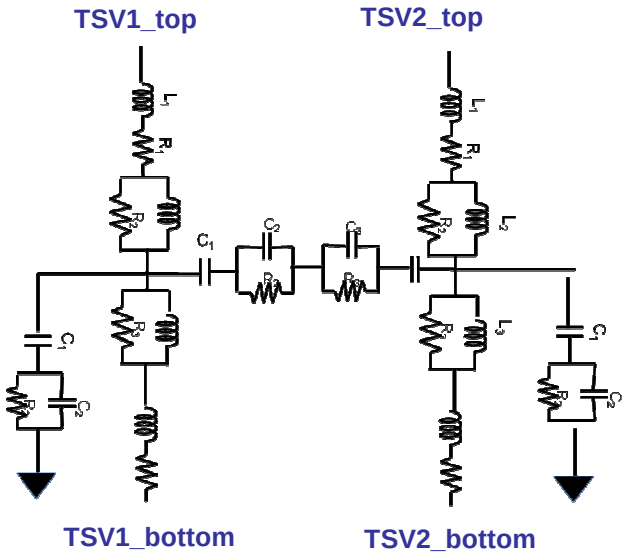
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Fast Field Solver Based Solution

- Fast-Field Solver based solution extracts TSV parasitics and TSV to TSV couplings (capacitive and inductive)
  - Produces netlist consisting of frequency-independent linear elements.
  - Accurate vs. reference results
  - Order of magnitude faster than other field solvers







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Field Solver Based Solution (Engine)

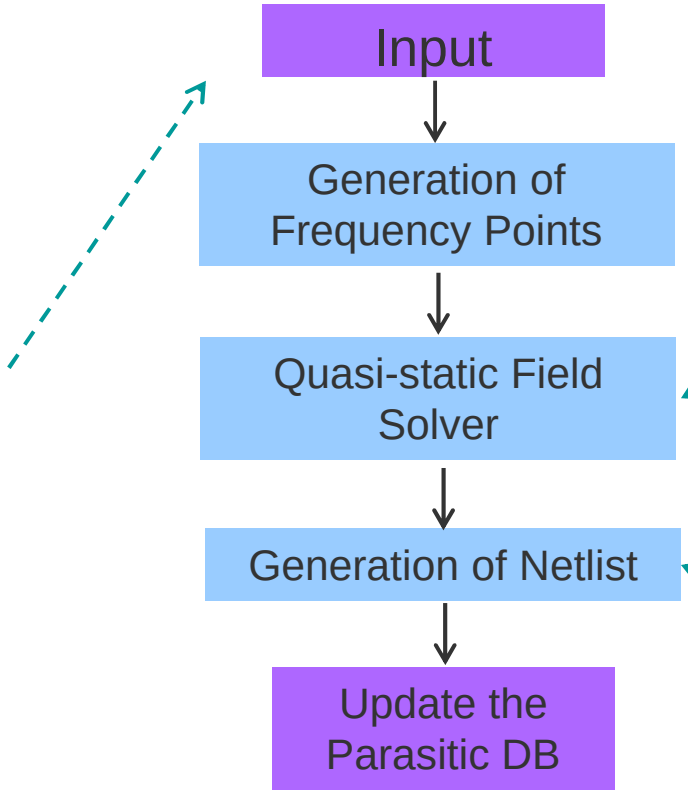
```
TSV = my_tsv {
    measured_from = BM1
    measured_to = M1
    radius = 3
    hollow_radius = 0
    height = 52.6565
    top_enclosure = 5
    bot_enclosure = 5
    resistivity = 2
    depletion_width = 0
    insulator = {{0.3, 5.2}}
}
```

```
substrate = psub {
        zbottom = -50
        ztop = -0.7
        resistivity = 101800
        eps = 11.9
}

well = psub_tw {
        zbottom = -0.7
        thickness = 0.7
        resistivity = 100
        eps = 11.9
}
```

```
conductor = BM1 {
        thickness = 10
        min_width = 0.045
        min_spacing = 0.045
        extra_width = 0.0146846
        resistivity = 0.3
}

dielectric = Underfill  {
        thickness = 10
        eps = 3.3
        diel_type = planar
}
```



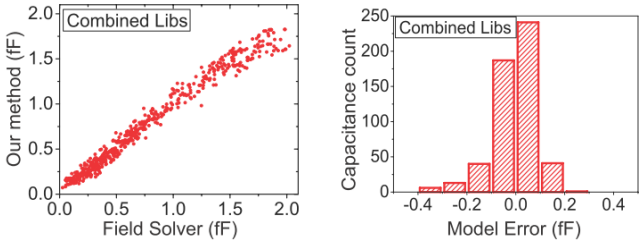
The FS is run for all the frequency points

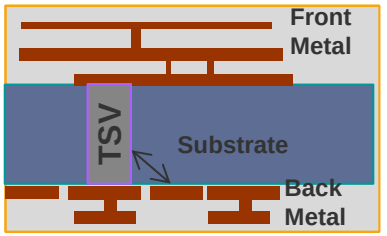
The netlist mimics the behavior of the frequency dependent data generated by the FS

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Extraction of TSV to Interconnect coupling

- Model and extract TSV to interconnect (RDL) extraction
- Full chip solution within 2% accuracy vs FS





- Significant impact:

TABLE I
TSV-TO-WIRE COUPLING FULL-CHIP IMPACT.

Is TSV-to-wire included?	no	yes
Longest path delay (ns)	4.48	5.08 (+13.4%)
Total power on TSV net (mW)	0.303	0.356 (+17.6%)
Total net switching power (mW)	2.42	2.50 (+3.3%)
Total noise on TSV net (V)	32.5	78.2 (+104%)

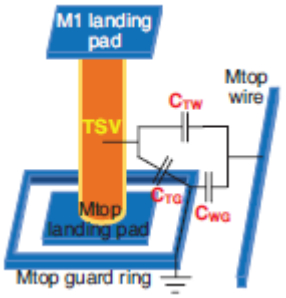
- To Reduce the impact

Table 6: Keep-out-zone impact on full-chip design. Power i reported in mW.

KOZ size (μm)	0.5	2.5	5
Longest path delay (ns)	5.08	4.95 (-2.6%)	4.77 (-6.1%)
Total power on TSV net	0.356	0.342 (-3.9%)	0.327 (-8.1%)
Total net switching power	2.50	2.47 (-1.2%)	2.45 (-2.0%)
Total noise on TSV net (V)	78.2	67.0 (-14.3%)	42.9 (-45.1%)

Table 7: Guard ring impact on full-chip design with 2.5μm KOZ. Power is reported in mW.

Guard ring width (μm)	0	0.5	1.5
Longest path delay (ns)	4.95	4.98 (+0.6%)	5.01 (-1.2%)
Total power on TSV net	0.342	0.351 (+2.6%)	0.358 (+4.7%)
Total net switching power	2.47	2.475 (+0.2%)	2.479 (+0.4%)
Total noise on TSV net (V)	67.0	58.0 (-13.4%)	53.6 (-20.0%)

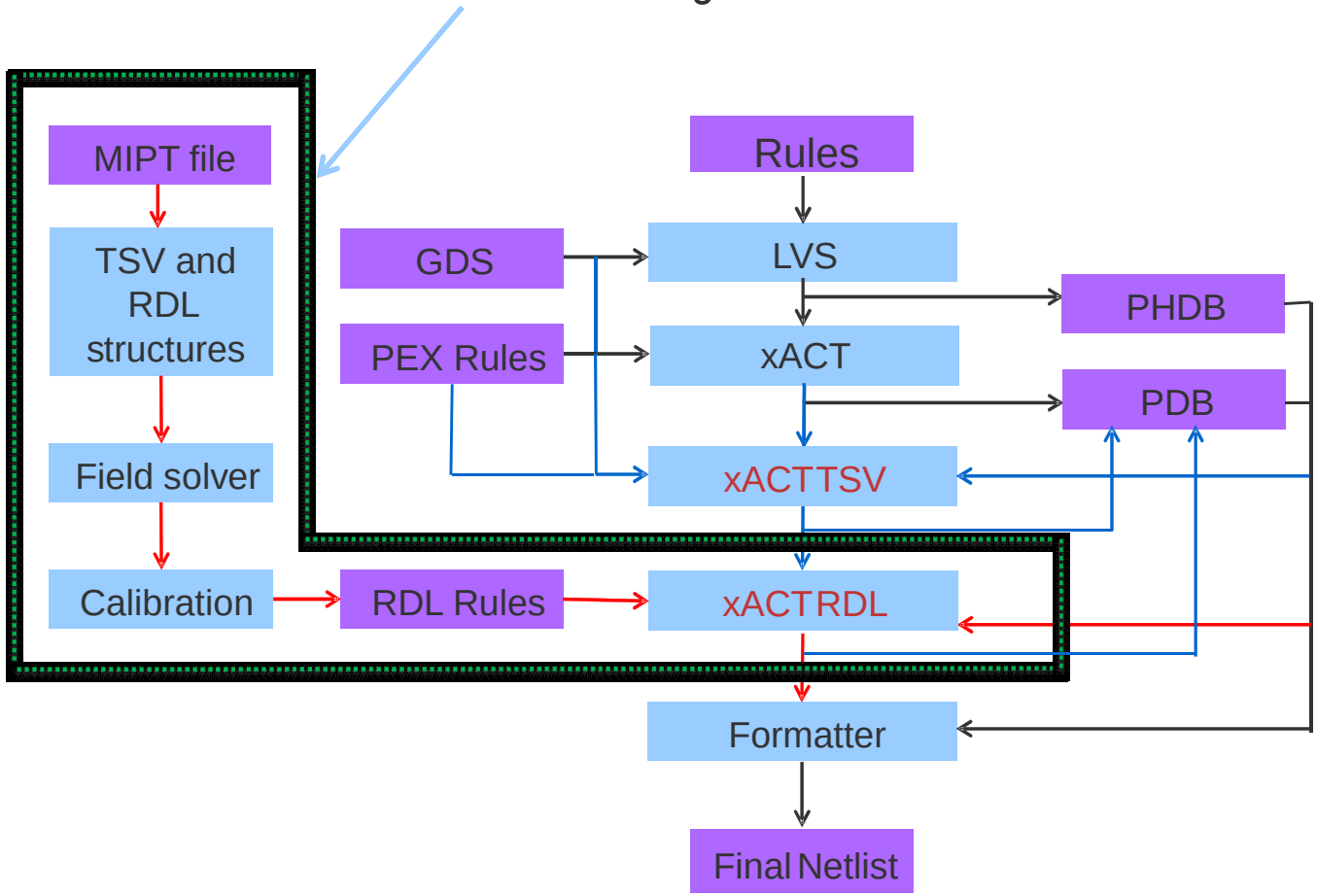


Y.Peng, D.Petranovic, SK.Lim, "**Multi-TSV and E-Field Sharing Aware Full-Chip Extraction and Mitigation of TSV-to-Wire Coupling**", IEEE Transaction on CAD of Integrated Circuits and Systems, Vol.34, NO.12, December 2015

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Integration with Extraction Tool

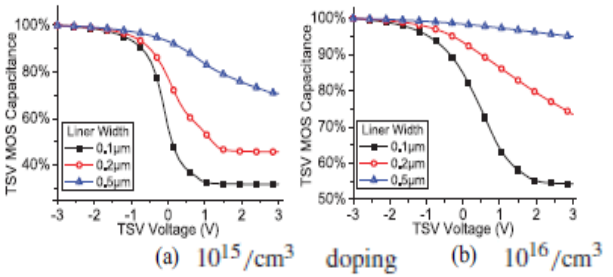
- To integrate TSV-to-RDL extraction with Calibre tool flow, the new rules should be defined in a new TSV-to-RDL extraction stage

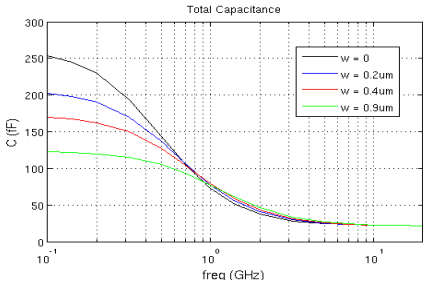


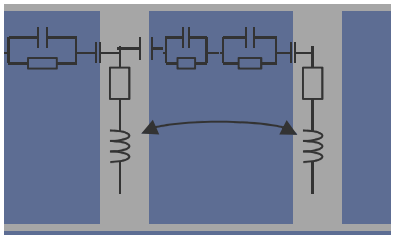
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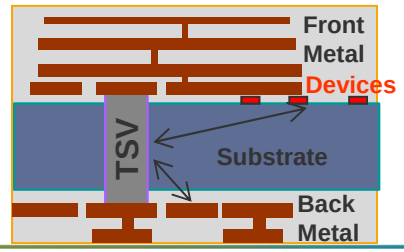
Issues in TSV Modeling

- Depletion region effects
  - TSD or TSV
    - Nonlinear behavior ; Capacitance vs. voltage across TSV
    - Support
      - Tables for C_{dep} vs. Voltage
      - Tables for W_{dep} vs. Voltage
  - Frequency dependence
    - Strong non-linear frequency dependence at low frequencies
    - Support
      - Additional Foster pairs for lower frequency
- Interactions between the TSVs
  - Capacitive and Inductive couplings
- Interaction between TSV and interconnect
  - Interactions with RDL and metal lines
- Impact of TSVs on device performance
  - Proper substrate description and modeling is needed







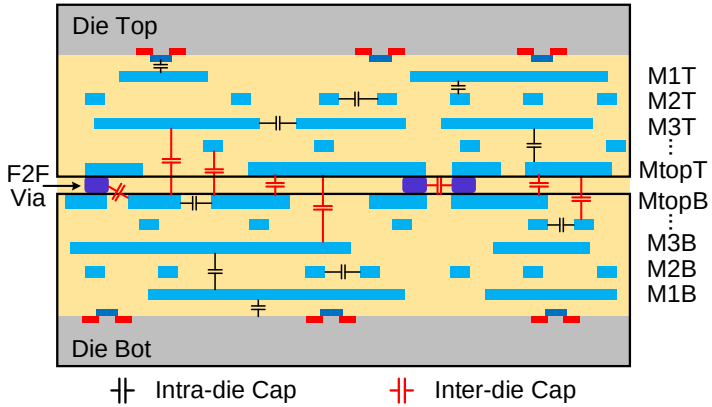


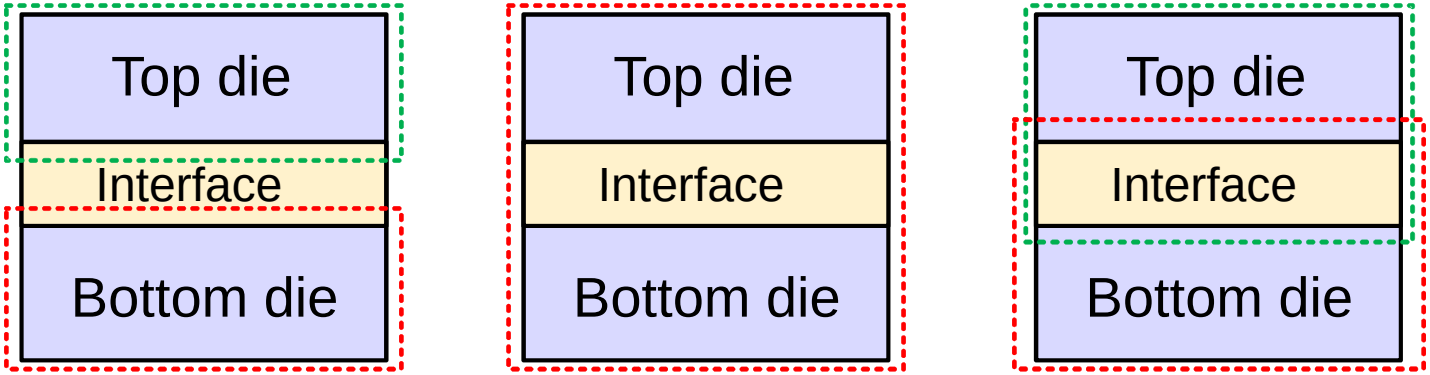
Y.Peng, T.Song, D.Petranovic, SK.Lim, **:"Silicon Effect-Aware Full-Chip Extraction and Mitigation of TSV-to-TSV Coupling"**, IEEE Transaction on CAD of Integrated Circuits and Systems, Vol.33, NO.12, December 2014.

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Three Ways of Full-chip F2F Bonded Dies Extraction

- **Die-by-die extraction**
  - — Extract the dies separately
- **Holistic extraction**
  - — Extract all layers simultaneously
- **In-context extraction**
  - — Extract each die separately but aware of neighboring die layers





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Impact of Extraction Methodology

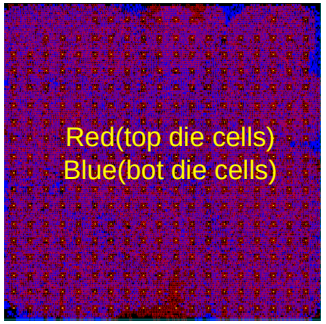
- die-by-die extraction underestimates coupling capacitance significantly, especially for layers close to the other die
- Holistic extraction corrects the errors
- In-context extraction is highly accurate

Die-by-die (D-D) vs. Holistic (Holi)

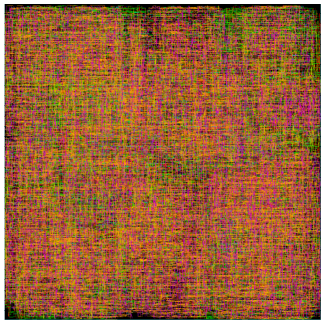
	M1B	M2B	M3B	M4B	M4T	M3T	M2T	M1T	Total
Holi	26.2	949	1,808	3,703	3,089	1,755	1,013	38.2	12,381
D-D	20.1	856	1,620	1,955	1,413	1,399	747	21.2	8,032
Err	-6.06	-93.4	-187	-1,747	-1,676	-356	-266	-17.0	-4,349
Err %	-23%	-9.8%	-10%	-47%	-54%	-20%	-26%	-45%	-35%

In-context (In-C) vs. Holistic (Holi)

	M1B	M2B	M3B	M4B	M4T	M3T	M2T	M1T	Total
Holi	26.2	949	1,808	3,703	3,089	1,755	1,013	38.2	12,381
In-C	26.3	950	1,803	3,679	3,058	1,734	1,001	38.0	12,287
Err	0.15	0.81	-5.15	-24	-31.0	-21.3	-12.3	-0.22	-93.3
Err%	0.6%	0.1%	-0.3%	-0.7%	-1.0%	-1.2%	-1.2%	-1%	-0.8%



Placement



Routing

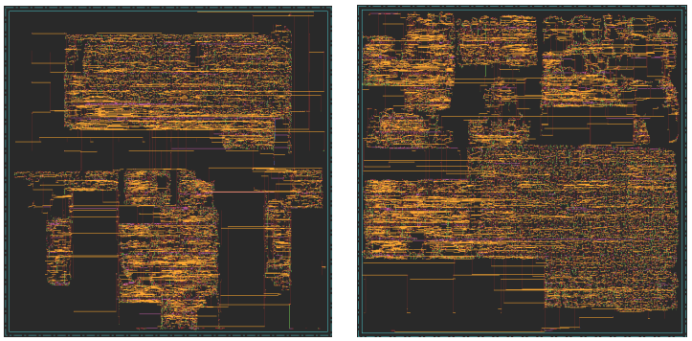
metric	Holi	D-D	Err%	In-C	Err%
Longest path delay (ns)	3.90	3.66	-6.2%	3.83	-1.8%
3D nets switching power (mW)	1.05	1.01	-3.5%	1.04	-0.4%
Total switching power (mW)	12.1	11.9	-1.7%	12.0	-0.8%
Total coupling cap on 3D nets (fF)	4.37	2.96	-32%	4.21	-3.7%
Total wire cap on 3D nets (fF)	10.8	9.35	-13%	10.7	-1.1%
Average aggressor # on 3D nets	285	200	-30%	253	-11%
Max noise on 3D nets (mV)	41.3	30.40	-26%	38.8	-6.1%

Y.Peng, T.Song, D.Petranovic, SK.Lim, **:"Full-Chip Inter-Die parasitic Extraction in Face-to-Face-Bonded 3D ICs**" Proc. ICCAD 2015, November 2015. ,pp 649-655.

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Impact on Clock Tree and Technology Scaling

- Inter-die coupling has large impact on clock tree, especially on top layer routing



	DBD	Holi	Δ%
Clock delay (ns)	1.02	1.16	**13.7%**
Clock transition (ns)	0.83	0.96	**15.7%**
Clock skew (ns)	0.54	0.59	**9.3%**
Switching power (W)	0.17	0.17	0.4%
Total power (W)	0.33	0.33	0.2%
Worst-case noise (V)	0.48	0.47	-2.1%
WNS (ns)	-0.07	-0.05	

- Die-to-die distance scaling keeps inter-die coupling similar across technology nodes

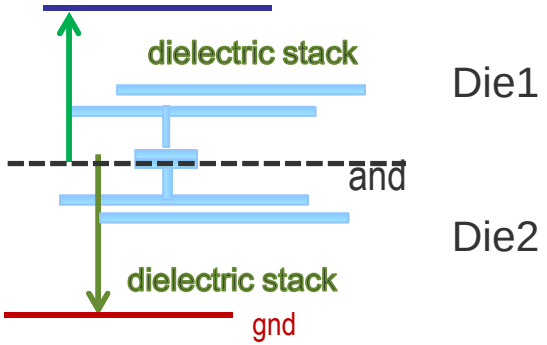
Node	28nm	14nm	7nm
Fin Pitch	-	0.04	0.036
Poly and M1 Pitch	0.116	0.064	0.054
M6 spacing/width	0.05/0.05	0.036/0.028	0.02/0.02
F2F via size/spacing	0.5/2.0	0.25/1.0	0.13/0.5
Pessimistic D2D distance	1.0	0.7	0.5
Optimistic D2D distance	0.7	0.5	0.35

	28nm	14nm	7nm
Die-to-die distance (μm)	1.00	0.50	0.35
LDPC inter-die coupling (pF)	208.3	59.3	37.4
LDPC intra-die coupling (pF)	8.10	1.99	1.45
LDPC intra-die coupling %	3.74%	3.25%	3.73%
T2 inter-die coupling (pF)	621.2	256.7	191.0
T2 intra-die coupling (pF)	18.9	14.9	5.55
T2 intra-die coupling %	2.95%	5.49%	2.82%

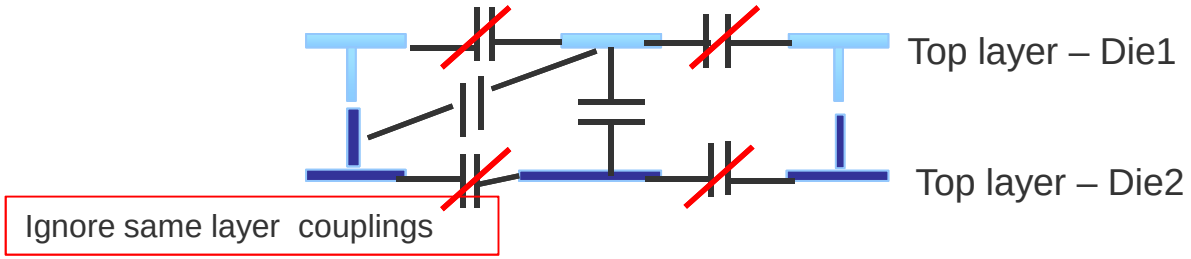
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In-Context Parasitic Extraction : Comments

- "In-Context" extraction is accurate.
- Extracting interface only is less accurate but simpler, if netlist of the dies already available
- "in-Context" can be reduced to "Interfaced In-context"
- Top layers from the dies to be included in the interface MIPT generated by xCalibrate
- Interface rules will be generated for extraction
- Generation of additional LVS statements for interface extraction will be done by 3DSTACK



- Ignore same layer couplings when extracting in interface since those are extracted in individual dies



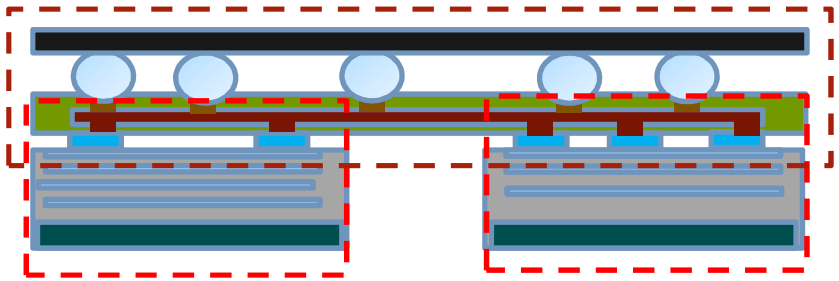
- **Note:** The dies top layer capacitances, are not accurate if no in-context extraction is used, since ,when the dies are extracted individually, no impact of the other die is taken into account.
- ***The flow is general and can be applied for digital, analog or mixed stacked dies***

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FOWLP Parasitic Extraction

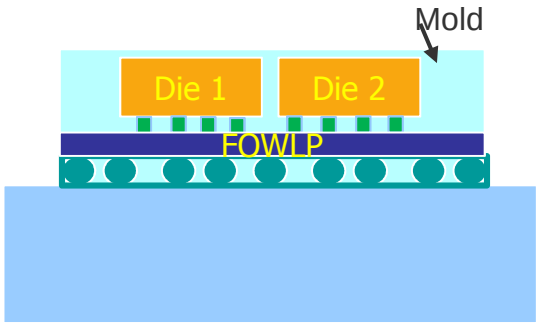
- Is there significant interaction between the die and package ?
- Is there any inductive interaction/impact?
- What tool should be used for extraction of the interface and die-package interaction?
  - Board/package tools have complexity/run-time issue
  - IC tools might not be accurate enough

- "In Context" Extraction Methodology



- Extract the dies "in context"
- Extract the package "in context" assuming that the dies are ground plates
- Netlisting

FOWLP

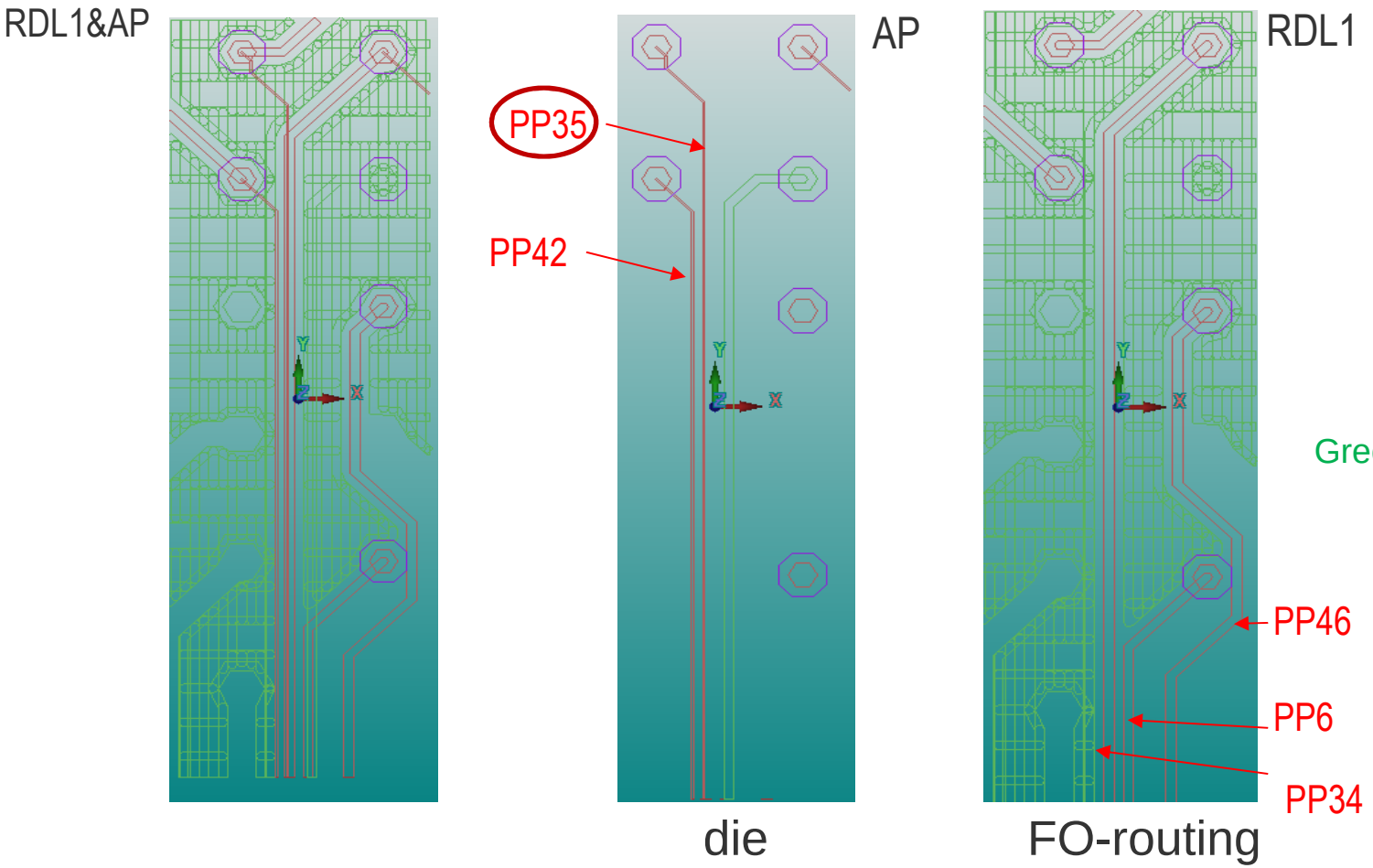


- Better Electrical Performance
  - No bumps, wire-bonds and substrate
  - Shorter interconnects
  - Fine Line Width/Space;
  - Finer pad pitch on die
- Thin package, Smaller Form Factor
- High integration
- Potential SiP, Multi-die, 3D Solution
- Heterogeneous chips + passives

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Coupling noise analysis: Mentor-Georgia Tech

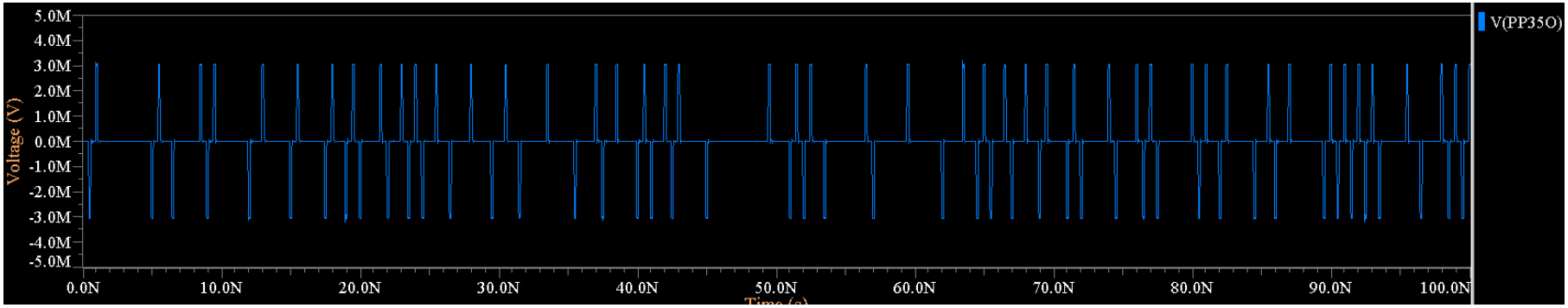
- PP35 and PP42 are on the AP layer (die) and PP6,46,34 on the RDL1



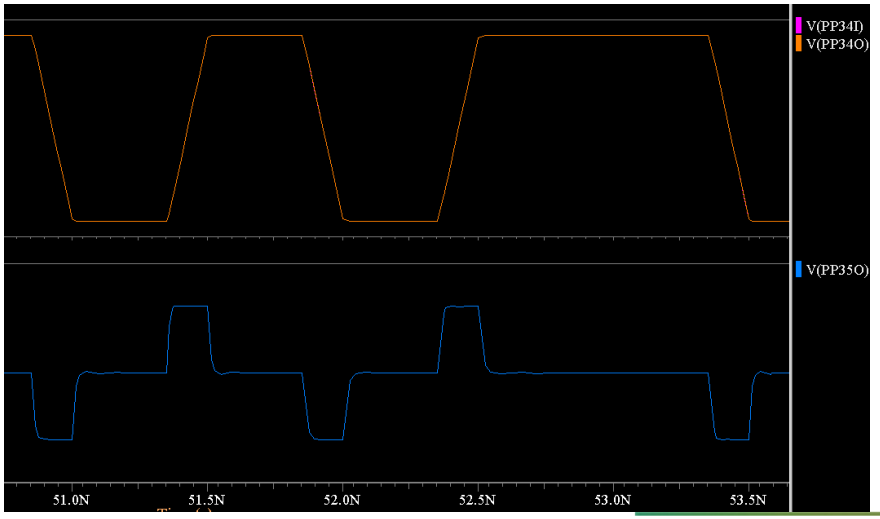
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Capacitive Coupling Noise (With RDL1 layer, RC)

- PP35 as victim, all other 4 nets as aggressor
- No inductive coupling;



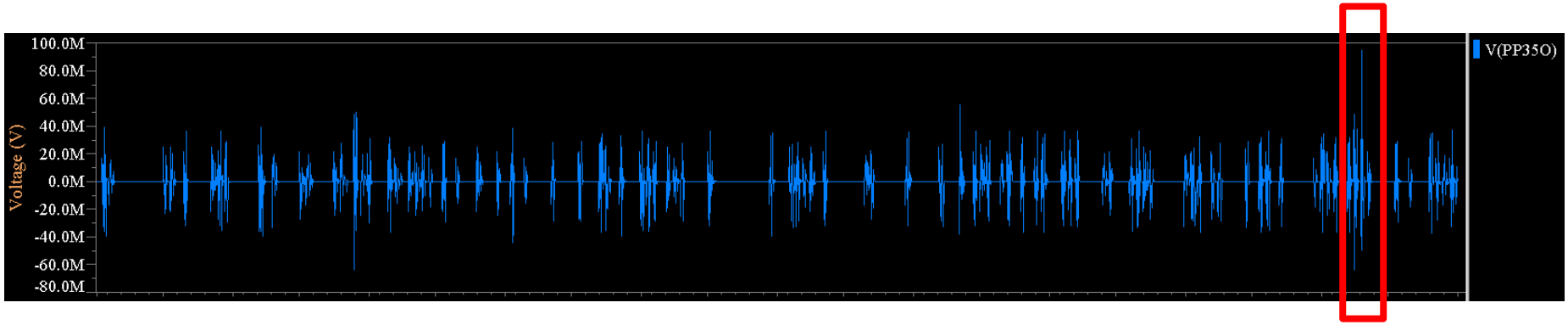
Peak noise:
3mV

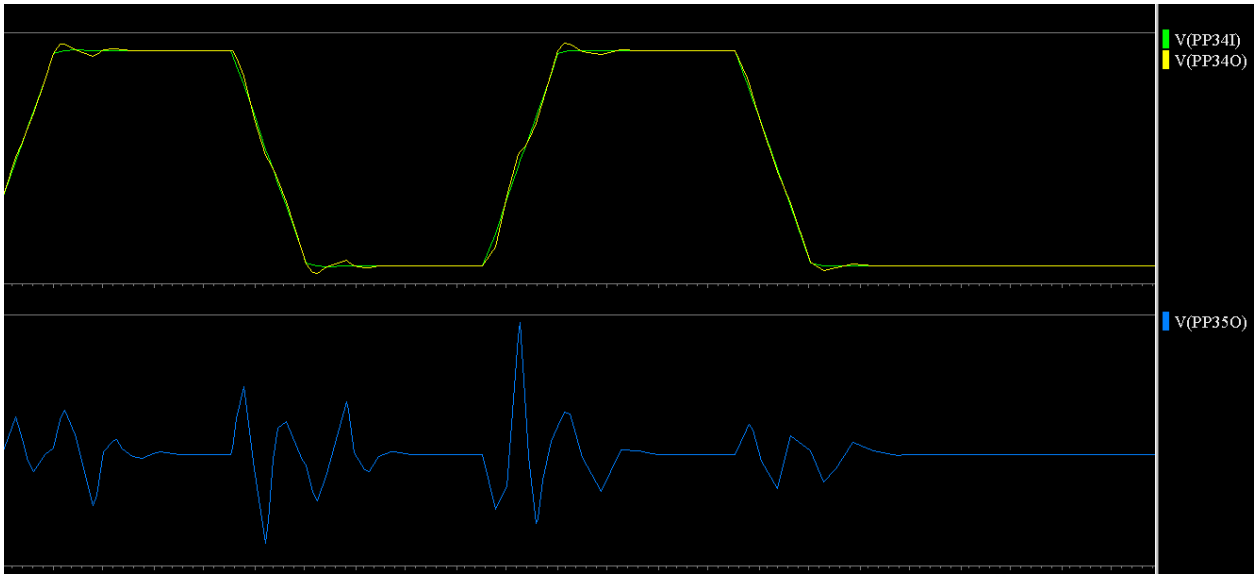


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Total Coupling Noise (With RDL1 layer, RCLK)

- PP35 as victim, all other 4 nets as aggressor, 2GHz random input



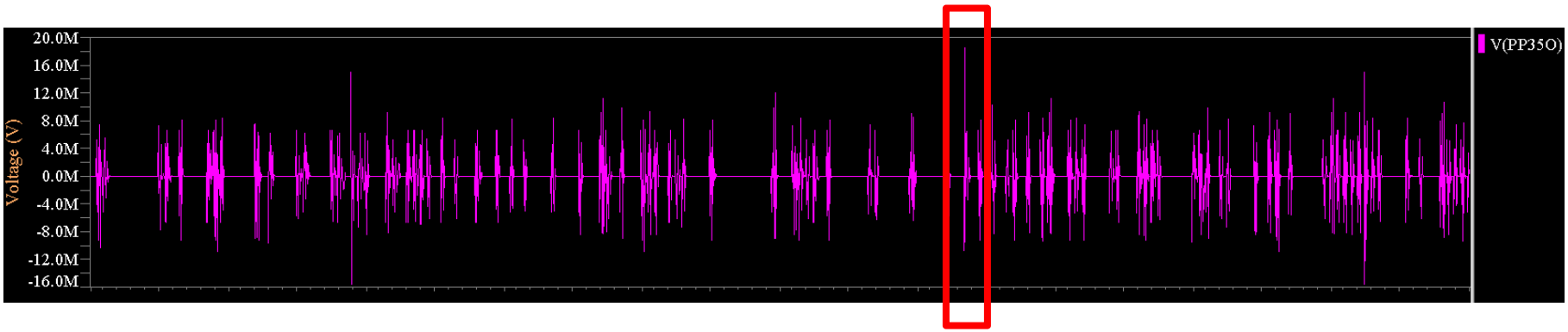


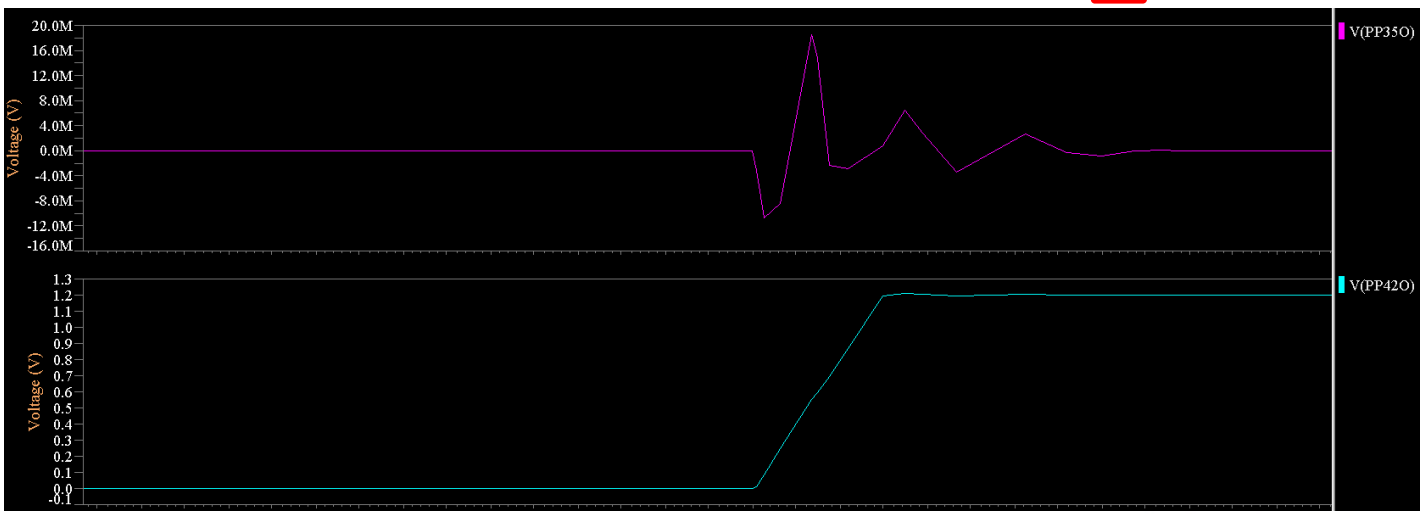
Peak noise:
94mV

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Coupling Noise (Without InFO)

- PP35 as victim, only PP42 as aggressor, No other signals (PP6,46,34)





Peak noise:
19mV

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Summary

- 3D stacking is reality
  - Lot of recent activities
  - Various configurations, strategies and business models
- There is need for accurate TSV modeling, including substrate and interactions
  - Various solution proposed: stand-alone TSV, parametrized models, …
  - Mentor's field solver based extraction: accurate and fast
- Chip interface and interaction modeling is now being considered
  - Fast inter-die links
  - Interface description and parasitic extraction
  - System level netlisting and simulation
- Collaborative partnerships are crucial
  - Design House – EDA - Foundry - Academia
  - Early cooperation eliminates redundant efforts and improves TTM
  - Results in timely, differentiating solutions

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