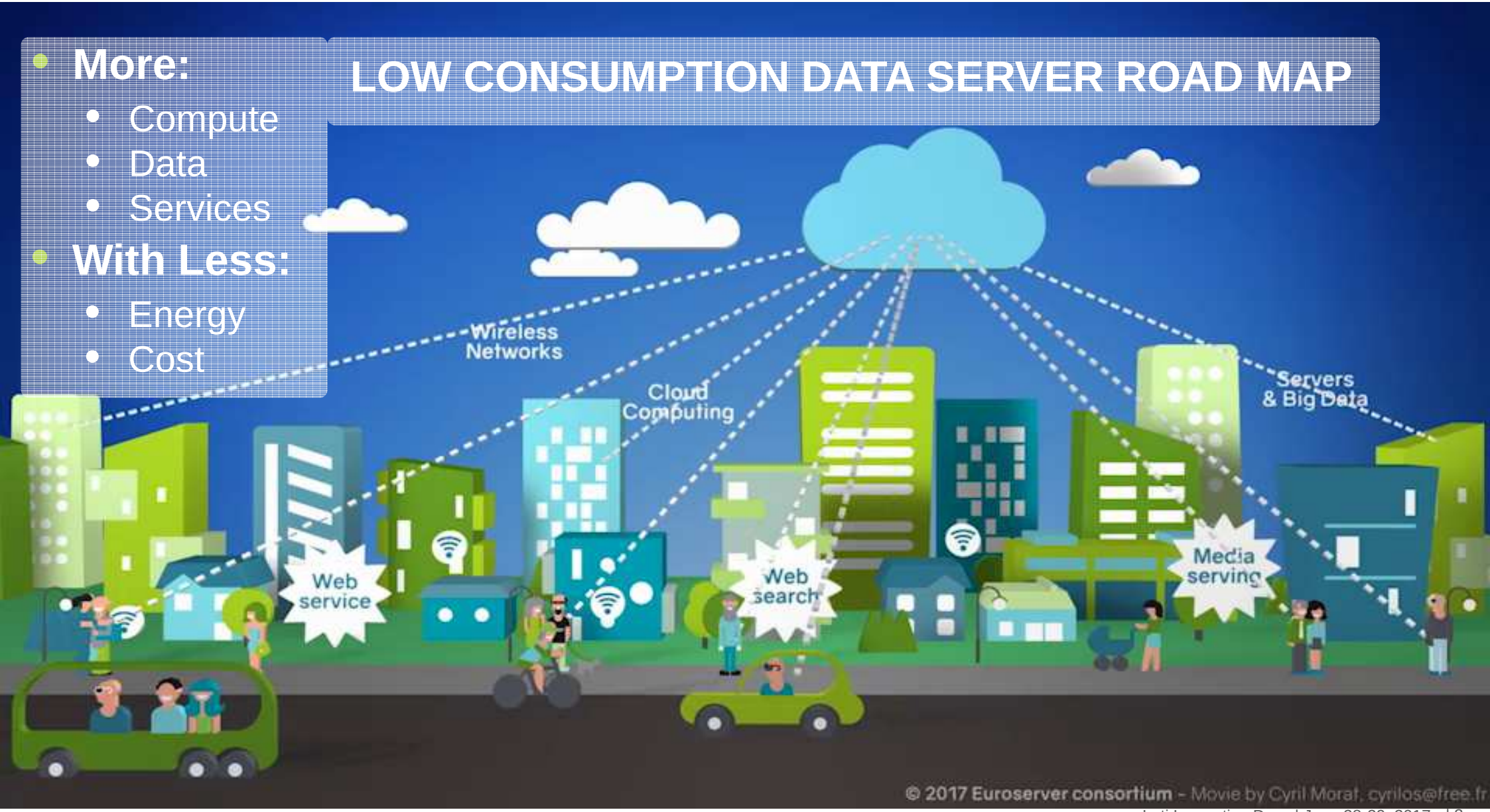


LOW CONSUMPTION DATA SERVER ROAD MAP

Leti Innovation Days | June 28-29, 2017

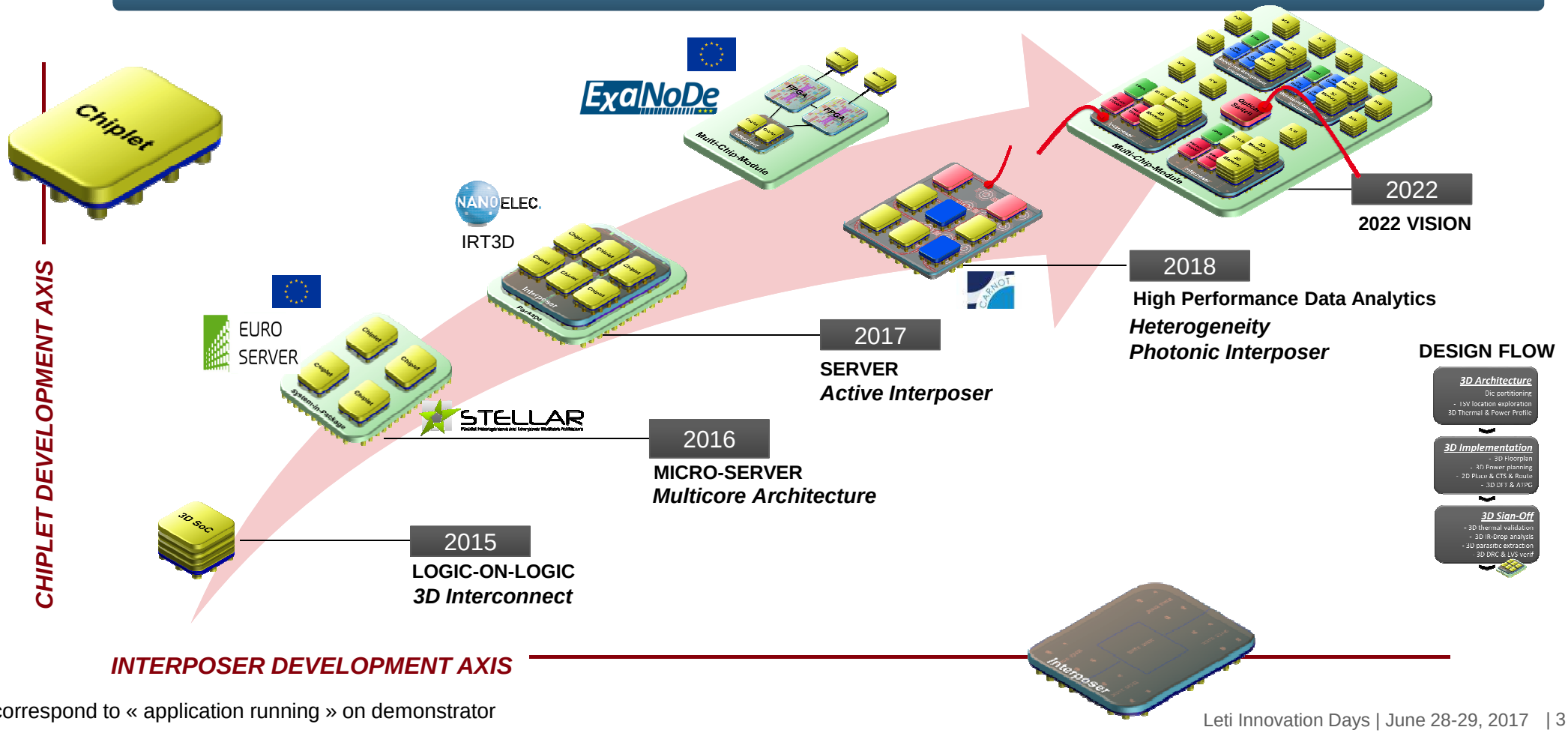
LOW CONSUMPTION DATA SERVER ROAD MAP

- **More:**
  - Compute
  - Data
  - Services
- **With Less:**
  - Energy
  - Cost



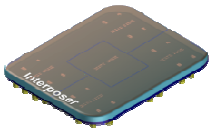
ROUTE TO LOW CONSUMPTION DATA SERVER

Leti's roadmap towards energy and cost efficient computing architectures



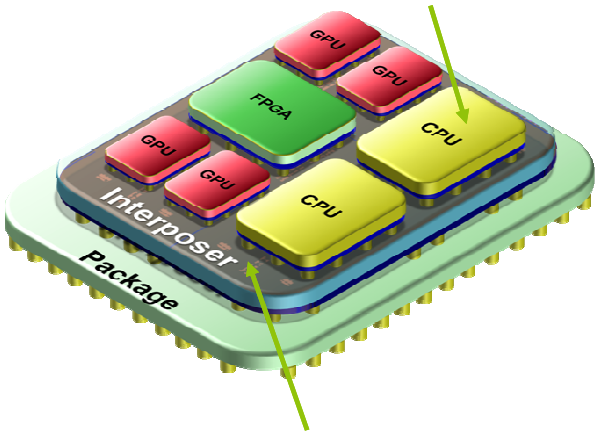
Years correspond to « application running » on demonstrator

LETI'S APPROACH FOR EFFICIENT DATA CENTERS

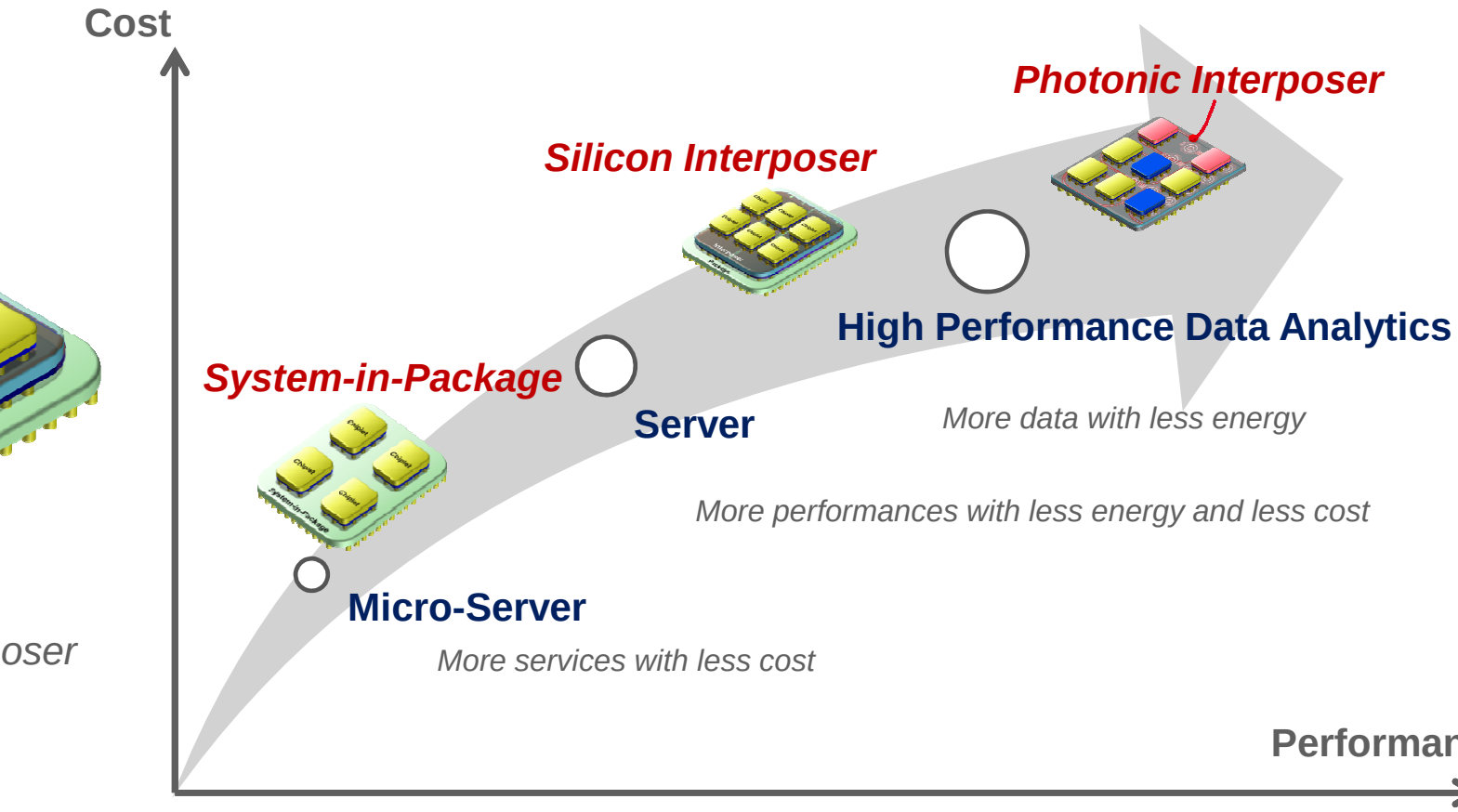


Co-design between architecture and integration technologies

Chiplet reuse

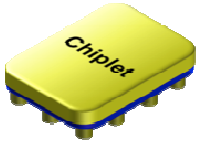


Application specific interposer

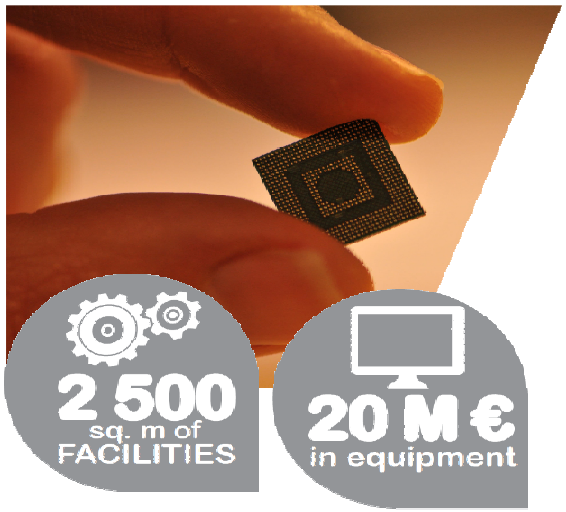


See demo

MANYCORE COMPUTING WITH CHIPLETS



System-on-Chip Design & Test Platform



- **Equipment**
  - Design tools
  - Test tools
- **Skills**
  - Highly complex digital IC and 3D-IC design
  - Advanced simulation & emulation
  - Application demonstrator & prototype
- **Strengths**
  - Data processing and 3D integration
  - From design to prototype



DESIGN FLOW



➡ Many EDA challenges met with our partners for the last 7 years

ATRENTA — *Common Lab*

SYNOPSYS — *Common Lab*

DOCEA POWER — *Common Lab*

intel — *Common Lab*

cadence — *No collaboration*

Mentor Graphics — *IRT Nanoelec open 3D Program*

Mentor Graphics — *IRT Nanoelec open 3D Program*

ANSYS — *No collaboration*

3D Architecture

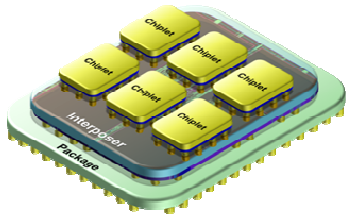
- Die partitioning
- TSV location exploration
- 3D thermal & power profile

3D Implementation

- 3D floorplan
- 3D power planning
- 2D place & CTS & route
- 3D DFT & ATPG

3D Sign-Off

- 3D thermal validation
- 3D IR-drop analysis
- 3D parasitic extraction
- 3D DRC & LVS verif



CAD tools challenges:

- *Handle complexity*
- *From system level down to implementation*
- *Strong coordination with existing tools and standards*

Si

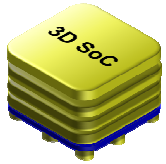
3D P1838

JEDEC

➔ ***EDA need to start 3-4 years before design …***

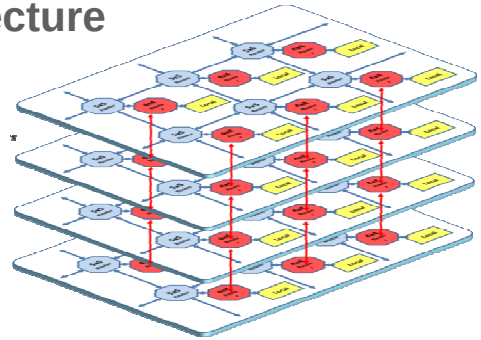
LOGIC-ON-LOGIC WITH 3D INTERCONNECTS

ISSCC'2016



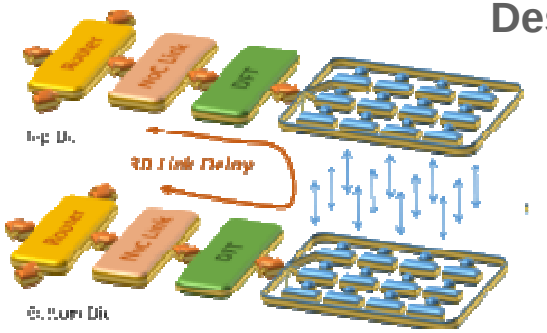
➡ Power efficient 3D interconnect, a first step towards 3D-based computing architectures

Architecture



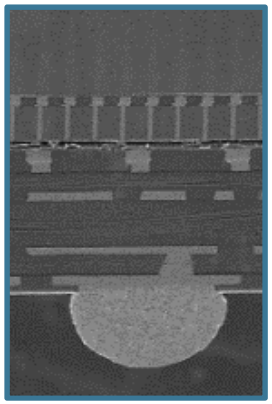
3D Network-on-Chip:
- *heterogeneous and homogenous multi-cores*

Design



3D Plug:
- *High throughput*
- *Low latency*
- *DFT*

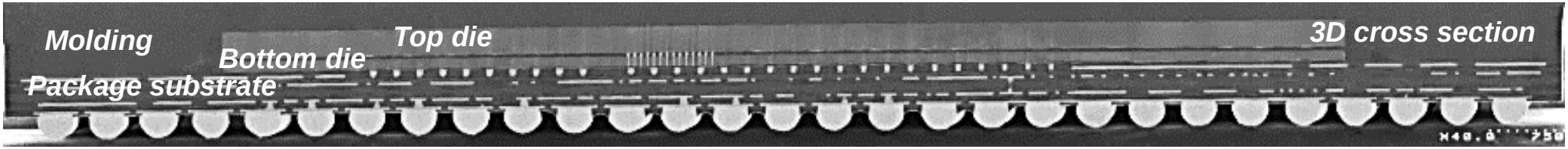
Technology



TSV middle (AR 1:8), µ-bumps, 50µm x 40µm pitch Face2Back stacking, Die2Die assembly

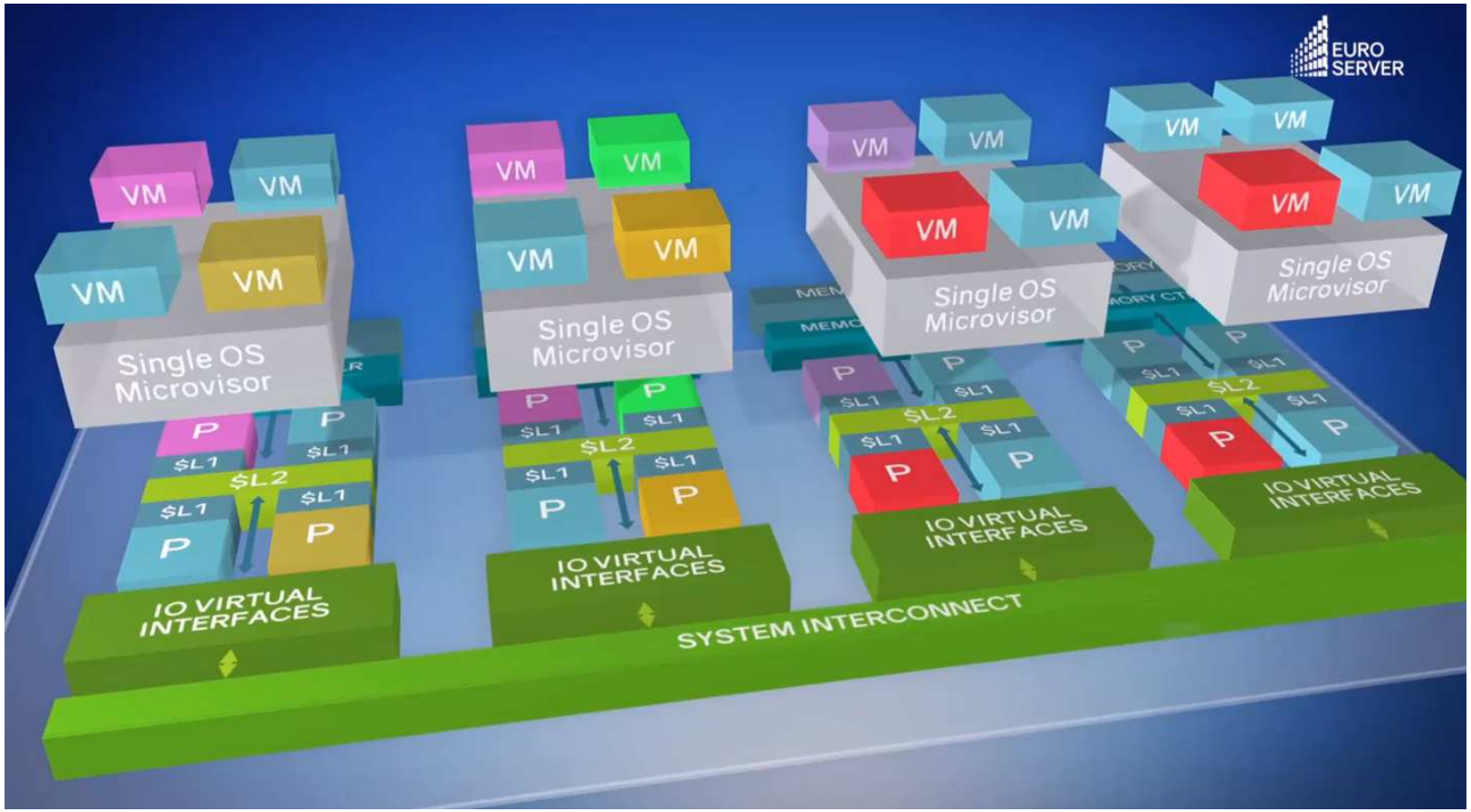
Demonstrator *3D NoC – 0.32 pJ/b*

See demo



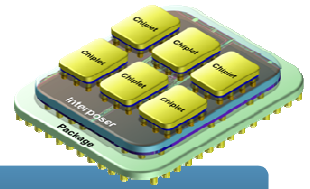
ARCHITECTURE PARTITIONING FOR MICRO-SERVERS

European ecosystem for scalable, low-power and low-cost approach to computing



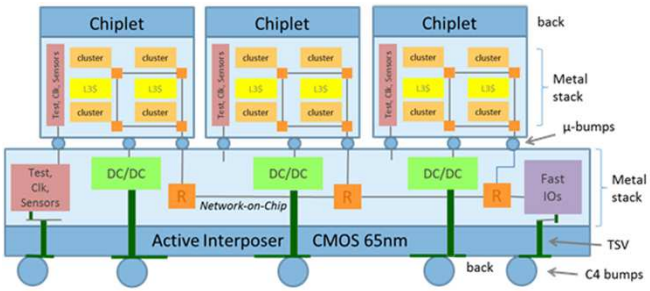
ACTIVE INTERPOSER FOR COMPUTING

Symposium'2016
3DIC'2015
ISVLSI'2015



96 cores compute fabric with 6 chiplets stacked on an active interposer

System Architecture



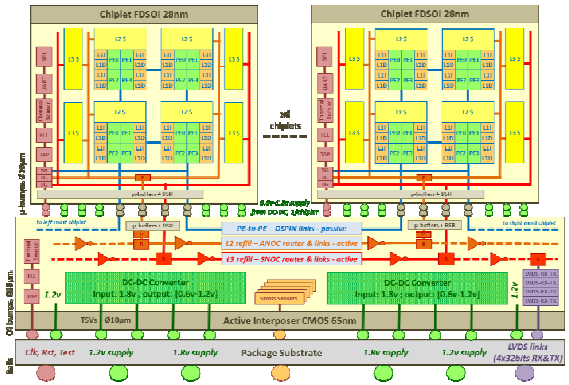
Cache Coherent Compute Fabric with:

- *96 cores (MIPS32),*
- *3 levels of caches,*
- *integrated power management*

Performance targets

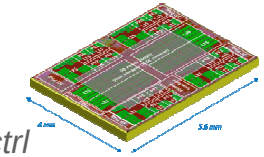
- 100 GOPS
- 10 GOPS/Watt
- 25 Watts total

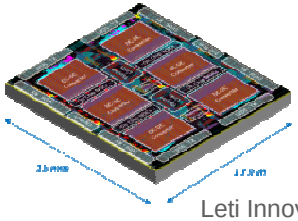
Design



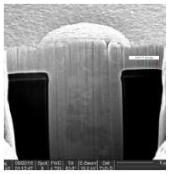
Heterogeneous 3D partitioning with:

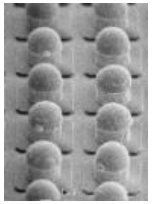
- *28nm FDSOI chiplets (x6)*
  - *Low power compute fabric*
  - *Wide voltage range (0.6V – 1.2V)*
  - *Body biasing for logic boost & leakage ctrl*
- *65nm active interposer*
  - *Power unit (Switched Cap DC-DC conv.)*
  - *Interconnect (Network-on-Chip)*
  - *Test, clocking, thermal sensors, etc*





Technology



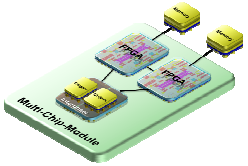


TSV
Ø 10µm
Height 100µm

µ-bumps
Ø 10 µm
Pitch 20 µm

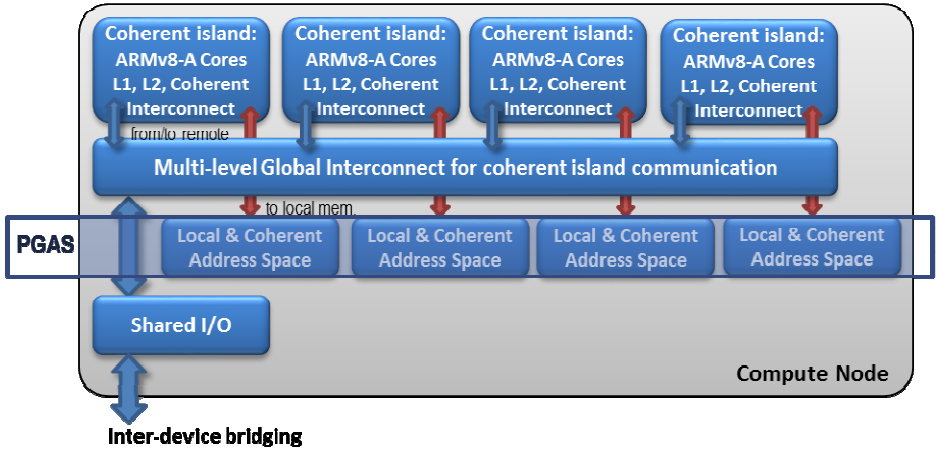
HETEROGENEITY FOR HIGH PERFORMANCE COMPUTING

DSD'2017



Communication blocks and advanced packaging for exascale computing

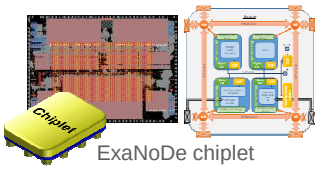
System Architecture



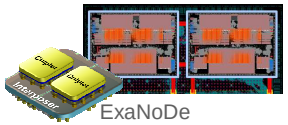
Partitioned Global Address Space:

- *ARMv8 cores,*
- *Coherent islands,*
- *FPGA support,*
- *Multi-level global interconnect.*

Design



ExaNoDe chiplet

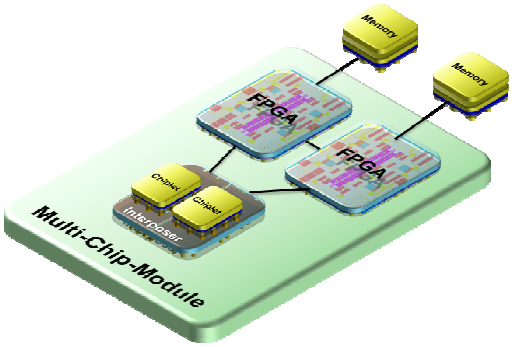


ExaNoDe
3D Integrated Circuit

3D Integrated Circuit:

- *Chiplet design with communication infrastructure and HW accelerators.*
- *Interposer design with FPGA interface.*

Technology



Integrated prototype:

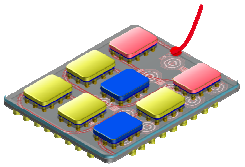
- *3D integration with active silicon interposer and chiplets*
- *Multi-Chip-Module integration for bare dies*

ExaNoDe

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

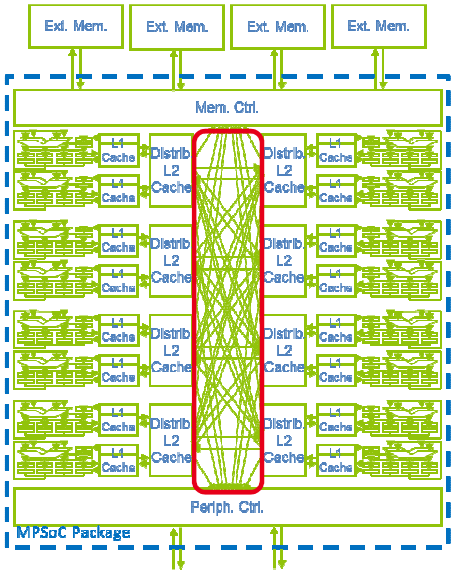
OPTICAL NETWORK-IN-PACKAGE

NOCS'2015



➡ Optical network-in-package to interconnect microprocessors and memories

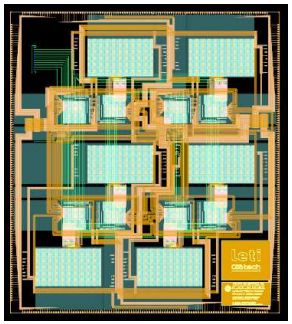
System Architecture

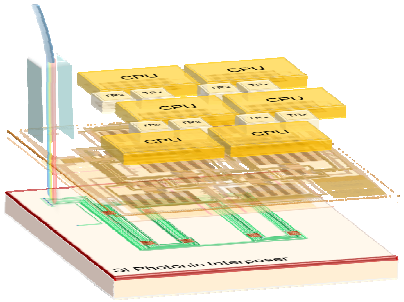


Cache Coherent Compute Fabric with:

- *96 cores (MIPS32),*
- *Optical NoC.*

Design



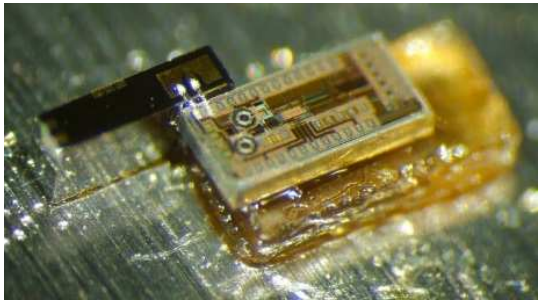


Demonstrator with 6 chiplets, 96 cores, 8 transceivers planned for 2018.
Design challenges:

- *Thermal control of WDM devices*
- *High-density high-performance integration*
- *E/O co-design of drivers*
- *Optimized short-range optical WDM system*

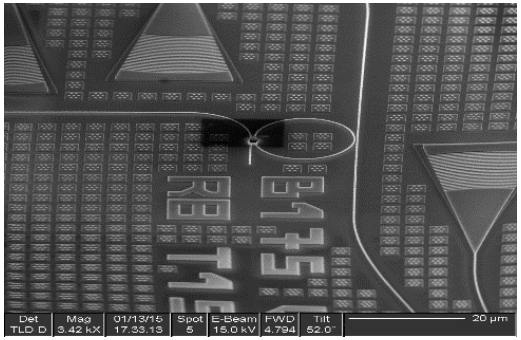
INSTITUT CARNOT CEA LETI

Technology

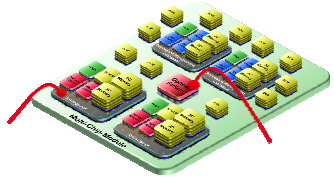


Preliminary integration of E/O transceiver and photo-diode

Photonic interposer

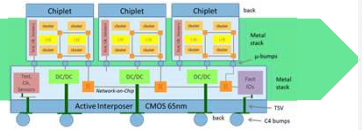


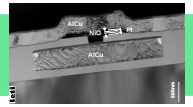
VISION

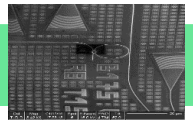


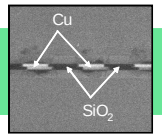
Heterogeneity & everything close

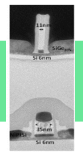
- Advanced Architectures
- Advanced CMOS: Scaling
- Photonic
- High Density 3D
- CoolCube™
- New Memory Technologies
- Neuromorphic

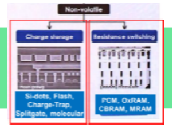














SW tools, benchmarks, co-design and design methodologies

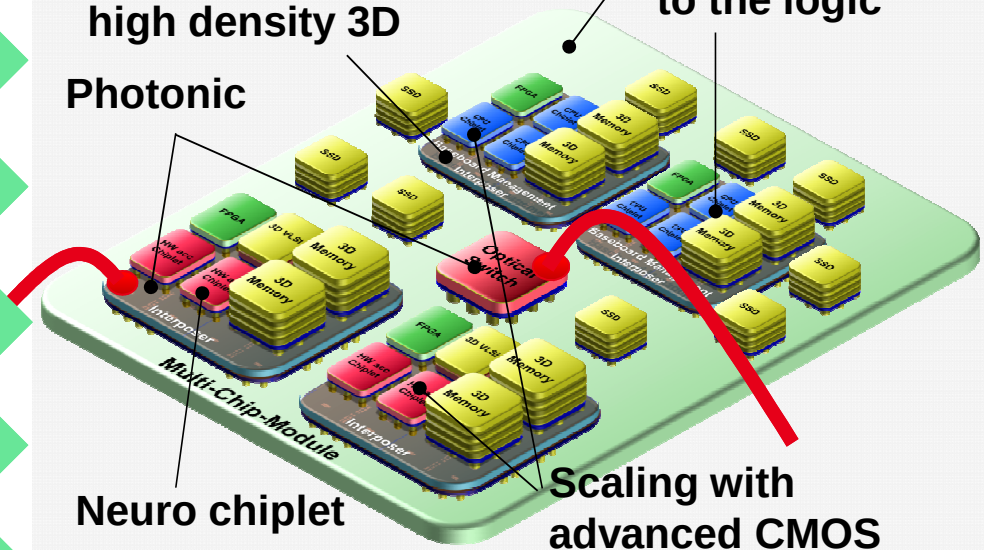
Active silicon interposer, high density 3D

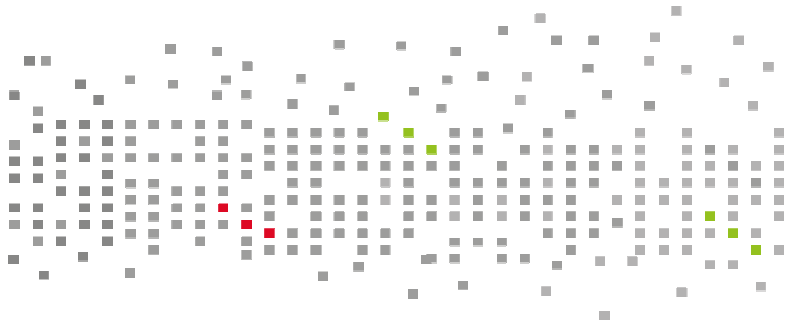
Memory close to the logic

Photonic

Neuro chiplet

Scaling with advanced CMOS and CoolCube™





Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
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PLANCHE DE PICTOS

