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SILICON TECHNOLOGIES AND COMPONENTS

2019

SCIENTIFIC
REPORT

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TECHNOLOGY
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COMMITTED TO INNOVATION, CEA-Leti CREATES DIFFERENTIATING SOLUTIONS WITH ITS PARTNERS.

CEA-Leti is a research institute of CEA Tech and a recognized global leader in miniaturization technologies.

CEA-Leti's teams are focused on developing secure solutions that will enable future information and communication technologies, health and wellness approaches, clean and safe energy production and recovery, sustainable transport, space exploration and cybersecurity.

For 50 years, the institute has built long term relationships with its industrial partners, tailoring innovative and differentiating solutions to their needs. Its entrepreneurship programs have sparked the creation of 65 start-ups.

CEA-Leti and its industrial partners work together through bilateral projects, joint laboratories and collaborative research programs, as illustrated in this report.

CEA-Leti maintains an excellent scientific level by working with the best research teams worldwide, establishing partnerships with major research technology organizations and academic institutions. CEA-Leti is also a member of the French Carnot Institutes network*.

*Carnot Institutes network: French network of 39 institutes serving innovation in industry.

DE LA RECHERCHE À L'INDUSTRIE

CEA Tech is the technology research branch of the French Alternative Energies and Atomic Energy Commission (CEA), a key player in research, development and innovation in defense & security, nuclear energy, technological research for industry and fundamental physical and life sciences.

www.cea.fr/english

CEA-Leti at a glance

800
publications per year

ISO 9001
certified since 2000

114
European projects

Founded in
1967

Based in
France (Grenoble)
with offices in the
US (San Francisco) and
Japan (Tokyo)

300
industrial partners

1,850
researchers

3,100
patents in portfolio

10,000
sq. meters cleanroom
100-200-300 mm wafers

65
startups created

SILICON TECHNOLOGIES AND COMPONENTS

Within CEA Tech and Leti, silicon technologies and components research activities are shared between two divisions gathering together around 600 researchers:

The Technology Platform Division carries out innovative process engineering, materials research and development as well as advanced nano-characterization. It operates 24/6 year round, and has 1100 m^2 of state-of-the-art cleanroom space divided into four different technology platforms. 2019 saw the addition of the fourth platform dedicated to photonics.

The Silicon Components Division carries out research on nanoelectronics and heterogeneous integration on silicon and is focusing on two mains areas: on-going shrinking of CMOS devices to extend Moore's Law for faster, less-expensive computing power, and the integration of new capabilities into CMOS, such as sensors, power devices, imaging technology, and new types of memory, to enable new applications.

This booklet contains 48 one-page research summaries covering advances in the focus areas of our Silicon Devices and Technologies Divisions, highlighting new results obtained during the year 2019.

Technological Platforms

The silicon divisions operate 11000 m² of state-of-the-art cleanroom space divided into three platforms, gathering 700 process tools and a combined staff of more than 520; they run industry-like operations, 24 hours a day, 6 days a week, all year round.

1. The Nanotech200&300 platform provides 200mm and 300mm CMOS wafer processing, which can be applied to both semiconductor and microsystem devices.

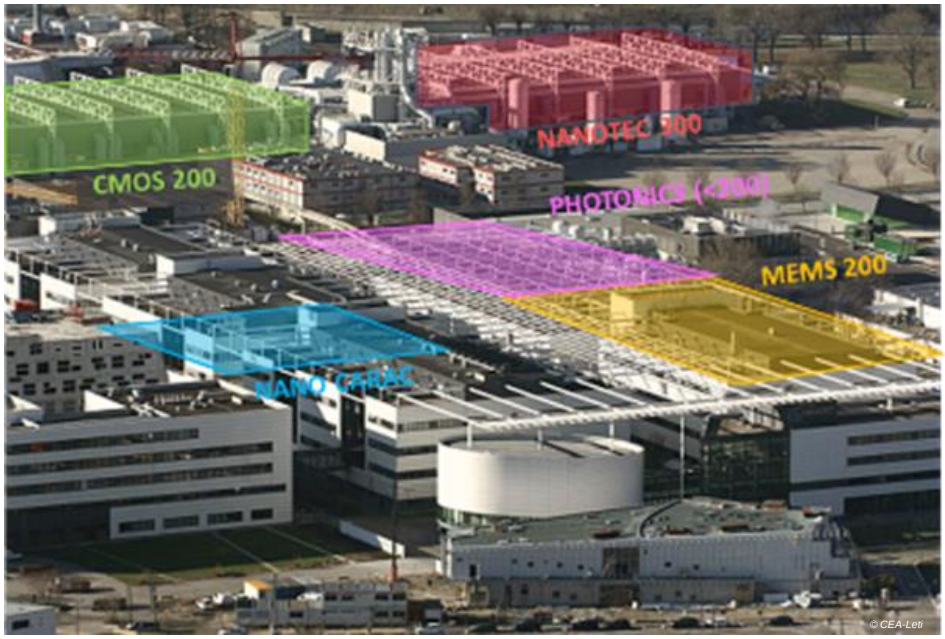
2. The MEMS200 platform produces non-CMOS Micro-ElectroMechanical Systems (MEMS).

Both platforms are focused on the More than Moore initiative to develop new semiconductor capabilities. An innovative cleanroom shuttle system links the two platforms to add process flexibility and faster processing.

3. The 3D Integration platform aims to integrate various microelectronics objects together in order to juxtapose complementary functions, such as sensing, storing, processing, actuation, communication and energy scavenging. This provides advanced system solutions in three dimensions. This line is open to our customers for prototyping through the Open3D service.

4. The fourth platform that was recently added is dedicated to photonics. It covers conception, III-V and II-VI semiconductor technology fabrication and packaging capability. Applications as diverse as lighting, micro-screens, visible and infrared detectors and devices for astrophysics …

All research carried out in our cleanrooms benefits from the Nano-Characterization Platform, which is located on the MINATEC campus. This platform, unique in Europe, covers eight domains of competencies, including electron microscopy, X-ray diffraction, ion beam analysis, optics, scanning probe, surface analysis and sample preparation, magnetic resonance.



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EDITORIAL

Laurent Clavelier

Head of Technological platforms

SILICON TECHNOLOGIES AND COMPONENTS

Writing an editorial for the 2019 scientific report in the midst of the COVID-19 crisis obliges us to consider our results in a new light and confirms the pertinence of many of our choices over the past years. These strategic orientations can only succeed because of the constant effort to maintain our more basic research activities (number of PhD subjects on offer, participation in ANR or CARNOT projects,…), in collaboration with national academic partners (in particular our work with the LTM, the CREHA, the Néel institute, ….), European partners (we have strengthened our links with the Fraunhofer Group and IMEC, but also with members of the HTA). This is the message that we have endeavored to convey with this scientific report.

In this period of confinement and social distancing, remote working has become the new norm. This has amplified the importance of digital technology in our daily lives. A striking example of the importance of the digital transition. We are addressing the fundamental side of this transition through our work on CMOS, quantum computing, advanced SOI substrates, new generation memories for AI, pattering, circuits for datacom, …Our results on the fundamental principles and the basic building blocks of the Smart-Cut™ process(fracture and bonding within the framework of the collaboration with SOITEC), Cool-Cube technology (CMP, bonding and low temperature epitaxy, …), new generations of filters for 5G(LNO and LTO but also SOI with integrated trapping layers), circuits mixing III-V materials and silicon technology (“Si-like” contacts on GaAs and InO, III-V technology on silicon with our start up SCINTIL, …), embedded memory (PCRAM with ST, TEMPO European project, …), …are closely tied to this transition and reflect an important scientific effort and the capacity to transform a proof-of-concept to an industrial product. This unique positioning between fundamental scientific research and industrial technology transfer is only possible in conjunction with a major investment program, an important part of which are the joint development programs with major industrial tool suppliers (AMAT, SCREEN, ASML, TEL, SET, .ENTEGRIS, FOGALE, EVG, …) that generate cutting edge scientific results that are valorized by patents and publications.

This period of crisis heightens the importance of energy efficiency in particular the transition towards electrified means of transport with the vast majority of carmakers announcing plans for electric vehicles. For several years now, our work on GaN power electronics, supported by our “conveyor belt” approach, place us at the forefront of scientific developments in this field (ALE etching, correlation of different characterization techniques, …). Recently we have completed our technology portfolio with our work on SiC with SOITEC and AMAT that will certainly lead to valuable scientific insights in the future

The year 2019 was also abundant in terms of scientific results on light emitting and detecting devices. Our work on micro-LEDs with a large international company (2D LEDs) and our start-up ALEDIA (3D LEDs) have generated state-of-the-art results in CMP, etching, nanoimprint lithography, … In terms of visible imagers with ST, our scientific results on micro-lenses and the triptych of simulation-technology-characterization deserve to be highlighted as well as our fundamental studies to accompany the transition to 100 mm of CdZnTe infrared technology with LYNRED.
I hope that you will enjoy reading the 2019 DPFT-DCOS scientific report

Laurent CLAVELIER

EDITORIAL

SILICON TECHNOLOGIES AND COMPONENTS

Olivier Faynot

Head of Silicon Components Division

Dear Reader,

The Silicon Components Division is at the heart of many societal issues, among the main ones we can mention wellness, mobility, communications with smart, green, efficient transportations, secure and energy efficient communications. These demands are driving the technological developments of silicon technologies, broadly relying upon state-of-the-art 300 and 200 mm facilities, as well as state-of-the-art characterization platforms, enabling us to understand and model the behavior and the benefit of such technologies.

Transversality and multi-disciplinarity are key today within CEA-Leti, in order to ensure high quality offers, from material to system (something we have been doing formany years in the GaN/Si Power program with ST Microelectronics).

DCOS is driving two of the four strategic programs defined for a long term structuring of CEA-Leti's activities: embedded Artificial Intelligence and Quantum Computing.

Let me now highlight a few of the main successes achieved in 2019:

- Significant progresses in resistive-RAM and associated selectors, either in support of ST in its manufacturing process, with key developments using Immersion lithography or in perspective of disruptive computing approaches.
- Validation of the integration flow of Silicon based quantum devices and associated packaging, with multi QBits structures, opening the door to 2 QBits based gate operation.
- Demonstration of RF GaN/Si amplification transistors with optimized epitaxial layer, complementing our RF activities that covers from Substrate engineering to tunable SAW/BAW filters, targeting 5G requirements.
- Many breaking news on 3D integration: Demonstration of sub 500°C process for sequential integration, as well as the demonstration of multicore chiplet integration using Silicon Interposer, with performances exceeding state-of-the-art reported performance at system level.
- Finally, we would like to bring your attention to our demonstrations of innovative MEMS/NEMS and more specifically to the promising design and fabrication of capacitive Backplate-less Microphones paving the way for reduced damping losses and ultra-high SNR (>75 dB(A)).

I would like to thank all the teams involved in these achievements and I hope you will enjoy reading the overview.

Olivier Faynot

SILICON TECHNOLOGIES AND COMPONENTS

EDITORIAL

Jean-Charles Barbé and Jean-Paul Barnes

Chief Scientists for the Silicon Components Division and the Technology Platforms Division

We are proud to share with you our tenth Silicon Technologies and Components Annual Scientific Research Report, for the year 2019. This report contains 48 one-page research highlights covering advances in the focus areas of our Silicon Components and Technology Platforms Divisions during the year.

2019 illustrates the perpetual renewal of innovation of our Silicon Divisions to meet societal challenges through industrializable hardware solutions in the fields of embedded artificial intelligence, Internet of Things (IOT), automotive, energy, health and environment monitoring.

In this annual report, we confirmed our positioning in disruptive silicon based research from emerging materials process development, to device scale integration and optimization, to demonstration at the architecture level. Beside several highlights including scalable QuBIT integration, emerging resistive memories integration for IMC and embedded AI, Chiplet-based 3D System Integration and opto-mechanic resonators, GeSn devices, power electronics and advances in 3D metrology and characterization we wish to draw your attention to new topics such as energy harvesting and process development and integration for opto-electronics.

In 2019, the Silicon Components and Technology Platforms Divisions produced 419 publications, achieving impact factors as high as 37.
We are committed to ensuring the transfer of the most advanced research to industry and, as such, the vast majority of our research is performed in close collaboration with our industrial and academic partners. We would like to take this opportunity to thank them for their continuing confidence in us. 2019 was the last year in the pre-COVID 19 era. In this period of uncertainty and change, the need to innovate will be accentuated. We will continue to work closely with our partners to accelerate innovation and bring advanced research to industrial maturity.

The strong presence of scientists from our divisions in major European research programs, European Research Council grants, international conferences, program committees, boards of governors and evaluation committees is a testament to our commitment to collaborative research in an international context.

These scientific achievements would not be possible without the hard work of all the researchers, support staff and management, of the Silicon Technologies and Silicon Components Divisions and CEA-LETI's scientific advisory board.

Last, but not least, we would like to express our gratitude to the editorial team and all the authors of the 2019 Scientific Report, who, despite the difficult conditions due to the global COVID-19 pandemic, ensured that the 2019 report was delivered on time to the same exacting standards as always.

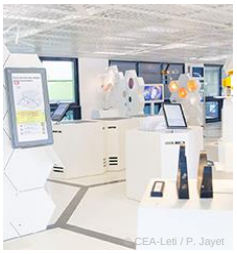
Jean-Charles Barbé and Jean-Paul Barnes

KEY FIGURES

498 researchers
135 industrial residents
147 PhD students in 2019
23 Post-docs in 2019

11000 m² of cleanrooms
24/6 operation
700 tools

3000 m² Nanocharacterization platform
50 advanced instruments
3 CEA institutes (LETI, LITEN, IRIG) working together



122 commun laboratories
129 patent filed in 2019
1342 patents in portfolio
419 Scientific communications in 2019

SCIENTIFIC ACTIVITY

Publications

180 publications in 2019 (WoS, SCOPUS, ACM)
239 international conference communications.

Prize and awards

3 on-going European Research Council Grants (S.Hentz, F. Andrieu, M. Vinet)

A-L Serra Best student paper award, 2019 IEEE Int. Mem. Workshop

G. Molas IEEE senior member

D. Bosch Best student paper award VLSI TSA 2019

P. Coudrain Best paper ECTC 2019

A. Ben Hadj Mabrouk, Excellent Presentation Award, SIMS 22 - Kyoto, Japan

A. Gomes de Carvalho, Biointerphases Award, SIMS 22 - Kyoto, Japan

CEA-Leti - Winners of the 2020 3D InCites Awards (Research Institute of the Year)

Experts

- 7 International Experts
- 4 Research Directors
- 38 Senior Experts
- 56 Experts
- 26 of them holding an HDR.

Scientific committees

- National Research Agency committee.
- Technical Program committees of:

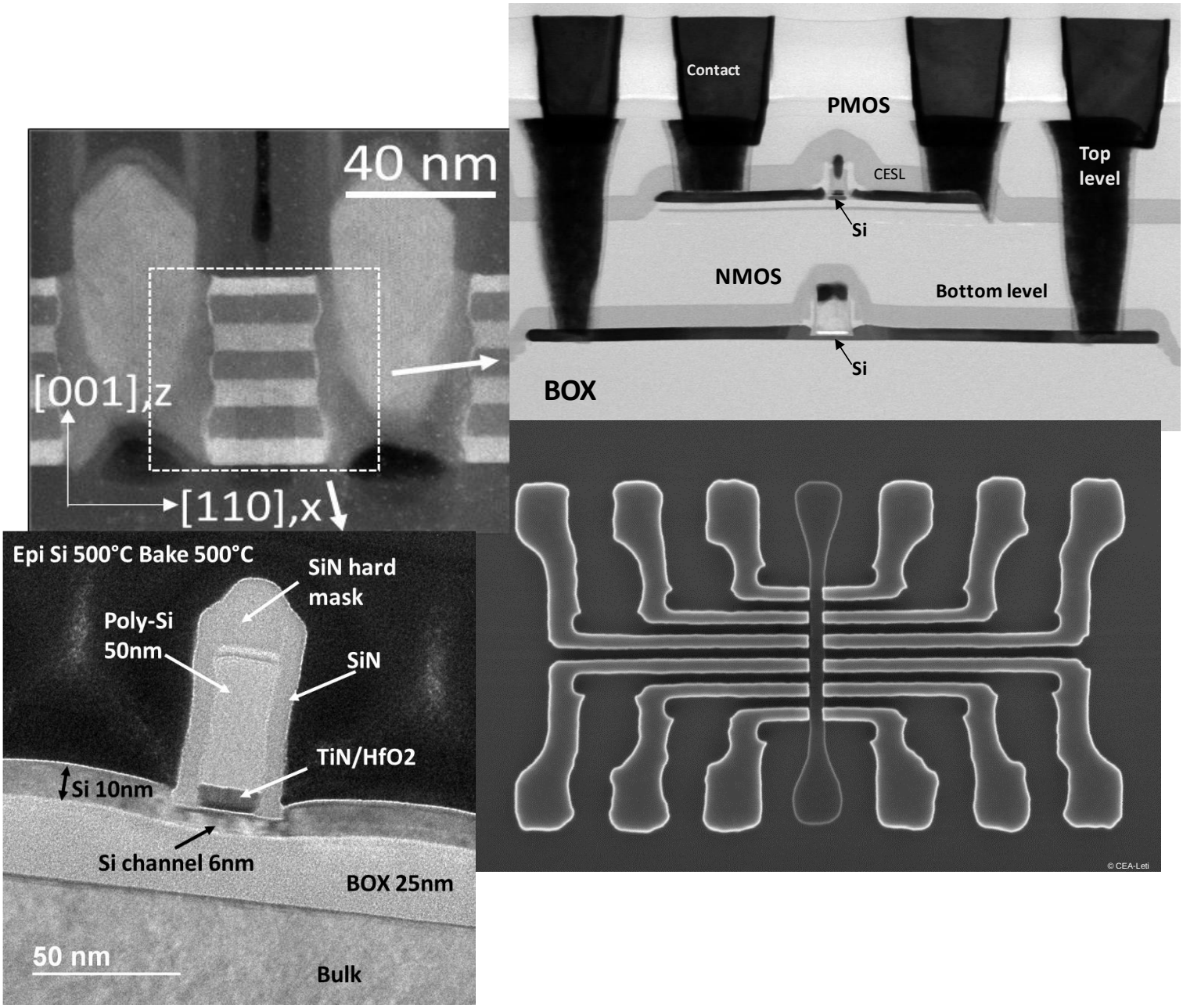
IEEE IEDM, IEEE VLSI Technology and Circuits, IEEE IRPS, IEEE TRANSDUCERS, IEEE IMW, IEEE ECTC, IEEE ESSDERC/ESSIRC, IEEE SISPAD, IEEE 3DIC,
AMC,
ICSI/ISTDM,
ECS Transactions AIMES,
JNTE, AVS,
SPIE Advanced Lithography,
FCMN, EMRS Spring,
MRS spring 2019, EPCOS 2019, RAFALD 2019, ICPT 2019, SPCC - 2019, 2nd Joint ISTDM / ICSI 2019, IITC/MAM 2019, European Atom Probe Workshop, European Phase-Change & Ovonic Symposium, European FIB Network Workshop.

Conferences and Workshops organizations

G03 SiGe Symposium at AIMES,
DSA Symposium,
PESM.

International Collaborations

Forschungs Zentrum Juelich (Germany),
Stanford University (USA),
Caltech (USA),
The University of California (USA),
Fraunhofer institutes (Germany),
Università degli Studi di Ferrara (Italy)
University of Cambridge (GB),
Université Catholique de Louvain (Belgium),
University of California at Berkeley (USA),
Politecnico Di Milano (Italy),
Paul Scherrer Institute (Switzerland),
École Polytechnique Fédérale de Lausanne (Switzerland), ETH – Zürich (Switzerland),
CNR (Italy),
University of Chicago (USA),
Sherbrooke, University (Canada)
NIMS (Japan), SPring-8 Synchrotron (Japan)
University of Southern Denmark
University Cagliari (Italy),
Institute for Technical Physics and Materials Science (Budapest),
Hungarian Academy of Sciences (Budapest),
Korea University (Seoul)
Centro universitario FEI (Brazil),
University of Tsukuba (Japan),
AIST (Japan),
Herzen University (St Petersburg, Russia).
IMEC, Leuven (Belgium), EMPA, Mons University (Belgium), University of Surrey (UK)
National Physical Laboratory, London (UK)
Elettra Synchrotron, Trieste (Italy)
NSLS-II, Brookhaven Nat. Lab. (USA)
Fondazione Bruno Kessler, Trento (Italy)
Physikalisch-Technische Bundesansalt, Berlin, Germany.
Varsaw University, IHPP (Poland)


40 nm
[001],z
[110],x
Contact
PMOS
CESL
Top level
Si
NMOS
Bottom level
Si
BOX
Epi Si 500°C Bake 500°C
SiN hard mask
Poly-Si 50nm
SiN
TiN/HfO2
Si 10nm
Si channel 6nm
BOX 25nm
50 nm
Bulk
© CEA-Leti

01 CORE & BEYOND CMOS

- Integration and Readout of Electron and Hole Spin Quantum Bits in Silicon MOS Technology
- Thermal Bulk 5V MOSFET Stability and Low Temperature Gate Resistance for 3D CoolCubeTM Integration
- 3D Coolcube Integration for RF Applications
- Imaging, Modeling and Engineering of Strain in GAA Nanosheet Transistors
- RF-SOI Technology for Power Amplifier Solutions

Integration and Readout of Electron and Hole Spin Quantum Bits in Silicon MOS Technology

RESEARCH TOPIC:
Quantum information, spin qubits, silicon, CMOS

AUTHORS:
B. Bertrand, N. Rambal, H. Niebojewski, T. Bedecarrats, L. Hutin, C. Vizioz, P.-A. Mortemousque, R. Kies, M. Cassé, H. Jacquinot, G. Billiot, G. Pillonet, Y. Thonnart, M. Vinet (Y.-M. Niquet, A. Crippa, R. Maurand, X. Jehl, M. Sanquer, S. de Franceschi)[1],
(T. Meunier, M. Urdampilleta)[2]

We studied the potential of silicon spin qubits for the realization of scalable quantum information processors. With that aim, we fabricated devices made of multiple gates arranged along an SOI nanowire, in order to define a 2xN array of individually controllable Si quantum dots. Using this platform, we implemented two different readout schemes based on gate-reflectometry to either directly probe a spin-dependent quantum capacitance or detect spin-dependent charge movements with a single-shot precision. These results are of significant relevance regarding the prospect of reducing the qubit footprint and required number of gates – two major characteristics for scalable quantum computing architectures.

SCIENTIFIC COLLABORATIONS: [1]CEA-IRIG, [2]CNRS Institut Néel

Context and Challenges

Silicon spin qubits confined in quantum dot (QD) arrays have demonstrated excellent performances in terms of control fidelity and coherence time. However, several requirements towards a fault-tolerant and scalable platform remain unfulfilled, in particular because of the high number of control lines per qubit and the relatively demanding single-spin measurement procedures.

Achieving a direct single-spin detection remains indeed a huge experimental challenge. Current single-spin detection schemes rely on a spin–charge conversion via spin-selective tunneling or Pauli Spin Blockade (PSB) [1]. However, the detection of these tunneling events usually requires the integration of cumbersome charge sensors – either single-electron transistors (SETs) or quantum point contacts (QPCs) – as close as possible from the QDs, which significantly increases the complexity and footprint of the device layout. SETs or QPCs indeed consist in one or several gates together with two charge reservoirs biased by a voltage source.

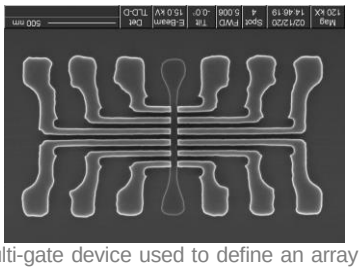


Figure 1: Multi-gate device used to define an array of nearest-neighbor-coupled spin qubits (one QD beneath each gate).

Main Results

The studied devices were multi-gate structures with only a single control line per qubit (Fig. 1). We demonstrated single-spin readout via a technique of gate reflectometry that enables charge sensing in the most compact way by directly measuring the QDs capacitances [2, 3]. When applying a radiofrequency pulse on the gate defining a QD, part of the signal is reflected with a magnitude and a phase that are determined by the QD effective capacitance. Spin readout is possible by the detection of a spin-dependent quantum capacitance emerging from Pauli Spin Blockade (PSB) in tunnel-coupled QDs.

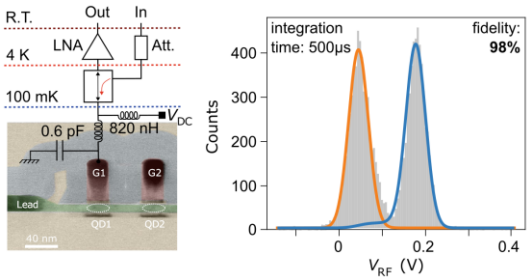


Figure 2: Reflectometry setup and single-shot readout results showing a fidelity above 98% over a 500 µs integration time.

Another demonstration [3, 4] of spin readout was made using "latched" Pauli Spin Blockade: in that case, PSB is used to induce a spin-dependent charge tunneling from an external reservoir. Using a similar gate-reflectometry procedure, we obtained a magnified detection signal that resulted in a high-fidelity single-shot spin readout (above 98%, see Fig. 2). Such reservoir-assisted readout remains compatible with large-scale arrays in the 3D-architecture we are developing.

Perspectives

These demonstrations are promising approaches towards the readout of large-scale QD arrays. In order to manage the readout of the whole array in a reasonable time (faster than the qubit coherence time), the next step will consist in the demonstration of parallel qubit readout by the multiplexing of several reflectometry signals.

RELATED PUBLICATIONS:
[1] T. Meunier, B. Bertrand et al., IEDM, (2019), https://doi.org/10.1109/IEDM19573.2019.8993534
[2] A. Crippa, R. Laviéville et al., Nature Communications (2019), https://doi.org/10.1038/s41467-019-10848-z
[3] L. Hutin et al., IEDM, (2019), https://doi.org/10.1109/IEDM19573.2019.8993580
[4] M. Urdampilleta, L. Hutin et al., Nature Nanotechnology, (2019), https://doi.org/10.1038/s41565-019-0443-9

Thermal Bulk 5V MOSFET Stability and Low Temperature Gate Resistance for 3D CoolCube™ Integration

RESEARCH TOPIC:

Low temperature FDSOI transistor applications, HV bulk transistor, 3D sequential integration, UV ns laser anneal

AUTHORS:

C. Fenouillet-Beranger, C. Cavalcante, P. Batude, L. Brunet, S. Kerdilès, P. Acosta-Alba, L. Brevard, X. Garros, M. Casse, J. Lacord, A.-S. Royet, N. Rambal, F. Andrieu, (G. Ghibaudo)[1]

For the first time, the thermal stability of 5V High-Voltage HV BULK devices is quantified. The static figure of merit are unchanged up to 600°C 2h thermal budget (TB). A slight poly deactivation is observed for the highest TB (600°C 2h) affecting only the gate Workfunction WF and can be compensated for by modifying the channel dopant concentration. The silicide on the source and drain is shown to be stable, the weak point being the silicide instability of poly gate starting from 550°C post anneals. These results shows that HV SiO_2/Poly devices can be integrated on the bottom level of 3DSI with a comfortable TB (at least 500°C 5h) to process the top device. In parallel, reaching a low gate resistance in order to maintain good RF performance is achieved using Low-Temperature LT. UV Nanosecond Laser Annealing UV-NLA.

SCIENTIFIC COLLABORATIONS: [1]IMEP-LAHC, STMICROELECTRONICS, SCREEN

Context and Challenges

3DSI consists in stacking device layers in a sequential manner. This integration offers the highest 3D contact density but comes at the cost of TB constraints for the top layer processing, in order to preserve the performance of the bottom one. 3DSI is a great candidate for More than Moore applications, requiring High Voltages (HV) devices. Previous studies have confirmed the stability of advanced digital top devices up to 500°C, and that TB is sufficient to process HP digital devices. The aim of this study is to evaluate the maximum thermal budget that can sustain HV MOSFETs used as bottom transistors of a 3DSI. In addition, in order to preserve the underlying devices, processing of the top tier with UV Nanosecond Laser Annealing (UV-NLA) is considered. Indeed, this technique allows a selective heating of the surface while maintaining the underlying level at a relatively low temperature and enables to achieve low gate stack resistance.

Main Results

The main differences between HV and digital devices are summarized in Fig. 1(a & b). Digital devices (0.9V) uses FDSOI technology with Lg_{min}=30 nm, undoped channel and HfSiON/TiN gate stack. Meanwhile the HV MOSFET presents a doped BULK channel, SiO_2/Poly gate stack (EOT=13 nm) and Lg_{min}=600 nm.

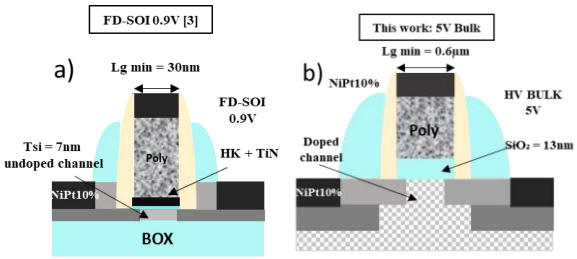


Figure 1: (a) Digital (0.9V) FDSOI & (b) 5V BULK

Additional TB (from 400°C to 600°C 2h) have been applied to BULK 5V devices. The Vth for both N&P after the additional TB is stable up to 550°C 2h, a slight Vth shift starts to be observed at 600°C 2h, for N&P respectively. In contrast, the gate resistivity is degraded up to 70% at 600°C. This gate deactivation has only a small effect on V_{th} (visible only at 600°C 2h), which can be compensated by adjusting the channel doping [1].

Low gate stack resistance with ns laser anneal

We propose a low temperature (LT) gate first approach in which an in-situ doped amorphous silicon layer is deposited at 475°C then subsequently converted into a polycrystalline film using UV ns laser annealing. We demonstrate the ability to obtain a low resistance poly-Si gate for the top transistors within a thermal budget expected to preserve the bottom devices electrical performance [2]. 2D numerical simulations performed using LIAB software show, in Fig.2, the beginning of the a-Si:P layer melt up to the complete melt. A correlation between the R_S quasi-linear decrease with larger and larger grains is proposed and attributed to the progressive conversion of the initial a-Si:P into poly-Si:P with a concomitant dopant activation until complete melt occurs.

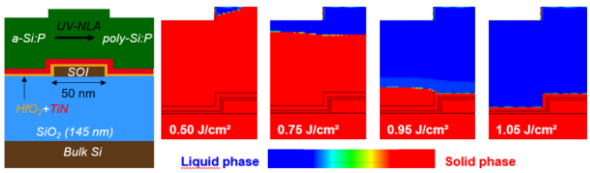


Figure 2: Numerical simulation of gate stack submitted to UV-NLA at various energy densities, from a-Si:P upper layer melt onset to its full melt.

Perspectives

Once, analog device stability is validated at LT up to 5V, the integration of analog stackable devices at LT with good analog performance should be possible.

RELATED PUBLICATIONS:

[1] C. Cavalcante et al., SSDM (2019), http://www.ssdm.jp/2019/ (paper N-4-02)

[2] S. Kerdilès et al., IEEE ECS (2019), https://iopscience.iop.org/article/10.1149/09301.0019ecst

3D Coolcube Integration for RF Applications

RESEARCH TOPIC:
RF applications, mm-wave, 3D sequential integration, low temperature process.

AUTHORS:
X. Garros, P. Sideris, J. Lugo, L. Brunet, C. Fenouillet-Beranger, P. Batude, (C. Theodorou)[1]

RF performance of a fully integrated CMOS 3D Sequential Integration (3DSI) is for the first time deeply investigated. We highlight that Top Tier PMOS processed at 630°C can feature good RF Figure-Of-Merits (FOM) with Ft=55GHz and Fmax=80GHz at L=30nm and VDD=-1V. Guidelines to further increase the 3DSI-RF MOS performance are also provided, based on a complete characterization and modeling of the key electrical factors affecting device RF FOMs. They lead us to propose an improved low temperature process (T<530°C) able to boost the PMOS RF performance i.e. towards Ft>100GHz and Fmax>170GHz.
Additionally, an in-depth analysis of the inter-tier dynamic coupling and RF crosstalk of digital circuits in 3D sequential integration enables to conclude for the first time on the need of a Ground Plane (GP) for various applications.

SCIENTIFIC COLLABORATIONS: [1]IMEP-LAHC

Context and Challenges
3D sequential integration (3DSI) is currently showing an industrial appeal for More Moore and More than Moore applications. It increases the density, efficiency and performance of digital chips without reducing the transistor size [1-2]. 3DSI opens the possibility to novel configurations such us analog-digital and analog-analog or RF applications. Current existing solutions such as Front End Module technologies (PDSOI, GaN) and Silicon photonics are still limited because of interconnections. 3DSI offers higher transistor density, small parasitic and interconnect length reduction, which should lead to better performance for millimeter-wave (mmW) circuits. 3DSI allows obtaining a performant digital tier close to the RF. For this reason, top-tier transistor are interesting for RF integration.
Also, in 3D sequential integration, the Inter-Layer Dielectric (ILD) separating the sequential tiers is ultra-thin (~100nm) and may lead to parasitic coupling between tiers. It is thus required to analyze the immunity of top devices when bottom layer is either digital, RF or analog circuit (VDD=2.5V).

Main Results
Low temperature devices RF performance:

	This Work		TED [a]	SSE'17 [b]
Technology	MOSFET		Junctionless	MOSFET
Channel	Si		Si	Top InGaAs Bottom SiGe
HK/MG	Top HfO_2/TiN	HfO_2/TiN	HfO_2/TiN	AL_2O_3/HfO_2/W
3D seq integration	FDSOI on FDSOI	Planar FDSOI	FDSOI on BULK	FDSOI on FDSOI
MaxProcess temp	630°C	<530°C	525°C	-
Top Tsi	7nm	11nm	9nm	20nm
Lg	30nm	30nm	80nm	120nm
Top channel type	PMOS		NMOS	NMOS
Top F_t@V_{DD}=1V	55 GHz	102 GHz	80 GHz	16.4 GHz
Top F_{max}@V_{DD}=1V	80 GHz	170 GHz	80 GHz	23 GHz

[a] A. Vandooren et al., TED 2018 [b] V. Deshpande et al., SSE 2017

Figure 1: Benchmarking of RF performance of 3D sequential [1]

Top Tier PMOS feature Ft of 55GHz and Fmax of 80GHz at VDD=-1V, FOMs which are at the state-of-the-art for a 3DSI integration (Fig. 1). In depth characterization and modeling allowed us identifying the key electrical factors affecting RF FOM such as mobility or gate resistance and to propose an improved low temperature process (T<530°C) able to boost the RF performance of the transistor [1].

Inter-tier Dynamic Coupling and RF Crosstalk in 3D Sequential Integration:
Through experiments and simulations, we have shown that, for purely digital 3D sequential circuits, there is no major coupling between top and bottom tiers, therefore inter-tier GP integration is not needed. However, when it comes to mixed signal and RF applications, a polysilicon GP layer provides the necessary immunity to inter-tier coupling effects like crosstalk. We have also demonstrated a novel integration scheme of inter-tier isolation with a polysilicon GP, highlighting its SOI compatibility and the advantages over metallic solutions (Fig.2) [2].

TOP TIER / BOTTOM TIER	Digital (V_{DD}=1V)	Mixed signal/RF
Digital (V_{DD}=1V)	No GP needed, t_{ILD}=130nm (Verified with SRAM cell in [4] and this work)	GP needed depending on frequency and layout of the application
RF	For typical digital logic level noise margins, GP may not be needed	
Analog (V_{DD}=2.5V)	t_{ILD}=350nm or GP insertion (Due to $V_{th,top}$ shift)	GP needed (Verified with RO case)

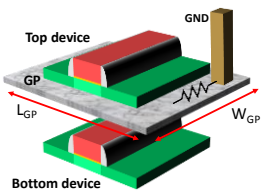


Figure 2: Summary table on the need of inter-tier Ground plane Introduction for various applications [2].

Perspectives:
Further RF performance boost for mm-wave applications are expected via technology/device co-optimization as well as in-depth device characterization and modelling.

RELATED PUBLICATIONS:
[1] X. Garros et al., IEDM (2019), https://doi.org/10.1109/IEDM19573.2019.8993512
[2] P. Sideris et al., IEDM (2019),https://doi.org/10.1109/IEDM19573.2019.8993493

Imaging, Modeling and Engineering of Strain in GAA Nanosheet Transistors

RESEARCH TOPIC:
CMOS, Transistors, Gate-All-Around, NanoSheet, Strain Engineering, Precession Electron Diffraction.

AUTHORS:
S. Reboh, R. Coquand, E. Augendre, N. Bernier, A. Jannaud, (N. Loubet, T. Yamashita)[1]

We combine in-house developed techniques of advanced transmission electron microscopy (TEM) and numerical models to map the evolution of strain along the integration of horizontally stacked Gate-All-Around NanoSheet transistors (GAANS). The findings provide insights and guidelines for strain engineering for sub-5 nm CMOS technology.

SCIENTIFIC COLLABORATIONS: [1]IBM Research Albany

Context and Challenges

In the framework of Moore's law, we saw a transition from 2D planar transistors to 3D FinFET. A forthcoming transition expected for sub-5 nm nodes where stacked gate-all-around channels (GAA) such as in NanoSheet (NS) transistors will define the architecture to deliver improved electrostatic control, density and performance [1]. Engineering of the elastic strains in the channel will be crucial to enhance the mobility of charge carriers. However, the complex 3D structure of GAA transistors makes measuring and controlling strain challenging. CEA-Leti has consolidated a solid reputation on developing TEM based techniques and modelling protocols to assess strain in nano-devices. Here, we use it to map the evolution of strain in integrated GAANS at an aggressive 10 nm design rule [2].

Main Results

To illustrate the work, in Fig. 1 we display the TEM and strain maps obtained by Precession Electron Diffraction (PED) after the epitaxy of source and drain. We show that the source/drain are not expected to be stressors as in previous technologies. Channels are tensile strained in εxx by the SiGe interlayers.

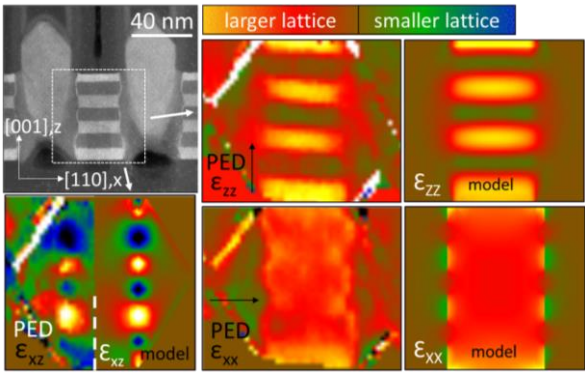


Figure 1: Dark-field TEM (top-left), strain maps (labeled PED) and model calculations after epitaxy of source and drain.

In Fig. 2, the TEM and strain maps are obtained when the channels are suspended before metal gate deposition. Strain in the channel is now compressive in εxx by -0.5% to -1%, in agreement with the needs for pFET. Our model suggests that the strain comes from inter layer dielectrics. Further impact of the gate stack, metal contacts and channel cladding is reported in [2]. We show that the suspended nature of the channels at the release step and the channel-embraced gate provide unique opportunities for strain manipulation in GAANS.

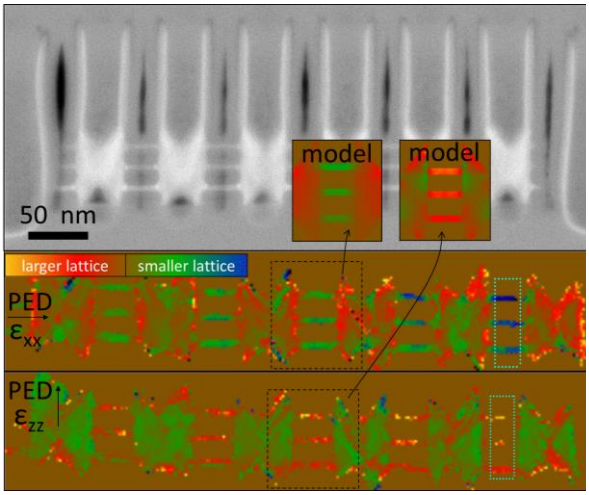


Figure 2: Dark-field TEM (top), strain maps (labeled PED) and model calculations for channel release step.

Perspectives

The developments and sophisticated protocols needed for the interpretation and modelling of the mechanics of this complex nanostructure are established. These methods and techniques can be directly extended to different systems where strain needs to be addressed at small local scale.

RELATED PUBLICATIONS:
[1] S. Barraud et al., Semicond. Sci. Technol. 34 (2019) 074001,https://doi.org/10.1088/1361-6641/ab1e5b
[2] S. Reboh et al., IEDM, (2019), http://dx.doi.org/10.1109/IEDM19573.2019.8993524

RF-SOI Technology for Power Amplifier Solutions

RESEARCH TOPIC:
RFSOI, 5G, Power Amplifier, Reliability

AUTHORS:
X. Garros, A. Divay, J. Cluzel, J. Lugo, A. Giry,F. Gaillard, (V. Knopik, N. Revil)[1]

A robust and low cost Si RF-SOI Power Transistor, which can deliver +31dBm output power with 74% of Power Added Efficiency (PAE) and 18dB of Gain, has been optimized for 4G & 5G sub-6GHz Power Amplifier (PA). In combining an original design and a full characterization of all aging mechanisms, it has been proven that power amplifiers fabricated in RF-SOI can meet the reliability and robustness required to challenge conventional technologies for power amplifiers. This study paves the way for integrating RF-SOI power amplifiers in front-end LTE and 5G modules for smartphones and Internet of Things (IoT) devices.

SCIENTIFIC COLLABORATIONS: [1]STMicroelectronics

Context and Challenges

RF-SOI is already the mainstream technology for some RF applications. In fact, SOI accounts for more than 90 percent of the current market for RF switches, which are integrated in smartphone Wi-Fi™ modules and every 4G LTE device. RF-SOI-based switches are a key technology to integrate into future 5G terminals. However, RF-SOI is less prominent in power amplifiers since the high voltages handled by the transistor induce device aging. So far, important design margins must be considered to guarantee this reliability at the expense of a performance reduction of the PA. The challenge of this work was therefore to determine how far RF performance can be improved without any reliability penalty.

Main Results

A 5 mm PA Transistor has been fabricated in 130 nm Si RFSOI technology by STMicroelectronics. The device is an interleaved transistor made of a L=0.3 µm nmos body-contacted transistors and a n-channel laterally diffused MOS (NLDeMOS) in cascode configuration (Fig. 1). The NLDeMOS has a ft of 44GHz and can handle high power due to its high BV of ~13.5V.

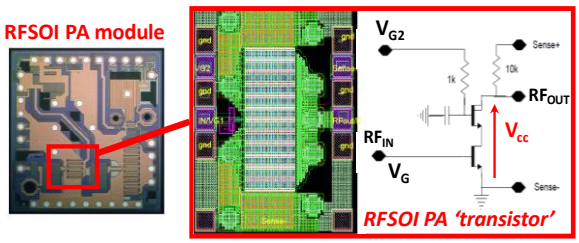


Figure 1: Schematic of the 5 mm PA RF-SOI transistor.

Large RF signal performance of the RF-SOI PA Transistor is measured at 2.7GHz. At nominal condition V_{CC}=3.4V, the transistor exhibits an excellent PAE of 74% at output power Pout of 28dBm. Increasing V_{cc} from 3.4V to 5V allows boosting the P_{out} of +3dBm while keeping the same record PAE and Gain (Fig. 2). Pushing further V_{cc} is suitable to improve PA performance.

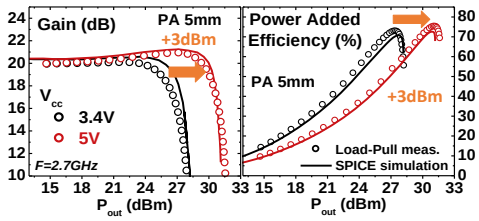


Figure 2: RF performance of the PA transistor for 3.4 & 5V power supply.

A large campaign of RF aging was then performed to determine how far V_{cc} can be pushed without affecting device long-term reliability. Negligible Hot Carrier aging is observed whatever the stress scenario - up to V_{CC}=6V. However, such a high V_{cc} may sometimes induce device BreakDown. Finally, the best trade-off in performance vs overall reliability (HC&BD) is obtained at a power supply of 5V. It allows to boost the RF PA transistor performance (P_{out}=31dBm) while guarantying a high reliability level - negligible RF aging & 3.5years TDDB lifetime (Table).

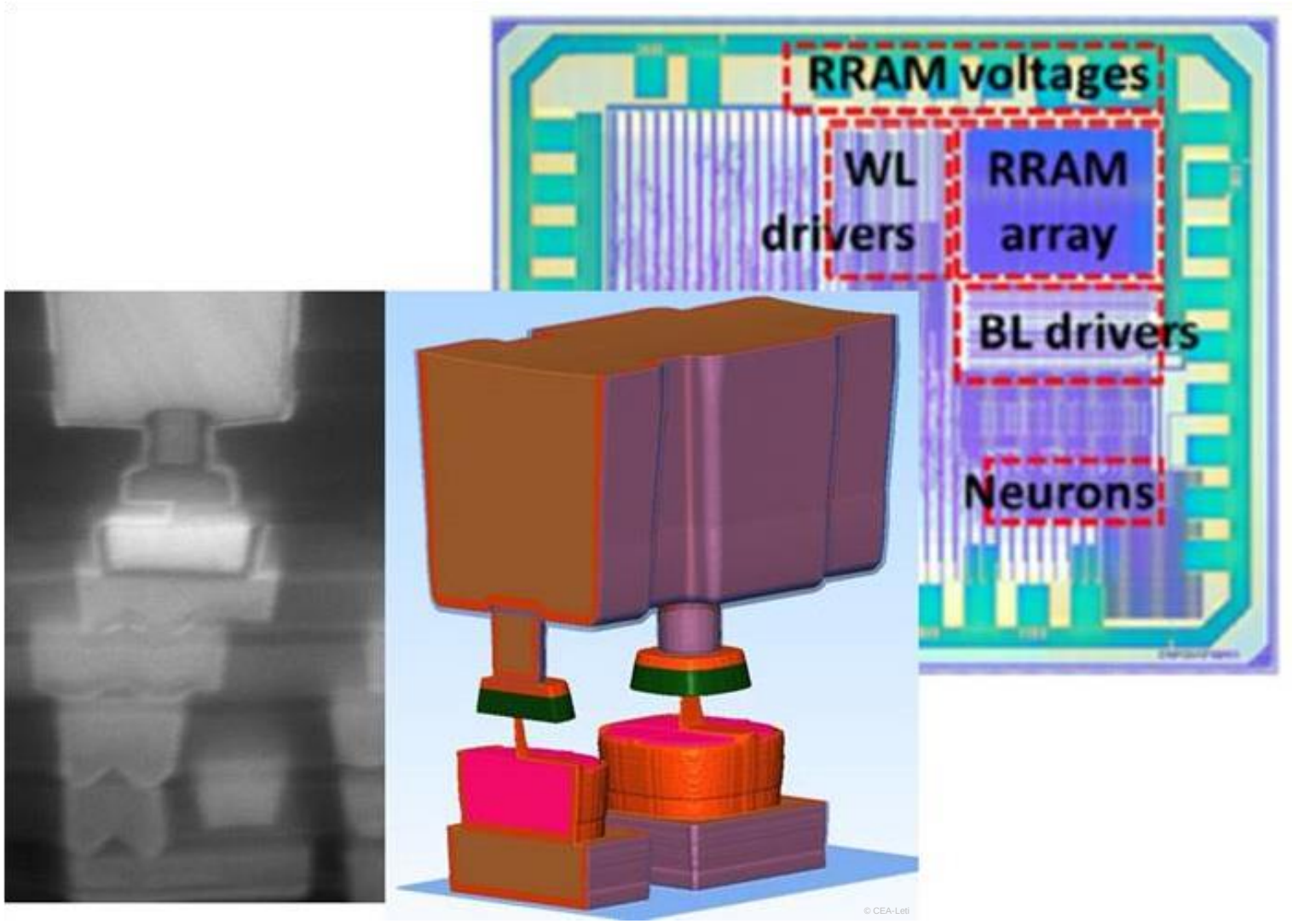
	Nominal V_{cc}=3.4V	Boost V_{cc}=5.0V
PA transistor Features	• L=0.3µm cascode interleaved PA transistor • ST 130nm RFSOI technology • F=2.7GHz	
RF Performance	- Max PAE=74% - Gain=+18dB - P_{out}=+28dBm	- Max PAE=74% - Gain=+18dB - P_{out}=+31dBm
PA Reliability		
RF HCI aging	Negligible Gain and PAE drifts	
Oxide BD MTTF	280000 years *@100% activity*	3.5 years *@100% activity*
BV	13.5V	

RF performance & reliability of our RF-SOI transistor.

Perspectives

This study focused on sub-6GHz frequency domain. It could be interesting in the future work to extend it on RF-SOI PA designed for 5G mm-wave applications.

RELATED PUBLICATIONS:
[1] X. Garros et al., IEDM (2019),https://doi.org/10.1109/IEDM19573.2019.8993649
[2] A. Giry et al., RFIC (2019); https://doi.org/10.1109/RFIC.2019.8701727


RRAM voltages
WL drivers
RRAM array
BL drivers
Neurons
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02 MEMORIES

- Resistive Memories to Enable the Design of Spiking Neural Networks
- Reliability and Variability of 1S1R OxRAM-OTS for High Density Crossbar Integration
- Phase Change Memory: Materials and Architecture Engineering Enabling Improved Speed and Stability for SCM and Embedded Applications
- Demonstration of BEOL-Compatible Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Scaled FeRAM Co-Integrated with 130 nm CMOS for Embedded NVM Applications
- Progress Toward Predictive Simulation of Electronic and Transport Properties Using ab initio Methods
- A2RAM as Capacitor Less Embedded DRAM

Resistive Memories to Enable the Design of Spiking Neural Networks

RESEARCH TOPIC:

Resistive memories, OxRAM, Spiking Neural Networks (SNN), synapses, neurons, Content Addressable Memories (CAM)

AUTHORS:

E. Vianello, A. Valentian, F. Rummens, T. Dalgaty, D.R.B. Ly, J-P. Noel, B. Giraud, E. Esmanhotto, E. Nowak, (M. Payvand, G. Indiveri)[1]

Resistive memory technologies (RRAM) can play a crucial role in the hardware implementation of the three main Spiking Neural Network (SNN) building blocks: communication, computation (neurons), learning and memory (synapses). We recently worked on the development of all these three blocks. We presented the first complete integration of a SNN, combining analogue neurons and Resistive RAM (RRAM)-based synapses. We fabricated and characterized a Content Addressable Memory (CAM) circuit that allows to implement the routing in reconfigurable neuromorphic hardware. We proposed to incorporate RRAM into neuron circuit models allowing memory to be truly co-localised with the computational units.

SCIENTIFIC COLLABORATIONS: [1]University of Zurich and ETH Zurich

Context and Challenges

Spiking Neural Networks (SNN), also called 3rd generation of neural networks, are fundamentally different from the neural networks that the machine learning community knows. In addition to neuron and synaptic models, SNNs incorporate the concept of time into their operating model. They operate using spikes, which are discrete events that take place at points in time, rather than continuous values. These networks are promising to build ultra-low power embedded and pervasive computing systems, which will fulfil the need to produce, process, and transmit an ever-increasing amount of data. We recently demonstrated that resistive memory technologies (RRAM) enables the hardware implementation of SNN, where storage and processing are inseparable.

Main Results

First, resistive memories arrays have been recognized as promising paths to realize density and plastic interconnects between neurons. We recently presented the first complete integration of a SNN, combining analog neurons and RRAM-based synapses [1] (Fig.1). The implemented topology is a perceptron, aimed at performing hand-written digit classification (MNIST database). The measured classification accuracy is 84%, with a 3.6 pJ energy dissipation per spike at the synapse and neuron level (up to 5x lower vs. similar chips using formal coding). Second, we designed and fabricated a resistive memories-based Content Addressable Memory (CAM) [2]. The proposed CAM cell is largely insensitive to the resistive memory resistance ratio and variability. This circuit allows to implement the routing (i.e. the method to send the spikes among the neurons) in reconfigurable neuromorphic hardware. This solution is less space consuming (2 transistors and 2 resistive memories) with respect to the conventional solutions (12 transistors) and it is non-volatile (no static power consumption). Third, resistive memories can be incorporated into neuron circuit models allowing memory to be truly co-localised with the computational units facilitating the realisation of massively parallel local plasticity mechanisms [3]. Based on this RRAM-based neuron, we proposed a technologically plausible intrinsic plasticity mechanism and demonstrated its use in the case of a recurrent neural network topology.

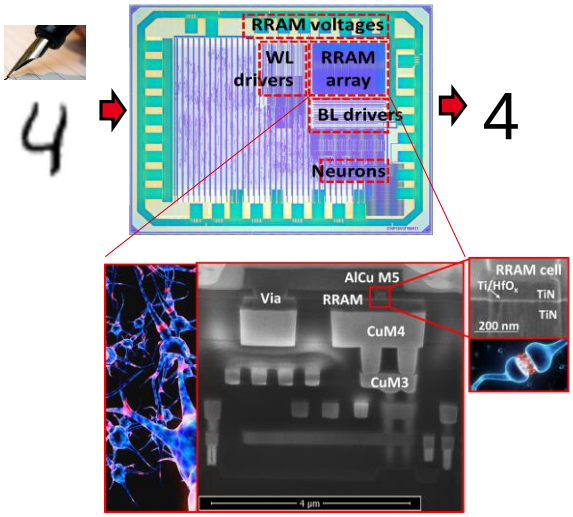


Figure 1: Chip micrograph of the SNN circuit for the hand-written digit classification (top) and cross section of the RRAM memories integrated between M4 and M5 of a 130nm CMOS technology

Perspectives

A first hardware implementation of the three main Spiking Neural Network building blocks (synapses, neurons, and routing) have been demonstrated. Next step will be a circuit directly connected to spike sensors, which will no longer need conversion and will offer temporal data.

RELATED PUBLICATIONS:

[1] D. R. B. Ly et al., IEDM (2019), https://doi.org/10.1109/IEDM.2018.8614603

[2] T. Dalgaty et al., APL Materials 7, 081125 (2019), https://doi.org/10.1063/1.5108663

[3] A. Valentian et al., IEEE IEDM (2019), https://doi.org/10.1109/IEDM19573.2019.8993431

Reliability and Variability of 1S1R OxRAM-OTS for High Density Crossbar Integration

RESEARCH TOPIC:

Resistive memories, OxRAM, embedded applications, storage class memories, crossbar, backend selectors, OTS

AUTHORS:

G. Molas, L. Grenouillet, J. Sandrini, C. Cagli, D. Alfaro Robayo, J. Minguet Lopez, N. Castellani, J. F. Nodin, A. Verdy, G. Navarro, M. Bernard, C. Carabasse, E. Nowak, (Q. Raffhay, G. Ghibaudo)[1], (M. Bocquet, J-M. Portal)[2], (D. Deleruyelle)[3]

HfO_2 OxRAM is one of the most promising advanced memory technologies. It can be integrated with a frontend transistor in 1T1R arrays for embedded applications. It can also be integrated with a backend selector in 1S1R for high density crossbar arrays for Storage Class Memory and In Memory Computing applications.
We recently pushed the scaling limits of OxRAM technology down to 30 nm and showed excellent compatibility with logic transistors on the 28 nm node. Memory reliability was analysed at the array level.
We then co-integrated an OxRAM memory with a backend selector showing outstanding device performances (10^6 programming, 10^8 reading and 10^9 read disturb cycles were demonstrated), opening the path for large memory crossbar arrays.

SCIENTIFIC COLLABORATIONS: [1]IMEP-LAHC, [2]IM2NP Marseille, [3]INL-CNRS, INSA de Lyon

Context and Challenges

Resistive Random-Access Memories (RRAM) are one of the most promising suitable technologies for embedded, Storage Class Memory and In Memory Computing applications. For embedded applications (1-32 Mb), a front end transistor is used as selector while for high-density crossbars (>1 Gb), a back-end selector is required to suppress sneak paths on unselected cells. Ovonic Threshold Switching (OTS) mechanism is one of the most interesting solutions for the latter due to their high non-linearity, high endurance and high ON/OFF current ratio. In CEA-Leti, we recently improved the maturity of the OxRAM technology for both embedded and standalone applications, and co-integrated it with a back-end selector for high density crossbar arrays.

Main Results

First a focus on the OxRAM technology was performed:
- The OxRAM shrink was addressed, down to 30 nm in diameter, focusing on the forming voltage, BER and data retention on a large statistics (4kbit arrays). Several strategies are provided to reduce the BER leading to a projected 10^{-6} BER result [1].
- We then illustrated how thin gate oxide transistors (GO1/SG) can meet the OxRAM high voltage requirement as the memory bit approaches 100 nm diameter, and we demonstrated a 120 nm OxRAM (1R) co-integration in 1T1R arrays with FDSOI transistors (Fig.1) with remarkably good performance (endurance up to 10^7 cycles on single bit). Co-integration of OxRAM with GO1 logic transistors is key for advanced embedded applications to allow large memory capacities.
Then, in a second step, the co-integration of an OxRAM (1R) with a backend selector (1S) was achieved in 1S1R arrays (Fig.2) to target stand alone and in particular storage class memories applications. Outstanding performances at the level of the state-of-art were demonstrated [2-3]. Up to 3 decades of current window margin and 6 decades of selectivity were achieved. More than 10^6 programming, 10^8 reading and 10^9 read disturb cycles were demonstrated. Ultra low OTS leakage current is compatible with 100Mb-1Gb bank size. Variability of voltage margin, selectivity and current margin were thoroughly investigated in a statistical way to identify the most critical features for high-density crossbar arrays.

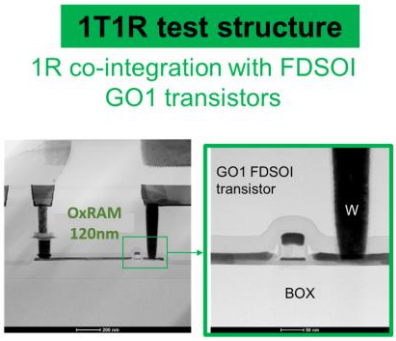


Figure 1: Cross sections showing the OxRAM integrated with a GO1 transistor on 28nm node for embedded applications

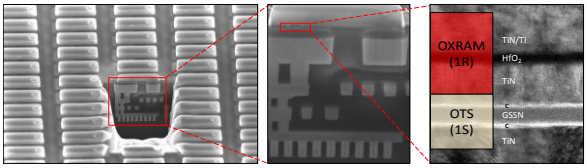


Figure 2: SEM image of an OxRAM with a back-end selector (1S1R) integrated In M4 on top of FEOL select transistor (130nm node)

Perspectives

A first demonstration of an OxRAM device with an OTS backend selector was achieved, showing excellent performances. The next step will be to shrink the OxRAM/OTS co-Integrated devices to <100nm to investigate the mechanisms that appear at small dimensions.

RELATED PUBLICATIONS:
[1] J. Sandrini et al., IEDM (2019), https://doi.org/10.1109/IEDM19573.2019.8993484
[2] D. Alfaro Robayo et al., IEEE int. Memory Workshop, (2019), https://doi.org/10.1109/IMW.2019.8739746
[3] D. Alfaro Robayo et al., IEDM (2019), https://doi.org/10.1109/IEDM19573.2019.8993439

Phase Change Memory: Materials and Architecture Engineering Enabling Improved Speed and Stability for SCM and Embedded Applications

RESEARCH TOPIC:

Resistive memories, PCRAM, GeSbTe, embedded applications, storage class memories

AUTHORS:

M.C. Cyrille, G. Navarro, AL. Serra, C. Sabbione, G. Bourgeois, N. Castellani, E. Nowak, (M. Frei, L. Nistor, M. Pakala)[1]

Phase-Change Memory (PCM) is today the most mature among innovative back-end non-volatile memory technologies, thanks to a wide set of features making PCM technology versatile enough to meet different applications requirements. The development of highly Sb-rich GeSbTe phase change material featuring high speed performance and high material stability under cycling suitable for Storage Class Applications is reported. For embedded automotive applications, the thermal engineering of the PCM cell architecture through the integration of low thermal conductivity dielectrics is reported, demonstrating improved PCM performance.

SCIENTIFIC COLLABORATIONS: [1]Applied Materials

Context and Challenges

Phase-Change Memory (PCM) is among the most promising innovative non-volatile memory technologies. It has entered the market addressing Storage Class Memory (SCM) applications and is sampled within Microcontrollers for Automotive applications. PCM technology features a wide set of interesting features such as fast read and write access, nanometer-scale scalability, good thermal stability and endurance. However, PCM cell architecture and material composition engineering is still necessary in order to improve electrical performances tailored to specific applications.

Main Results

First Focus:

Sb-rich GST compositions have been developed (Fig. 1.a: γ and δ compositions), targeting high speed performance and material stability under cycling for SCM applications [1]. Both compositions were integrated within 4Kb arrays. SET programming time as small as 10 ns was demonstrated on δ-GST single devices. Such high speed programming was confirmed in 4Kb δ-GST PCM arrays, with the demonstration of a reliable SET programming of more than 70% of the array with a 30 ns single pulse (Fig. 1.b). High stability of resistance states and high endurance cycling was confirmed.

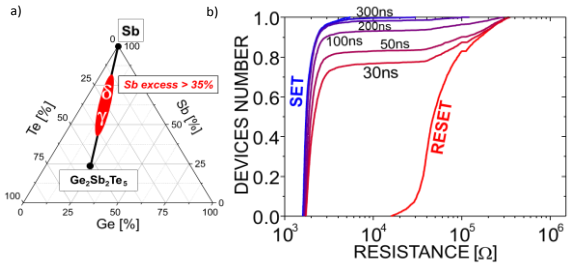


Figure 1: (a) γ and δ GST compositions (b) Resistances distribution obtained from SET speed test in δ GST 4kb array

Second Focus:

A low thermal conductivity SiC layer was integrated as the PCM encapsulation on Ge rich-GST 4Kb arrays (Fig.2.a). SiC-PCM cells performances were compared to standard SiN encapsulated cells [2]. A reduction of programming current was demonstrated (~ 15% of reduction wrt SiN-PCM) (Fig.2.b), as well as a higher programming speed and a data retention of more than 1h at 250°C. The improved stability at high temperature is attributed to a more uniform amorphous volume in SiC devices, confirmed by electro-thermal simulations, which enables a higher thermal confinement and therefore a more efficient heating of the phase-change material.

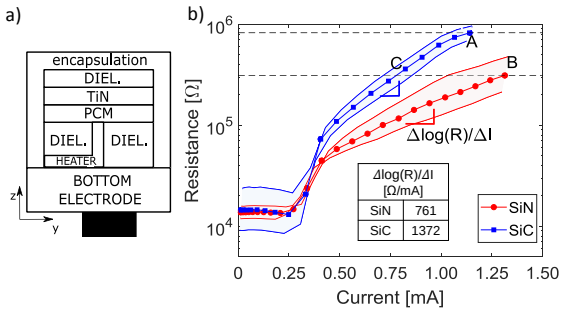


Figure 2: (a) Device Schematic, (b) Resistance vs programming current for 4Kb PCM arrays for SiN-PCM and SiC-PCM.

Perspectives

Alternative GST compositions as well as innovative encapsulations are being investigated to further improve PCM performances at the array level.

RELATED PUBLICATIONS:

[1] G. Navarro et al., IEEE int. Memory Workshop (2019), https://doi.org/10.1109/IMW.2019.8739656

[2] AL. Serra et al., IEEE int. Memory Workshop (2019), https://doi.org/10.1109/IMW.2019.8739588

Demonstration of BEOL-Compatible Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Scaled FeRAM Co-Integrated with 130 nm CMOS for Embedded NVM Applications

RESEARCH TOPIC:

Non-Volatile Memory, Ferroelectric Memory (FeRAM), Ferroelectric HfO_2,

AUTHORS:

T. François, J. Coignus, C. Carabasse, N. Vaxelaire, L. Grenouillet, E. Nowak, (U. Schroeder, S. Slesazeck)[1]

We successfully co-integrated $Hf_{0.5}Zr_{0.5}O_2$ scaled capacitors in the Back-End Of Line (BEOL) of 130nm CMOS, demonstrating for the first time their scalability and compatibility with BEOL thermal budgets. Excellent capacitor performance is reported down to 300 nm diameter, with remanent polarization $2.P_R$ > 40 µC/cm², 30ns operation speed and outstanding > 10^{11} cycling capability. Those results pave the way to ultra-low power (< 10fJ/bit), low cost FeRAM for IoT applications.

SCIENTIFIC COLLABORATIONS: [1]NaMLab gGmbH

Context and Challenges

Ferroelectric HfO_2-based thin films (< 15 nm) have been intensively studied for next generation ultra-low power memories due to their excellent CMOS compatibility compared to more conventional ferroelectric materials like PZT, and their potential for scalability. Promising performance, such as high remanent polarization > 40 µC/cm², coercive fields < 2 MV/cm, ultrafast switching speeds < ns and high endurance were reported since the first discovery of ferroelectric HfO_2 in 2007. However current published results are based on large area Metal/Ferroelectric/Metal capacitors (typically 10000 µm²), with thermal budgets larger than 500°C. Therefore we focused our studies on the following challenges: 1) co-integrate scaled capacitors with CMOS while preserving the orthorhombic (ferroelectric) phase with a BEOL-compatible thermal budget and 2) extract ferroelectric performance of single 1T-1C bitcells with memory-like electrical patterns.

Main Results

TiN/10 nm $Hf_{0.5}Zr_{0.5}O_2$/TiN capacitors with diameters down to 300 nm were integrated between M4 and M5 of 130 nm CMOS (Fig.1). The ferroelectric phase is maintained down to 350°C thermal budget [1], demonstrating the BEOL compatibility of this stack.

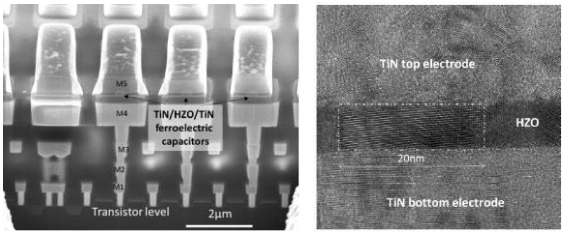
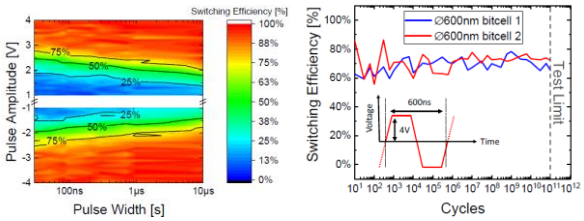


Figure 1: (a) SEM cross section showing the transistor level, the different metal lines, and Ø300 nm ferroelectric TiN/ $Hf_{0.5}Zr_{0.5}O_2$/TiN capacitors integrated between M4 and M5 of 130 nm CMOS (b) HRTEM image detail of a Ø300 nm capacitor with 20nm crystallite size (in-plane)

The ferroelectric switching kinetics was then derived [2] on 0.27µm² single cells for various pulse widths and amplitudes, revealing operation speeds as low as 30 ns and potential for multi-level programming (Fig. 2.a). The endurance measured on the integrated capacitors exceeds 10^{11} cycles (Fig. 2.b). The reported value is quite promising for FeRAM memories, where such high endurance will be required due to the destructive reading operation that necessitates a write back step.



(a) (b)

Figure 2: (a) Switching efficiency map on Ø600 nm capacitor with a PUND $2.P_R$ as reference and (b) ferroelectric switching efficiency measured on two Ø600 nm single capacitors with optimized pattern along cycling. No bitcell breakdown is observed before 10^{11} cycles (*i.e.* experimental limitation)

Perspectives

The BEOL compatibility demonstration of ferroelectric TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN capacitors combined with their excellent performance in terms of speed, power consumption, and data retention at 125°C [1] is promising for future embedded NVM applications. The next step consists in the design and characterization of FeRAM memory arrays to assess thoroughly the state distributions with bitcell size and therefore the potential of ferroelectric HfO_2-based capacitors for future low power and low cost applications.

RELATED PUBLICATIONS:

[1] T. François et al., IEDM, (2019), https://doi.org/10.1109/IEDM19573.2019.8993485

[2] T. François et al., IEDM, (2019), https://doi.org/10.1109/IMW.2019.8739664

Progress Toward Predictive Simulation of Electronic and Transport Properties Using *ab initio* Methods

RESEARCH TOPIC:

Simulation of electronic, optical and transport properties, using atomistic first principles methods

AUTHORS:

B. Sklénard, F. Triozon, A. Dragoni, (V. Olevano)[1]

Ab initio simulations based on density functional theory including many-body corrections are performed on various materials and heterojunctions. They provide reliable results for the electronic structure, optical properties, and quantum transport properties. They have been employed to compute accurate electronic structure and optical absorption of HfO_2. A new methodology has also been developed to couple *ab initio* calculations with quantum transport simulations. It has been applied to the calculation of the tunneling current through a metal/insulator/metal junction. These developments open perspectives for the technological development of new devices, which should benefit from a better knowledge of materials properties.

SCIENTIFIC COLLABORATIONS: [1]CNRS Institut Néel

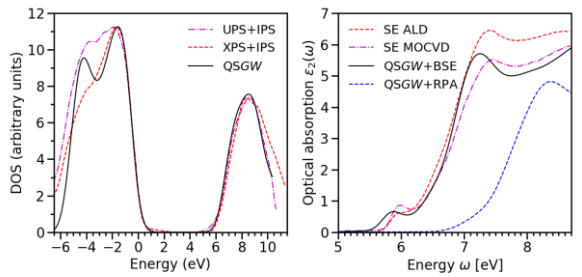
Context and Challenges

First principles methods based on density functional theory (DFT) allow the simulation of materials, defects, and interfaces at the atomic scale. While these methods are highly accurate for structural properties, they have limitations to predict electronic or optical properties. This is because DFT is a ground state theory, which generally underestimates the electronic band gaps of semiconductors and insulators, and which does not provide accurate excited states energies.

Many-body corrections, added on top of DFT, allow simulating electronic properties with much better accuracy. The use of these methods remains challenging, mainly because of their high numerical cost. The purpose of our research activity is to apply these methods to materials of interest for technological applications.

Main Results

The electronic and optical properties of monoclinic HfO_2 have been calculated using different levels of many-body corrections on top of DFT [1]. The results have been directly compared to raw experimental spectra. It was shown that the quasiparticle self-consistent GW (QSGW) correction, which updates both energies and wavefunctions, yields the best agreement with the experimental density of states (Fig. 1.b.). The optical absorption spectrum is well reproduced (Fig. 1.a.) by accounting for excitonic effects via the Bethe-Salpeter equation (BSE) on top of QSGW.



(a) (b)

Figure 1: Simulated vs. experimental density of states and optical absorption spectra of monoclinic HfO_2 [1]

These results enabled the material parameters to be refined with respect to the literature. In particular, the electronic bandgap was found 0.57 eV larger that the optical bandgap, which is attributed to the exciton binding energy.

The impact of many-body corrections on transport properties has also been investigated. The tunneling conductance through Ag/MgO/Ag junctions was calculated by using plane-wave DFT calculations, transformation to Wannier basis set, and calculation of the quantum transmission with the Landauer formalism [2]. Various many-body corrections were added on top of DFT and it was shown that while G_0W_0 corrections do not impact the conductance, hybrid functional (HSE) and COHSEX reduce similarly the conductance by more than one order of magnitude for the thickest oxide considered (figure 2). These two latter approximations are expected to yield more reliable results.

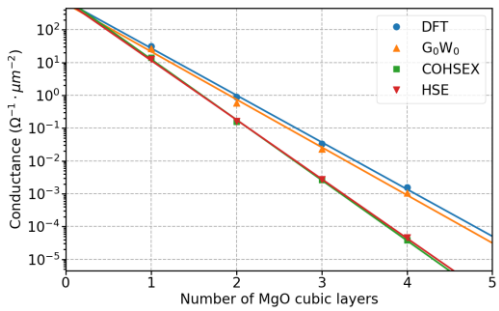


Figure 2: Tunneling conductance of an Ag/MgO/Ag junction vs. MgO thickness, computed within various approximations [2]

Perspectives

This research activity aims at providing predictive simulations of the transport properties of materials and heterojunctions. Targeted applications include emerging memories such as OxRAM or PCRAM, 2D materials, and ferroelectric devices. An important goal is the ability to screen several materials and/or metal contacts to guide technological developments

RELATED PUBLICATIONS:

[1] B. Sklénard et al., Applied Physics Letters 113, 172903 (2018), https://doi.org/10.1063/1.5044631

[2] A. Dragoni et al., Physical Review B 101, 075402 (2020), https://doi.org/10.1103/PhysRevB.101.075402

A2RAM as Capacitor Less Embedded DRAM

RESEARCH TOPIC:
1T-DRAM, memory, A2RAM, TCAD simulations, electrical characterization

AUTHORS:
J. Lacord, F. Tcheme Wakam, (X. Mescot, M. Bawedin, S.Cristoloveanu)[1]

A2RAM is a 1-transistor DRAM device built on SOI substrate with a doped buried layer, the so-called bridge, short-circuiting the source and the drain. The '1' state is defined by the presence of charges in the undoped part of the silicon film (the body) while the '0' state corresponds to a body empty of charge. Using TCAD simulations, we demonstrate a methodology to characterize electrically the bridge doping profile. We also show the functionality of A2RAM fabricated with an adaptation of the nanowire MOSFET process flow. Finally, we have developed an A2RAM compact model which describes memory operation.

SCIENTIFIC COLLABORATIONS: [1]IMEP-LAHC

Context and Challenges
Standard DRAM memory cells include one transistor used as a selector and a capacitor used as the storage element. DRAM scaling is achieved with the scaling of both elements: the transistor follows Moore's law and the capacitor, which needs to guarantee a capacitance value around 30~40pF is now built in 3D using a trench or stacked structure. The new capacitor structures involve higher process complexity, so higher cost. One solution to continue DRAM scaling is to use capacitor-less DRAM, such as A2RAM (Fig.1.a).

Main Results
After the first experimental A2RAM operation demonstration in 2012, we performed extensive TCAD simulations to optimize A2RAM structure and evidence the crucial role of the bridge doping profile. However, A2RAM bridge cannot be physically characterized because the film is too thin (< 20 nm) and not sufficiently doped (around $1 \times 10^{18}cm^{-3}$). That is why we have developed a bridge doping profile extraction method through electrical characterization based on C(V) measurement and the use of the capacitance derivative. The method is validated by TCAD simulation and use on experimental data [1]. Based on this study, A2RAM devices are fabricated following an adaptation of the nanowire MOSFET process flow (Fig1.b). It also includes a heterostructure between the SiGe body and the silicon source, drain and bridge to have a deeper potential well to enhance the charge storage, as well as the memory performance. Electrical measurement demonstrates the presence of the bridge and the ability to program and read the '1' state of A2RAM.

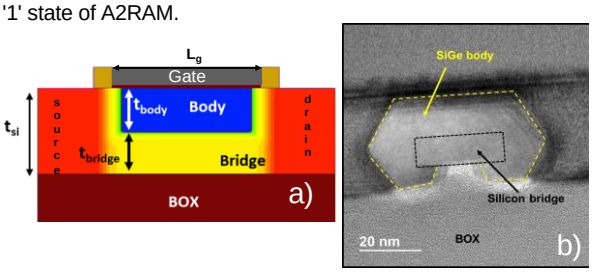


Figure 1: (a) A2RAM structure (b) A2RAM TEM cross section

To evaluate if A2RAM can operate in a matrix environment, a compact model is necessary. We consider the A2RAM as the combination of a SOI transistor in parallel with a variable resistor, the bridge (confirmed by [1]). As a consequence, only the bridge model development is needed. The DC behavior is provided by an empirical function that captures the variation of the bridge resistance with gate voltage from depletion to conduction (ohmic transport). The transition between both regimes occurs at the bridge threshold voltage [1,2] which is analytically expressed as a function of A2RAM technological parameters and back gate voltage.
A2RAM memory effect can be seen as a bridge threshold voltage shift due to the presence of charges in the body, so to memory state. First, the memory state is detected with a RC circuit comparator. Then, the memory state modulates the bridge threshold voltage where '0' state threshold voltage is given by the analytical expression developed for DC operation.
The A2RAM model has been implemented in Verilog-A and is used to simulate a 2x2 A2RAM matrix with a SPICE simulator. As illustrated in Fig.2, SPICE simulation can be used to demonstrate the successful programming and reading of the '1001' word.

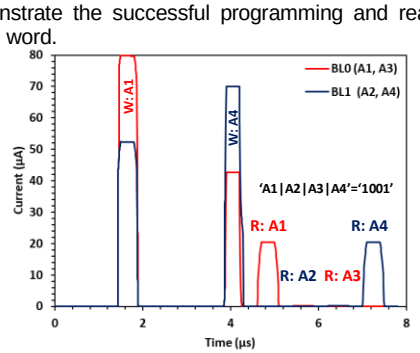
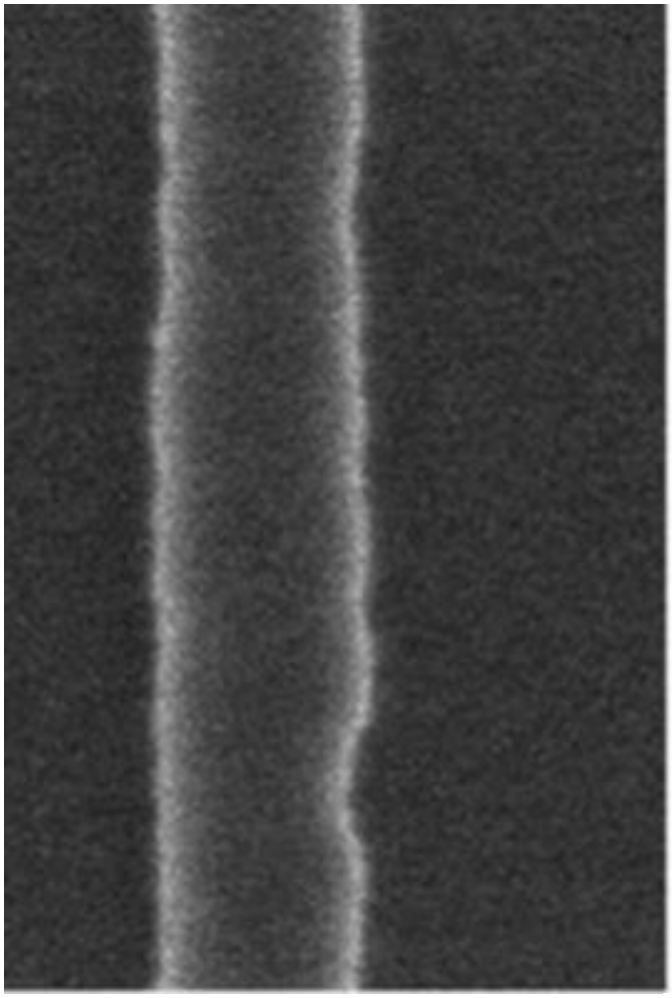


Figure 2: Current versus time obtained by SPICE simulation of two bit lines (BL0 & BL1) of 2x2 A2RAM matrix: 1001 word is programmed and read on A1|A2|A3|A4.

Perspectives
Compact model improvements are ongoing to account for retention and to include more physics into the memory operation model.

RELATED PUBLICATIONS:
[1] F. Tcheme Wakam, et al., Solid State Electronics (2019) https://doi.org/10.1016/j.sse.2019.03.038
[2] F. Tcheme Wakam, et al., Solid State Electronics (2019),https://doi.org/10.1016/j.sse.2019.107731



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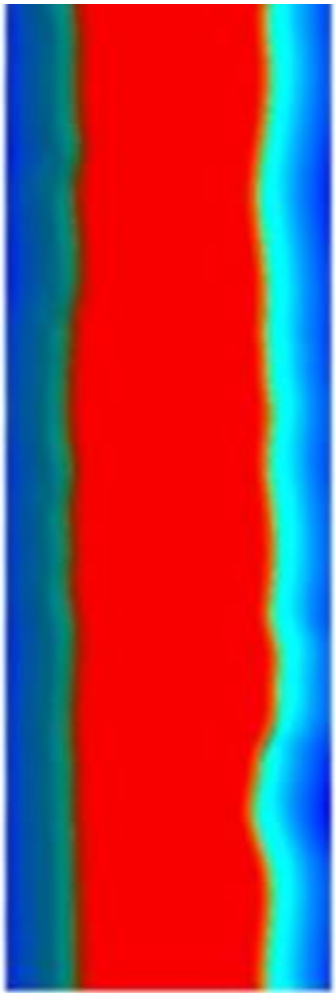
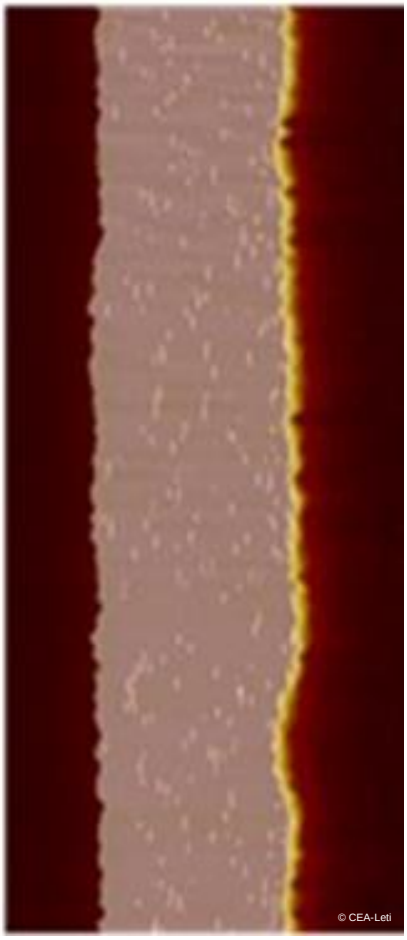


3D metrology from SEM



AFM

03 PATTERNING

- Enabling and Modeling 3D Lithography: An Application to CMOS Image Sensors
- Modifications of GeSbTe during Dry Etching for the Patterning of Phase Change Memories
- 3D Metrology from Tilted Electron Microscopy Images
- Spacer Patterning Lithography as a New Process to Induce Block Copolymer Alignment by Chemo-Epitaxy
- Alternative Lithography Combining Nano Imprint Lithography and DNA origami Technique

Enabling and Modeling 3D Lithography: An Application to CMOS Image Sensors

RESEARCH TOPIC:
CMOS Image Sensors (CIS), microlens, grayscale, 3D lithography, resist model, computational lithography

AUTHORS:
S. Bérard-Bergery, N. Allouti, J-B. Henry, P. Quéméré, F. Tomaso, R. Eleouet, M. Cordeau, R. Coquand, (P. Chevalier, C. Beylier)[1]

The last decades have seen a widespread use of optical systems, their applications ranging from mass-market to professional products. The core of such optical systems is the photodetector array, a pixelated matrix composed of thousands of pixels - a photodiode topped with a microlens. Its role is to focus precisely the incident light on the photosensitive area. The microlens is thus a crucial element whose 3D shape controls device efficiency. LETI has not only developed a 3D modeling approach to optimize the microlens manufacturing with the classical resist thermal reflow approach, but also investigates the grayscale lithography. Considered as an innovative and alternative solution, grayscale would enable the microlenses to be fabricated directly in 3D on the resist.

SCIENTIFIC COLLABORATIONS: [1]STMicroelectronics

Context and Challenges

Microlens integration on top of a pixel surface is now mainstream in the CIS industry. However, the ability of microlens devices to focus efficiently the incident light is governed by its curvature, which is adjusted according to the pixel size and the required focal distance. Thus, the microlens 3D shape must be carefully adapted to a given pixel to ensure maximal efficiency. The microlens optimization remains a crucial, yet empirical step in a fab. To speed up this processing time in a production environment, alternative solutions should be considered. Computational approaches can predict the formation of microlens, and new lithography techniques enable a direct patterning in 3D in the photosensitive resist.

Main Results

Photoresist thermal reflow is the most widespread method to manufacture microlenses. It is a cost effective solution, but it requires cycling masks and wafers to co-optimize design, lithography and melt conditions. To overcome this issue and propose an alternative low cost solution, LETI has developed a 3D resist reflow compact model approach, which enables fast and precise 3D simulation of microlenses [1]. This offers designers and process engineers an interesting anticipation tool (Fig. 1).

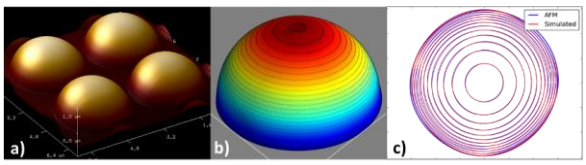


Figure 1: (a) AFM characterization of microlenses, (b) 3D reflow simulation results, (c) perfect match between AFM & simulation.

An alternative approach to the thermal reflow process to fabricate microlenses is the grayscale lithography. If mastered, this technique enables the fabrication of 3D complex shapes in the resist directly during the photolithography step. With a first *a priori* test mask, new 300 mm lithography processes have been developed [3], bringing the first proof-of-concept of 3D objects achieved with optical lithography (Fig. 2a and 2b).

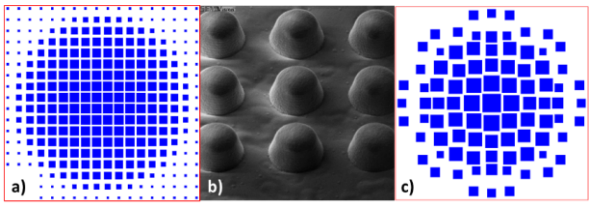


Figure 2: (a) *a priori* pixelated example embedded into 1st mask, (b) corresponding microlenses obtained, (c) optimized mask result from dedicated data-preparation solution.

From these results, LETI has developed specific computational solutions. A new mask optimization flow has been implemented (Fig 2c) to determine which non-intuitive configurations embedded into the mask may print later the desired 3D shape in the resist. This alternative data-preparation relies on a specific grayscale resist modeling approach [2], and can be distributed on computing cluster under Unix environment. Its intensive use serves to build a second mask iteration, attempting to address real optical applications cases for industrial partners.

Perspectives

Grayscale is foreseen as an enabling technique which could give access to 3D features not achievable with optical lithography. Grayscale capabilities will be explored thanks to the next mask to cover a wide range of 3D geometries, mostly being microlenses. In particular, we will try to enable the patterning of multi-height, multi-shape structures in a single lithography step. Continuous work will be carried out with resist suppliers to evaluate new materials. The compatibility of grayscale lithography with following etch process step will be studied also.

RELATED PUBLICATIONS:
[1] S. Bérard-Bergery et al., Proc. SPIE, 10962 (2019), http://dx.doi.org/10.1117/12.25149221
[2] P. Chevalier et al., Proc. SPIE, 10958, (2019), http://dx.doi.org/10.1117/12.2514234
[3] N. Allouti et al., Proc SPIE, 10958, (2019), http://dx.doi.org/10.1117/12.2514712

Modifications of GeSbTe during Dry Etching for the Patterning of Phase Change Memories

RESEARCH TOPIC:
Plasma etching, GeSbTe (GST), damages, oxidation, phase change memories (PCM)

AUTHORS:
C. Boixaderas, S. Barnola, Y. Mazel, E. Martinez, (Y. Canvel, Lagrasta)[1]

Phase-Change Memory (PCM) can be viewed as one of the most promising candidates for replacing current non-volatile memory devices such as Flash technologies. In the perspective of large-scale integration, the device performances are getting increasingly more sensitive to surface effects with the GST layer. A full study of interactions between Ge-rich GST and halogen gases used during plasma etching was performed and completed by the reactions induced by air exposure: CF_4, HBr or Cl_2 bring about some alterations of the GST stoichiometric composition and surface damages. In addition, the chalcogenide is very sensitive to oxidation by air exposure. Currently the best compromise found is the use of HBr as an etching gas and the implementation of time constraints between the manufacturing steps. Future studies will focus on the passivation of the GST that can be a means of protection against aggressive environments.

SCIENTIFIC COLLABORATIONS: [1]STMicroelectronics

Context and Challenges
For the manufacture of PCM, GST ternary alloys are patterned using Inductively Coupled Plasma etching. effects of different plasma chemistries on GST have been investigated.
Ge-rich GST films were deposited on 300 mm substrates and partially etched with CF_4, HBr or Cl_2 [1]. Thanks to several complementary techniques such as XPS, PP-TOFMS, AFM and SEM, etched films were characterized and compared to reach a trade-off for GST etching process.

Main Results
XPS results show the incorporation of halogens resulting in the formation of GST halides at the surface, with decreasing reactivity following the sequence CF_4>Cl_2>HBr (Fig. 1)
The quantification of Ge, Sb, Te elements reveals a Te-rich damaged layer at the extreme surface of GST for HBr (<2nm) but deeper in bulk for CF_4 and Cl_2 (4-5nm).

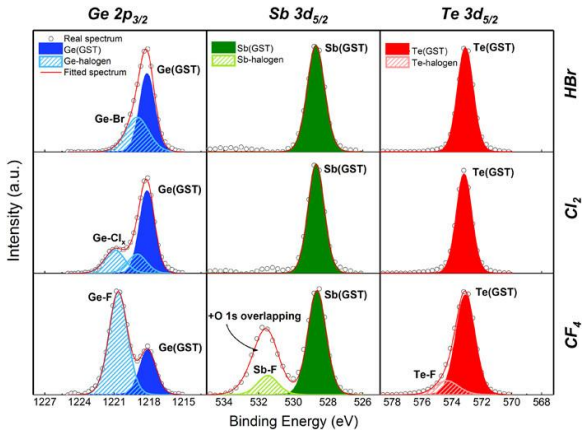


Figure 1: XPS spectra of Ge, Sb, Te elements after the GST partial etching in HBr, Cl_2 and CF_4 plasmas.

Scanning electron microscopy (SEM) and atomic force microscopy (AFM) characterization demonstrate that HBr plasma generates the smoothest etched surface and the lowest roughness.
In all cases, both chemical reactivity and physical ion bombardment cause GST stoichiometry modification due to the higher affinity between halogen and GST in the order of Ge>Sb>Te.
Finally, the HBr plasma can be considered as the best etching chemistry to minimize the degradation of the Ge-rich GST composition, the halogen contamination and the surface roughness.
Air exposure is unavoidable during the process flow of the PCM cell. The sidewalls of GST are modified by the incorporation of oxygen that induces changes of the material composition and degradation of the pattern dimensions (Fig. 2). This phenomenon starts to become critical only after 24h of air exposure [2].

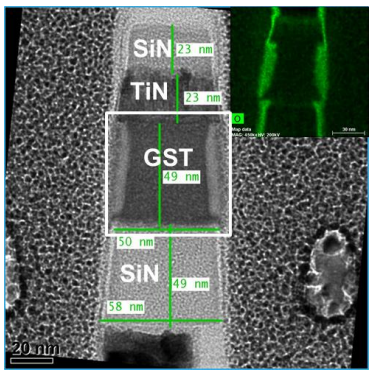


Figure 2: TEM-EDX image of a PCM cell post plasma etching and 30 days air exposure

Perspectives
Two root causes of GST damages were clearly identified and demonstrated: interaction with etching plasma and oxidation by air exposure. Current investigations on the passivation of the GST appear to be an effective solution to protect the material from potential degradations.

RELATED PUBLICATIONS:
[1] Y. Canvel, C. Boixaderas et al., J. Vac.Sci.Technol. A37(3), 10 (23), (2019), http://dx.doi.org/10.1116/1.5089037
[2] Y. Canvel, C. Boixaderas et al., Microelectronic Engineering, (2020), https://doi.org/10.1016/j.mee.2019.111183

3D Metrology from Tilted Electron Microscopy Images

RESEARCH TOPIC:

3D metrology, electron microscopy, 3D architecture, computational metrology

AUTHORS:

A. Fay, J. Hazart, S. Bérard-Bergery, (C. Valade, E. Sungauer)[1], (M. Besacier, C. Gourgon)[2]

The chip scaling and the increased 3D complexity of the device architectures for advanced nodes comes together with 3D metrology requirements. Within this context, LETI has developed a robust, non-destructive and fast 3D metrology based on scanning electron microscopy (SEM) with a tilted electron beam. The reconstruction of the topography of structures is performed by mean of a linear model, which links defined points of interest on stereoscopic SEM images to the geometrical parameters. The model calibration is carried out with Monte-Carlo SEM simulations, experimental SEM images and associated atomic force microscopy (AFM) images. The reconstruction of experimental "line" type patterns demonstrates the good accuracy of the method.

SCIENTIFIC COLLABORATIONS: [1]STMicroelectronics, [2]LTM-CNRS

Context and Challenges

With the advancement of microelectronics technologies, the architecture of electronic components is becoming increasingly complex. The knowledge of the dimensional characteristics of the structures becomes the key to understanding and optimizing the behavior of these components. It is therefore critical to develop rapid, non-destructive three-dimensional measurement methods. SEM is widely used to carry out dimensional measurements because of its speed and its non-destructive character. However, obtaining quantitative and precise 3D information remains a challenge.

Main Results

Thanks to an electron microscope fitted with a tilted electron beam, it is possible to obtain images at different viewing angles (Fig. 1.a). From a naïve analysis of these images, the height and the sidewall angles of the observed patterns can be directly extracted geometrically. However, the electron-matter interactions make the problem non-trivial as the SEM signal depends on the surrounding environment of the electron beam impact point.

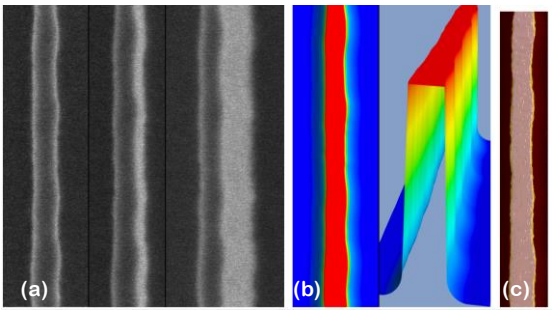


Figure 1: (a) Raw SEM images of a line pattern (b) 3D reconstruction (c) Reference AFM image

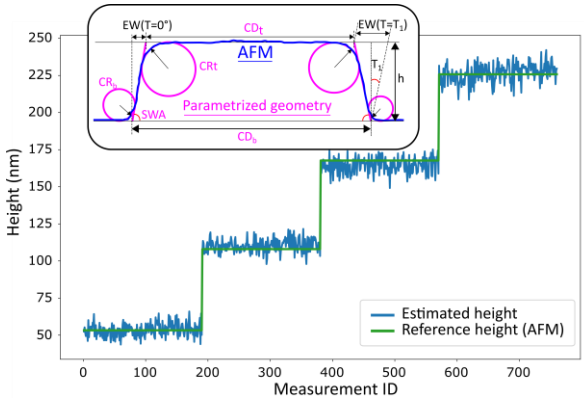


Figure 2: Height estimate of 800 line patterns. (inset) approximation of a line type geometry with 8 parameters.

For line-type patterns (inset Fig. 2), specific points called descriptors are placed mathematically on the SEM images, and their variation laws as a function of the geometry parameters is theoretically established by mean of Monte-Carlo simulations. These laws are refined with experimental SEM and AFM images in order to build a linear reconstruction model. This model is then used to reconstruct the topography of lines of different heights, showing overall results consistent with reference 3D metrology (AFM, FIB-STEM) (Fig. 2 and 1.b).

Perspectives

The presented 3D reconstruction approach from stereoscopic SEM images can be extended to multiple patterns such as trenches, dense-lines and micro-lenses. The reconstruction uncertainty can be further reduced by improving the SEM images pre-processing. We also investigate a more generic approach to reconstruct the geometry when the feature is not known in advance.

RELATED PUBLICATIONS:

[[1] C. Valade et al., Proc. SPIE 10959 (2019), https://doi.org/10.1117/12.2514977

[2] C. Valade et al., JM3, 18(3) 034001 (2019), https://doi.org/10.1117/1.JMM.18.3.034001

Spacer Patterning Lithography as a New Process to Induce Block Copolymer Alignment by Chemo-Epitaxy

RESEARCH TOPIC:
Advanced patterning, directed self-assembly, block copolymers

AUTHORS:
M. Argoud, G. Rademaker, A. Sarrazin, A. Le Pennec, A. Gharbi, G. Eleouet, K. Benotmane, N. Possémé, R. Tiron (A. Paquet, C. Navarro)[1], (K. Sakavuyi)[2], (P. Nealey)[3], (R. Le Tiec)[4], (M. Harumoto)[5]

Directed self-assembly (DSA) of block copolymers (BCP) is a promising solution for advanced patterning of sub-10-nm technology nodes. Known for high-resolution capabilities, low-cost and easy process integration, DSA continues to raise interest in the semiconductor industry. DSA technology is suitable for multiple patterns such as line and space, contact shrink and multiplication and pillars. Recently, CEA-LETI has developed original DSA approaches from lab scale to industrial scale using its DSA pilot line and advanced BCP materials. A new DSA chemo-epitaxy process, using spacer patterning lithography benefits, is reported here.

SCIENTIFIC COLLABORATIONS: [1]Arkema, [2]Brewer Science, [3]Univ. Chicago, [4]Aplied Materials, [5]SCREEN

Context and Challenges
Affordable, simple, versatile: DSA is still highly investigated as a lithography technique to pattern sub-10-nm features for CMOS industry. DSA is used to target different lithography applications: line/space in metal layers, contact hole shrink and multiplication, and pillar patterning.
Chemo-epitaxy DSA processes align the block copolymers by means of a template with chemical contrast. The current chemo-epitaxy processes are showing their limitations today, mainly due to the resolution limitation of conventional lithography techniques needed for the guide formation.

Main Results
A new chemo-epitaxy process, named ACE (Arkema-CEA), based on spacer patterning, has been developed on a 300 mm DSA pilot-line [1]. This process offers chemical guides with a very small critical dimension (CD < 20 nm) controlled by the deposition process (Fig. 1). Moreover, by combining spacer pattering and DSA advanced technologies, high pitch division is feasible (for example from 120 nm initial pitch to 30 nm final pitch).

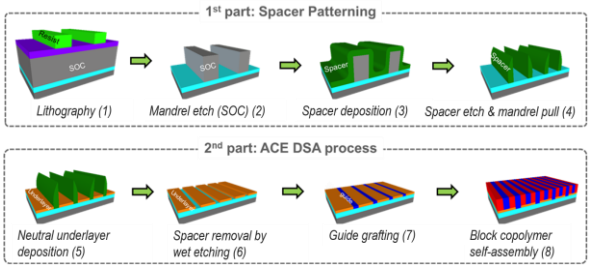


Figure 1: ACE process flow

The main efforts for ACE process development concerned the surface energy control and compatibility of the materials of the chemical guiding template. By using advanced metrology, selected depending on the step, a process window for a 30 nm pitch PS-*b*-PMMA BCP has been successfully demonstrated (Fig. 2). The chemical guiding pattern design and the various etching steps have been optimized to achieve this state-of-the-art result. Moreover, a first proof-of-concept of DSA of high-χ BCP system with aggressive pitch (18 nm pitch) (Fig. 2b).

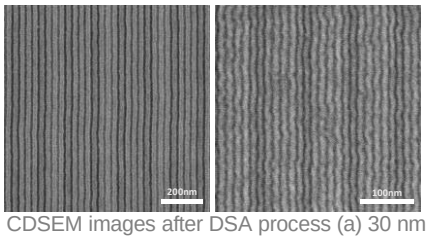


Figure 2: CDSEM images after DSA process (a) 30 nm pitch (b) 18 nm pitch

A high-resolution patterning context such as ACE, removing PMMA without consuming PS and conserving the initial dimensions remains a challenge requiring excellent etch control. Hence, a plasma etch chemistry allowing a perfect control of polymerization has been developed [2]. This works by protecting the PS template by thin polymer deposition, while PMMA is etched by the same plasma chemistry. By applying a single step, results remain similar to atomic layer etching. This process has been applied to line/space applications and confirmed its potential to develop new patterning architecture.

Perspectives
Future works will be focused on ACE process stabilization, understanding and characterization, especially in terms of roughness, for the 30 nm pitch PS-*b*-PMMA BCP. Chemical guiding patterns will be manufactured by immersion lithography, in order to optimize alignment of 18 nm pitch high-chi BCPs. Finally, transfer of DSA patterns into underlying hard-mask will be closely investigated

RELATED PUBLICATIONS:
[1] A. Paquet, A. Gharbi et al., Proc. SPIE 10958 (2019) https://doi.org/10.1117/12.2514960
[2] A. Sarrazin et al., Journal of Vacuum Science & Technology B 37, 030601 (2019), https://doi.org/10.1116/1.5090395

Alternative Lithography Combining Nano Imprint Lithography and DNA origami Technique

RESEARCH TOPIC:

Nanolithography, advanced patterning, nanoimprint lithography, DNA origami

AUTHORS:

M. Marmiesse, J. Reche, H. Teyssedre, F. Delachat, R. Tiron, (X. Chevalier, C. Nicolet, C. Navarro)[1], (G. Bellot et N. Aissaoui)[2]

Alternative lithography such as Nanoimprint lithography (NIL) and DNA origami lithography techniques differ from other conventional lithography by the fundamental process mechanisms involved. The structures are firstly created by resist flow then by DNA structuration. In order to be integrated in nanoelectronic devices, it is crucial to develop a method to place individual DNA origami structures on a patterned substrate. NIL appears like an ideal candidate to manufacture patterns thanks to high throughput and low cost. The combination of these two methods are closely linked to material usage and compatibility. LETI has defined the process conditions needed to make sub-10nm patterning successful.

SCIENTIFIC COLLABORATIONS: [1]Arkema, [2]INSERM Montpellier.

Context and Challenges

The microelectronics industry is facing a huge challenge for sub-10-nm lithography. The Extreme ultraviolet (EUV) technology insertion still deals with process, infrastructure and cost challenges. Therefore, several alternatives to photo-lithography have been developed.

One of them, the Nanoimprint Lithography (NIL) provides a low-cost solution of replication, with access to sub-50 nm structures. Thanks to this technique, single step for 3D patterning and beyond CMOS applications becomes promising for features down to 50 nm. A second alternative lithography, based on DNA nanostructures, offers periodical auto-organization with a theoretical resolution of 2 nm DNA origami shape, with the advantage to address complex patterns, by adjusting critical dimension (CD) and pitch in the same origami. However, the main limitation of DNA origamis is their deterministic positioning on a substrate.

To overcome this major issue, nano-patterning hybrid process has been developed by combining nanoimprint lithography and self-assembly of DNA origami. Today, the key challenge is to preserve post-lithography surface chemistry to allow deterministic placement of DNA nanostructures on the substrate.

Main Results

NIL process includes almost ten steps comprising five different materials to obtain replication (Fig. 1). A crucial point to guarantee correct replication is material selection.

Anti-stacking layers have been evaluated [1], where the compatibility of this material with one of working stamps has been demonstrated.

In parallel, a first demonstration of patterning capabilities by using DNA origami as a lithographic mask process was achieved [2]. To counter the random adsorption of DNA, a NIL process has been developed (Fig. 2). The creation of a chemical contrast HMDS/SiO_2 allows the specific DNA placement on the desired binding sites. More precisely, SiO_2 exhibits DNA origami binding, whereas HMDS does not allow DNA adsorption.

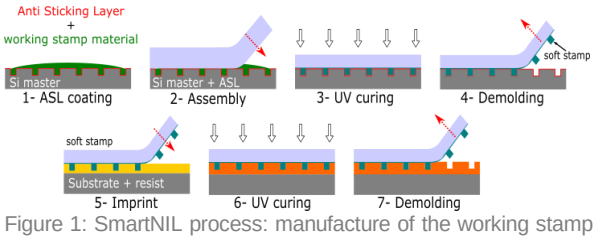


Figure 1: SmartNIL process: manufacture of the working stamp (steps 1 to 4) as a bilayer foil composed of a working stamp material and a polymer foil coated with an acrylic glue, process replication (steps 5 to 7) in the imprint resist with successive lamination-curing-demolding steps

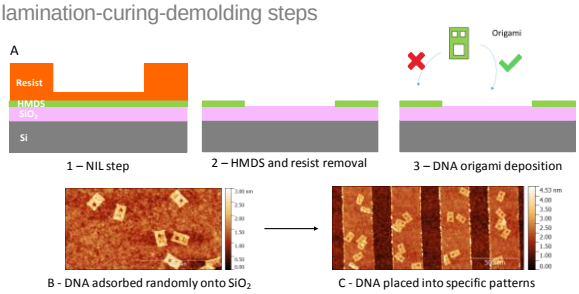


Figure 2: (A): Nano-patterning hybrid process scheme. (B) AFM images of DNA randomly adsorbed on a substrate, and (C) DNA deposited on NIL patterned substrate.

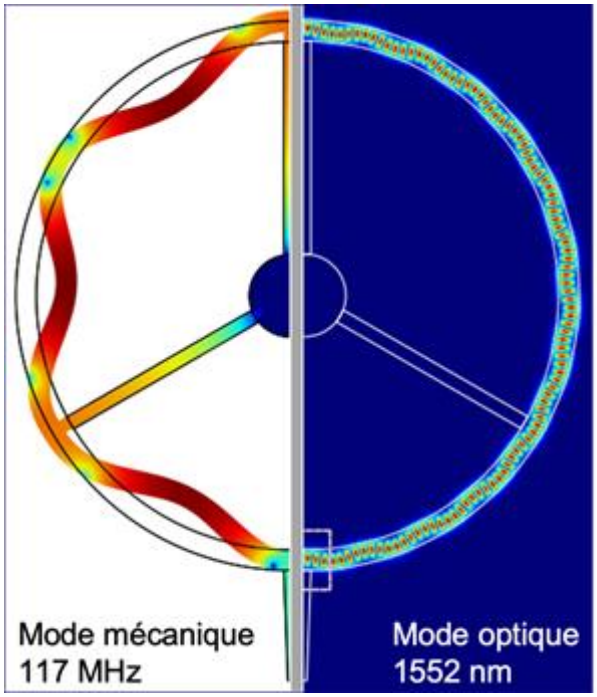
Perspectives

This first demonstration of DNA origami placement on a substrate pre-patterned by NIL is very encouraging. The next challenge will be to control more precisely their orientation on a substrate by using high resolution NIL masters with patterns of the size of DNA origami and functionalization of DNA origamis.

RELATED PUBLICATIONS:

[1] F. Delachat et al., Proc. SPIE, 10958, (2019), https://doi.org/10.1117/12.2515607

[2] R. Tiron et al., Proc. SPIE, 10958, (2019), https://doi.org/10.1117/12.2515811


Mode mécanique
117 MHz
Mode optique
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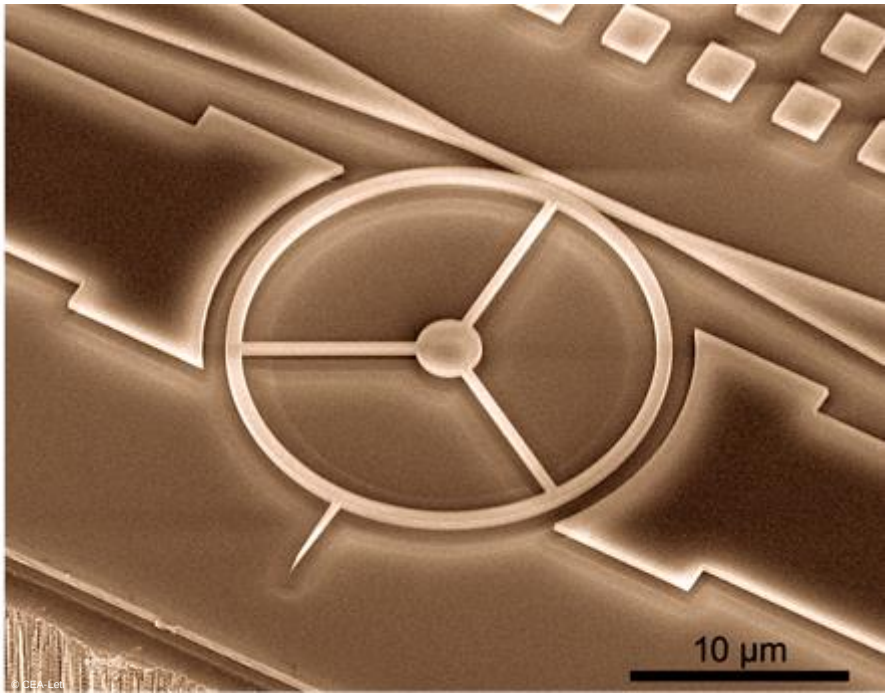

10 µm

04 MENS, NEMS & RF COMPONENTS

- Piezoelectric PZT Actuators on Glass
- High-Frequency Lithium Niobate Film Bulk Acoustic Resonator
- Silicon-Integrated Photoacoustic Sub-ppm Gas Sensor
- A 3D Process for High Performance Capacitive Inertial Sensors
- Towards Ultrasensitive and High Bandwidth Optomechanical AFM Probes
- Biosensing with Graphene Transistors
- First MEMS Microphone Based on Capacitive Transduction in Vacuum
- Near-Zero Energy Computing Based On Contactless MEMS

Piezoelectric PZT Actuators on Glass

RESEARCH TOPIC:
MEMS, Actuators, Sensors, Piezoelectric, PZT, Glass, Haptics, ITO electrodes, Transparent stack

AUTHORS:
G. Le Rhun, F. Casset, C. Dieppedale, B. Desloges, B. Wagué, B. Neff, C. Querné, G. Enyedi, P. Perreau, P. Montméat, C. Licitra, S. Fanget

Lead zirconate titanate (PZT) is today the most powerful piezoelectric material for micro-actuator applications. However, its high crystallization temperature, around 700°C, makes its deposition on glass substrate very difficult. We developed a 200 mm technological process that allows the transfer of film stacks from a silicon substrate to any other substrate. It was used for transferring high quality sol-gel deposited PZT films from the silicon growth substrate to glass. A unique haptic solution based on thin-film PZT actuators reported on glass substrate was then developed. It enables textured surfaces to be felt, induced by ultrasonic vibration, playing with the variable friction between a finger and the plate resonator. In addition, we managed to fabricate functional ITO/PZT/ITO transparent capacitors on glass, thus opening the way to the integration of transparent piezoelectric MEMS on glass for haptics devices or other functionalization of screens and windows.

Context and Challenges

With the emergence of haptic devices, there is a growing need for piezoelectric transducer devices integrated on transparent support. One great challenge is thus the integration of PZT, one of the most suitable piezoelectric material for actuation on glass for touch screen/panel as well as smart windows. However, due to the relatively high crystallization temperature (700 °C), it is practically impossible to grow high quality sol-gel PZT thin-films on any type of glass substrate.

Main Results

At CEA-Leti, we developed a 200 mm technological process that allows the transfer of film stacks from a silicon substrate to any other substrate. It was used for transferring high quality sol-gel deposited PZT films from silicon growth substrate to either Si, glass or polymer. The transferred PZT film keeps its high (100) texturation obtained during deposition, which is required for optimal piezoelectric properties. Taking advantage of the high piezoelectric coefficient of PZT actuators reported on glass, we demonstrated low voltage and high performances haptic interfaces [1]. The integration of PZT actuators on glass substrate leads to a plate displacement amplitude multiplied by more than a factor 7 compared to the displacement amplitude induced by thin-film AlN actuators that are typically deposited on glass substrates (Fig. 1).

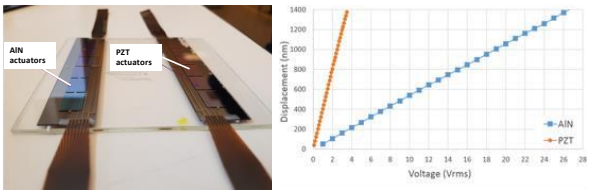


Figure 1: Photograph of the haptic plate with either AlN or PZT actuators, and measured maximum displacement amplitude, function of the actuation voltage, for both deposited thin-film AlN and reported thin-film PZT on glass devices.

In a subsequent development, a PZT-based transparent stack was reported on a glass substrate to form transparent capacitors that could be used as actuators for haptic applications [2]. Figure 2 shows a photograph of a transparent PZT/ITO full sheet stack reported on a 200 mm glass substrate. The multicolor logo is clearly visible through the entire wafer. The transparency of the full stack was superior to 60% in the visible range. Functional ITO/PZT/ITO capacitors on glass with remarkable ferroelectric and piezoelectric properties were successfully realized. This demonstrates that we can integrate high quality PZT on both glass substrate and Si. Our demonstration opens the way to the integration of transparent piezoelectric actuators on glass for haptics.

Figure 2: Photograph of a 200 mm Glass wafer with full sheet PZT/ITO stack reported on it

Perspectives

Now we aim at realizing fully transparent haptic devices based on thin-film PZT actuators reported on glass substrate. Other developments of transparent piezoelectric actuators and sensors are considered to functionalize screens and windows.

RELATED PUBLICATIONS:

[1] F. Casset et al., IEEE MEMS (2019), https://doi.org/10.1109/MEMSYS.2019.8870715

[2] G. Le Rhun et al., Transducers (2019) - EUROSENSORS XXXIIII, https://doi.org/10.1109/TRANSDUCERS.2019.8808241

High-Frequency Lithium Niobate Film Bulk Acoustic Resonator

RESEARCH TOPIC:

Lithium niobate $LiNbO_3$, Film Bulk Acoustic Resonator (FBAR), 5th Generation of mobile applications (5G), RF filters

AUTHORS:

A. Reinhardt, M. Bousquet, P. Perreau, C. Billard

X-cut and Y+163°-cut $LiNbO_3$ Film Bulk Acoustic Resonators (FBAR) with patterned bottom electrodes and a sacrificial layer cavity have been fabricated using a layer transfer process. Particularly, the Y+163° orientation provides a single resonance at 2.2 GHz, with an effective electromechanical coupling factor (k_t^2) of 26 %. Thanks to this single mode behavior and to the energy trapping induced by the heavy tungsten electrodes, the quality factor at antiresonance (Q_a) is increased up to 600. Moreover, a Temperature Coefficient of Frequency (TCF) of -45 ppm/°C is obtained. This demonstrates a significant improvement towards introducing $LiNbO_3$ as an alternative to AlN in Bulk Acoustic Wave (BAW) filters for the new generation of RF filters.

Context and Challenges

As the number of frequency bands is growing significantly with the deployment of the 5th Generation of mobile applications (5G), mobile communication systems require RF filters with increasingly stringent performances in terms of frequency, fractional bandwidth, temperature coefficient of frequency, skirt steepness, insertion loss and compactness. As a key metric for relative filter bandwidths, the electromechanical coupling factor can be adjusted by the choice of the piezoelectric material used to implement resonators and its crystal orientation (k2 ranging from 5 % to 45 % for bulk waves). Single-crystal lithium niobate (LiNbO3) appears as an appealing candidate to replace AlN and its derivatives (kt2 = 6.5 - 9 %) in Bulk Acoustic Wave (BAW) resonators. As this material is difficult to grow as a single crystal thin film by conventional deposition techniques, film transfer approaches such as wafer bonding and mechanical thinning or crystal ion slicing are privileged. Up to now, only few reports dealt with the integration of single crystal LiNbO3 films in BAW resonators.

Main Results

Sub-micron thick single crystal Film Bulk Acoustic Resonators (FBAR) based on X-cut and Y+163°-cut $LiNbO_3$ with patterned bottom electrodes (AlSi and W) and a sacrificial layer cavity have been fabricated using a layer transfer process [1]. Fig. 1 shows an optical microscope image of a fabricated resonator.

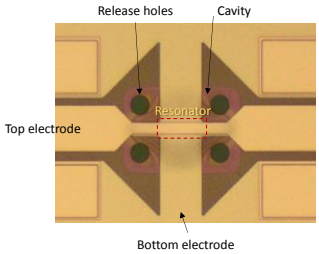
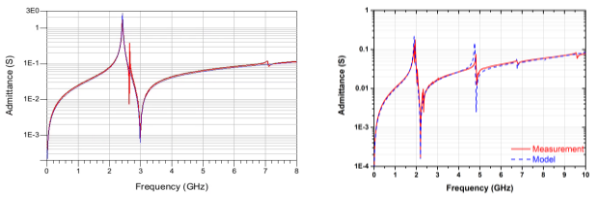


Fig. 1. Optical microscope photograph of a fabricated $LiNbO_3$ resonator

X-cut LiNbO3 FBAR displays resonance and antiresonance frequencies of 2.42 and 2.99 GHz, respectively, leading to a large electromechanical coupling factor of 39.2 %. The quality factor at antiresonance is close to 250 (Fig. 2a). Nevertheless, the existence of a second piezoelectrically active wave in X-cut LiNbO3 leads to a strong parasitic located between resonance and antiresonance [1].



(a) (b)

Fig. 2. Typical response of (a) X-cut and (b) Y+163°-cut ion-sliced $LiNbO_3$ Film Bulk Acoustic resonator

On the contrary, the Y+163°-cut is known to support only one piezoelectrically coupled shear wave and is expected to provide less spurious resonances Indeed the admittance curve of the Y+163°-cut $LiNbO_3$ FBAR reveals a stronger and cleaner response, with resonance and antiresonance frequencies of respectively 1.90 and 2.32 GHz, leading to an electromechanical coupling factor of 26 % (Fig. 2b). Thanks to this single mode behavior and to the energy trapping induced by heavy tungsten electrodes, the quality factors are this time evaluated to be 110 at resonance and 610 at antiresonance, pushing the impedance ratio to around 60 dB [2]. Finally, the temperature coefficient of frequencies of the series and the parallel resonances are equal to -61 ppm/K and -45 ppm/K, respectively, which is lower than the -80 ppm/K of X-cut $LiNbO_3$ FBAR [1].

Perspectives

Future work will be devoted to further improve performance, in terms of operation frequency, quality factor, spurious resonance mitigation and temperature compensation.

RELATED PUBLICATIONS:

[1] M. Gorisse et al, IEEE International Frequency Control Symposium & European Frequency Time Forum (2019).https://doi.org/10.1109/FCS.2019.8856017

[2] M. Bousquet et al, IEEE International Ultrasonics Symposium (2019). https://doi.org/10.1109/ULTSYM.2019.8925617

Silicon-Integrated Photoacoustic Sub-ppm Gas Sensor

RESEARCH TOPIC:
Silicon, MEMS, NEMS, piezoresistive nanogauges, photoacoustic spectroscopy, gas sensor

AUTHORS:
H. Lhermet, A. Glière, T. Verdot, A. Teulle, A. Berthelot, B. Desloges, F. Souchon, J.-G. Coutard

Downsizing and compatibility with MEMS silicon foundries is an attractive path towards a large diffusion of photoacoustic trace gas sensors.
For the first time, an on-chip integration of a photoacoustic detector was achieved. A 2.3 mm^3 silicon cell with a built-in piezoresistive pressure sensor has been designed. The components have been fabricated by microfabrication on the CEA-LETI 200 mm silicon platform.
Coupled with a quantum cascade laser source, this trace gas detector was characterized. Based on a compilation of experimental data, a sub-ppm limit of detection is demonstrated.

Context and Challenges
Integration on a silicon platform led to major successes in the recent years in the domain of micro-electromechanical systems (MEMS), enabling cost reduction and large-scale deployment.
The application of this strategy to photoacoustic (PA)-based trace gas sensors aims at a widespread usage for indoor and outdoor air quality measurement.
The scope of this paper is limited to the PA detection building block. To overcome the fundamental restrictions that faces the miniaturization of conventional photoacoustic detectors, we propose an integrated PA cell, which includes its own dynamic pressure sensor based on an innovative architecture.

Main Results
The PA detector consists in an illuminated chamber, separated from a closed expansion volume by a channel where a cantilever beam is placed. The beam in-plane motion produces a longitudinal stress inside two suspended piezoresistive Si nanogauges and is thus transduced into resistance variations; the amplitude of these variations is related to the gas concentration.

The PA detectors (Fig. 1) were fabricated in the CEA-Leti 200 mm silicon facilities using the so-called "M&NEMS" technological process.

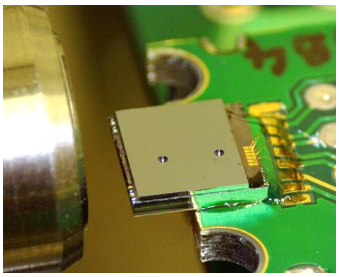


Figure 1: Photograph of a PA detector mounted on a printed circuit board and placed in the optical test bench.

Measurements were performed to assess the gas-sensing capabilities of the device. A methane and nitrogen gas mixture was injected through the fluidic port. The laser was wavelength-modulated at the mechanical resonance frequency of the cantilever beam and a 2-f detection scheme was performed to read the photoacoustic signal. Allan deviation measurements presented in Fig. 2 show that the long-term stability of the instrumentation chain is good, reaching its optimal performance for a 54 s integration time. The corresponding 1σ ultimate limit of detection (LOD1σ) is estimated to be 1.4 ppm. Similar measurements carried out on the same devices with a quantum cascade laser QCL tuned to the carbon dioxide absorption line led to a LOD1σ of 0.9 ppm for a 7 s integration time.

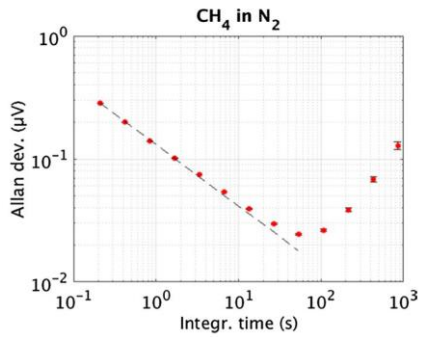


Figure 2: Allan deviation plot measurement of methane in nitrogen. The dashed line represents the fit by $\sqrt{\tau}$.

Perspectives
The ultimate goal is to develop a highly sensitive gas sensor combining, on the same chip, a mid-infrared laser, a light injection circuit, and this PA cell including an integrated pressure sensor.

RELATED PUBLICATIONS:
[1] H. Lhermet et al., IEEE Transducers, (2019), https://doi.org/10.1109/TRANSDUCERS.2019.8808295
[2] A. Glière et al., International Journal of Thermophysics, (2019), https://doi.org/10.1007/s10765-019-2580-7

A 3D Process for High Performance Capacitive Inertial Sensors

RESEARCH TOPIC:
MEMS - Inertial - 3D process - capacitive detection

AUTHORS:
F. Maspero, S. Delachanal, A. Berthelot, L. Joet, S. Hentz (G. Langfelder)[1]

A 3D process is proposed for inertial MEMS sensors where a thin layer allowing nanometric gaps for high-density comb fingers is patterned below a thick seismic mass layer. The objective is to achieve high-performance in a reduced footprint. This technology is compatible with surface-variation capacitive detection, enabling high dynamics. An in-plane and an out-of-plane accelerometers have been designed, fabricated with this new 3D process and tested under acceleration. Initial in-plane and out-of-plane devices demonstrate outstanding dynamic ranges for open-loop operation, respectively 150 dB/√Hz and 138 dB/√Hz, for a total footprint of 0.24 and 0.12 mm².

SCIENTIFIC COLLABORATIONS: [1]Politecnico di Milano, Italy

Context and Challenges

In most capacitive MEMS inertial sensors, the seismic mass and sensing elements are patterned in the same silicon layer. A thick layer increases seismic mass and decreases the Brownian noise floor, whereas a thin layer enables smaller gaps between electrodes and decreases electrical noise.
Our new technology overcomes this trade-off by providing two layers, a thin one and a thick one. It enables submicronic comb fingers and large mass on top of each other for small footprint.

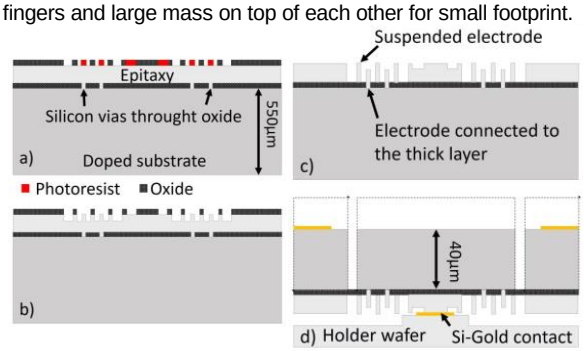


Fig. 1. Fabrication process flow

The fabrication process (fig. 1) starts with a doped substrate, covered by a 2 µm patterned oxide layer. 7 µm doped epitaxial Silicon is grown to form the thin layer. This layer is double masked (oxide and photoresist) to realize a twostep etching. It enables partial etching of electrodes to obtain out-of-plane surface varying comb-fingers. The wafer is reported on a holder wafer, previously prepared for eutectic bonding on contact points and cavities facing moving parts. The thick layer is thinned down to a few 10's µm and etched to form the proof mass, the springs and the release holes. Finally, the device is released by vapor-phase HF during a time-controlled etching.
This technology makes surface variation, intrinsically linear regardless of polarization voltage or gap size, very attractive.

Main results

A first run has been successfully processed and delivered functional devices. Figure 2 shows the thin layer side of 0.24 mm² in plane, and 0.12 mm² out-of-plane accelerometers.

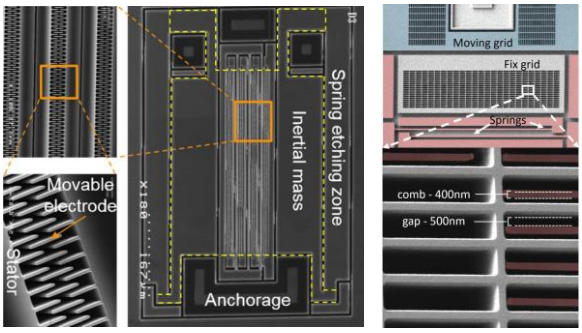


Figure 2: SEM images of the thin layer of a device

These devices present a 150 dB and a 138 dB dynamic (on 1 Hz) respectively, exceptional performance for open loop readout accelerometers. The in-plane accelerometers combines multiple advantages:

- ✓ High linearity due to surface variation (full scale = 190 g).
- ✓ High sensitivity due to 500 nm gap comb fingers (5.3 fF/g).
- ✓ Low Brownian noise due to 100 µm thick mass (7 µg/√Hz).

Moreover, the 4.8 kHz resonant frequency provides a large bandwidth and high stiffness prevents sticking.
The out-of-plane accelerometer performances are impacted by the 10 kHz resonant frequency, resulting from trade-offs required for this first debug process. In spite of this, the accelerometers presents a sensitivity of 0.74 fF/g, a Brownian noise of 27 µg/√Hz and a full scale range higher than 400 g.

Perspectives

The tuning of the out-of-plane accelerometer design should enable the same performances on the three axis.
It will be also interesting to use this technology for gyroscopes.

RELATED PUBLICATIONS:
[1] F. Maspero et Al., IEEE 32nd International Conference on Micro Electro Mechanical Systems (MEMS), (2019), https://doi.org/10.1109/MEMSYS.2019.8870681
[2] F. Maspero et Al., IEEE Sensors Journal, (2020), https://doi.org/10.1109/JSEN.2019.2942797

Towards Ultrasensitive and High Bandwidth Optomechanical AFM Probes

RESEARCH TOPIC:

AFM probe, high speed AFM, Optomechanics, force sensor, resonant sensor, silicon photonics, non-contact interaction

AUTHORS:

G. Jourdan, M. Gely, S. Hentz, L. Banniard, (L. Schwab, B. Legrand)[1], (P-E. Allain, I. Favero)[2],(M Faucher)[3], (B. Walter)[4]

VLSI optomechanical micro-resonators offer a new way to address high resolution and high speed AFM Imaging. Recent developments made by CEA-Leti and its partners in this field have implemented fully-optically operated resonating optomechanical AFM tips above 100 MHz, 2 decades above the fastest commercial cantilever probes. With Q-factors larger than 1000 in air, it offers large measurement bandwidths above 100 kHz. Low thermomechanical noise provides an exquisite motion detection limit down to a few 10^{-16} m.Hz$^{-0.5}$. It allows very low oscillation amplitudes down to a few tens of pm in operation, which is a prerequisite to probe molecular interaction at such a scale. This performance, enabled by optomechanical transduction, paves the way for high-speed and ultra-sensitive measurements in the field of molecular biophysics.

SCIENTIFIC COLLABORATIONS: [1]LAAS, [2]MPQ, [3]IEMN, [4]VMicro

Context and Challenges

Atomic Force Microscopy (AFM) is a versatile technique based on a resonating tip that interacts with a sample surface to probe its topography and its mechanical properties. Next-generation investigations in molecular biophysics like protein folding/unfolding, receptor-ligand interaction and molecular diffusion on cell membrane require molecular forces to be tracked at the nanosecond timescale in a non-perturbative manner. Conventional AFM probes, based on micro-cantilevers vibrating in the MHz range with nanometer amplitudes and tracked by an optical deflection detection system, are the current bottleneck to reach the required performances. A very low and a non-perturbative vibration amplitude, a high time resolution and measurement bandwidth, are all impacted by the same chief parameter [1]: the resonance frequency of the mechanical probe. While a higher frequency unlocks the bandwidth and the time resolution, it also sets the Brownian motion low enough to provide exquisite signal-to-noise ratio and force resolution even for vibration amplitude in the picometer range, *i.e.* much lower than the molecular dimensions. Recent advances in optomechanical device technology can tackle this challenge by offering resonators at very high frequencies above the GHz range and motion sensitivity below 10^{-17} m.Hz$^{-0.5}$.

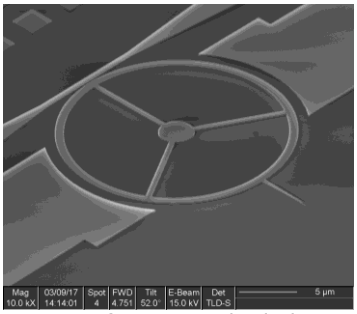


Figure 1: SEM Image of an optomechanical AFM probe before substrate etching below the tip area

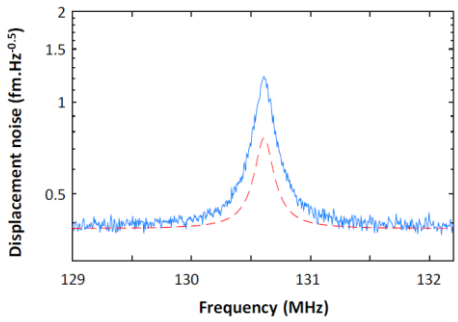


Figure 2: Brownian motion of the optomechanical AFM probe measured at 1 Hz bandwidth

Main Results

The probe, depicted in Fig. 1, consists of a suspended silicon ring, on which a sharp tip has been clamped. The photonic cavity is addressed by a silicon waveguide coupled with two optical fibers to feed the device with a laser beam and a photodiode. A dedicated etching process will provide an overhanging tip outside the substrate, to allow the probe approach to a sample surface. Approach retract experiments have demonstrated the large bandwidth of the device required to track fast biophysical phenomena [2]. Brownian motion has been resolved down to a few 10^{-16} m.Hz$^{-0.5}$ (Fig. 2). It allows the oscillation amplitude to be kept below tens of pm, well below usual AFM probes (around 1 nm), while providing very high signal-to-noise ratio, larger than 10^4, required for high resolution measurements. Both aspects prove the capabilities to probe molecular interactions at the close vicinity of a surface and at very short time scales [2-3].

Perspectives

Optomechanical AFM probes are a promising tool to study biological systems like proteins, viruses, etc. It provides a way to push AFM Imaging to high-speed analysis of biological properties of these species. In particular, ultra-fast force spectroscopy is expected to deliver valuable information about the relation between their conformation and their function.

RELATED PUBLICATIONS:

[1] L. Schwab et al., International Conference on Quantum Metrology and Sensing, (2019), . https://tel.archives-ouvertes.fr/DRT/hal-02407634v1

[2] P.E. Allain, et al., Nanoscale (2020);12(5):2939-2945. https://doi.org/10.1039/C9NR09690F

[3] L. Schwab et al., IEEE MEMS, (2019),. https://doi.org/10.1109/MEMSYS.2019.8870718

Biosensing with Graphene Transistors

RESEARCH TOPIC:
MEMS, NEMS & RF COMPONENT

AUTHORS:
T. Alava, J. Simon, A. Hugo, M. Kumar, P.I Mailley (J. Renard, V. Bouchiat)[1], (J. Parpia, H. Craighead)[2], (W. Dichtel)[3]

Graphene is the thinnest and strongest material, its ability to maintain high electrical conduction even under important deformation makes it ideal for future wearable electronic devices. Its ultimate surface-to-volume ratio makes it an ideal candidate for biosensing with charge detection. CEA-Leti has developed a unique fabrication protocol to realize graphene transistors that, when operated in liquid medium, become outstanding transducers of charged biological molecules. We show here the proof of concept of graphene-based biosensing with the first results of specific biological detection.

SCIENTIFIC COLLABORATIONS: [1]Institut Néel (CNRS, Grenoble), [2]Cornell University (USA), [3]Northwestern University (Chicago, IL, USA)

Context and Challenges

An electrical biosensor involves the conjunction of two elements: 1 - a device with electrical properties that can be altered by the presence of charged molecules from a liquid solution atop its surface, combined with 2- a layer of solidly attached biological molecules to which the desired biological target will bind. In the constant quest for more sensitive solid state electrical biosensors, sensors made from silicon transistors have been shrunk down to nanometre scale and have reached outstanding sensitivities (down to pM range). Yet, they still fail to withstand deformation and they are not adapted to flexible electronic systems. Inversely, graphene, a one atom thick layer of carbon atoms, can maintain outstanding electronic conduction even when suffering high deformation. Graphene has therefore been investigated in electronic-based charge sensitive biological sensors. In particular, solution-gated graphene field effect transistors have shown promising results. In this configuration, a graphene channel connects a source and a drain and its conductivity can be tuned by varying the electrical potential applied to the liquid solution atop the graphene layer. When properly functionalized with sensitive biological molecules, this device can be used as a biological sensor. Figure 1 shows the working principle of a SGFET graphene biosensor principle. Adsorption of charged biological molecules disrupts an electrical double layer present near the graphene/liquid interface.

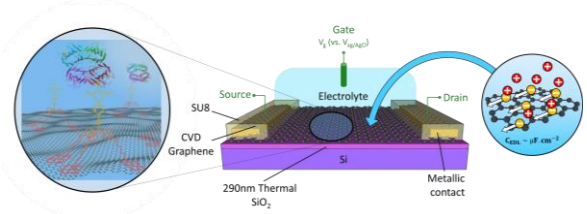


Figure 1: Schematic of a graphene solution-gated field effect transistors zooming on: the electrical double layer and the adsorption of biological molecules on a layer of biological functionalization

The detection is performed through a change of the SGFET electrical properties.

Main Results

We have developed an original fabrication protocol for graphene-based solution-gated FETs with very good yield. This protocol also maintains optimal graphene surface cleanliness even on large graphene area, enabling large capture area sensors. Figure 2.a. shows a graphene device between source and drain gold contacts. Electrical performances of our devices match state-of-the-art devices. We have then implemented an innovative functionalization protocol with the help of Professor William Dichtel of Northwestern University and we have been able to record specific adsorption of protein target on our sensors (Fig 2.b).

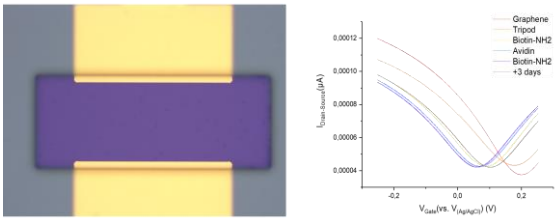


Figure 2: (a) Micrograph of a graphene SGFET sensor between two gold contacts (b) Electrical conduction properties of the SGFET after different adsorption of charged molecule and detection of target

Perspectives

We are now seeking to integrate multiple sensors on the same chip to multiplex biological detection; we intend as well to transfer our fabrication protocol to other substrates. We have achieved fabrication on glass and silicon and are currently pursuing fabrication on polyethylene flexible substrates.

RELATED PUBLICATIONS:
[1] A.Hugo et al, Graphene2019 (2019), June 25-28, Rome, Graphene 2019
[2] A. Hugo et al, (2019), October 20-25, Colombus (USA), AVS Symposium 2019

First MEMS Microphone Based on Capacitive Transduction in Vacuum

RESEARCH TOPIC:
MEMS - Microphone - capacitive detection

AUTHORS:
S. Dagher, A. Berthelot, C. Ladner, F. Souchon, L. Joet, (S. Durand)[1]

This innovative technology enables the realization of microphones composed of a pressure-harvesting rigid piston in air, mechanically linked through an airtight hinge to a capacitive transducer enclosed in a vacuum cavity. In theory, this separation should lead to very low acoustical and mechanical noises, thereby increasing the overall microphone performance (estimated SNR>75 dB(A)). First wafer-level tests give a clear proof-of-concept of this new microphone design, with a resonance frequency of 19 kHz and a measured sensitivity of 6 fF/Pa.

SCIENTIFIC COLLABORATIONS: [1]Laboratoire Laboratoire d'Acoustique de l'Université du Mans

Context and Challenges
Increasing demand for ever-higher performance has pushed the current simple condenser design of MEMS microphones to its limits. Increasing the performance is only possible at the cost of a larger chip and back-volume (BV) size.
In fact, performing the capacitive transduction in air leads to unavoidable squeeze film damping and acoustical resistance between the deformable membrane and the backplate, which is the dominant noise source in these microphones (Fig. 1).

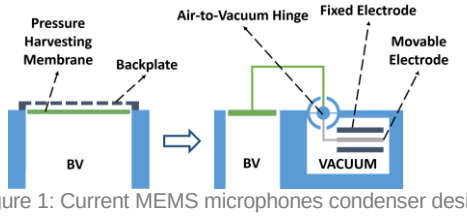


Figure 1: Current MEMS microphones condenser design / proposed air-to-vacuum transmission design

This innovative technology consists in splitting the microphone into a pressure harvesting membrane in air linked to a capacitive transducer sitting in vacuum. An airtight mechanical hinge, able to transfer a displacement from one atmosphere to the other, ensures the connection between the two parts (Fig. 1.). By removing the backplate, this method drastically reduces viscous damping effects, thereby increasing overall microphone performance.

Main Results
A first device based on this technology has been designed (Fig. 2). At the center, a light and rigid piston sits on top of a BV and moves out-of-plane under an incoming pressure difference. Four airtight hinges, mechanically linked to the piston, transmit its movement to two lateral electrodes enclosed in separate vacuum cavities.
Sitting on opposite sides, the electrodes move in the opposite direction of the piston between top and bottom electrodes.

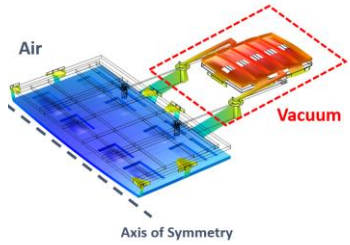


Figure 2: FEM simulation of structure half

A first run has been successfully processed and delivered functional devices (Fig. 3).

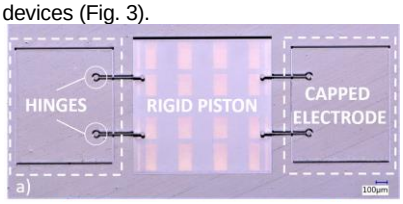


Figure 3: Optical microscopy images of the airside of the microphone (a)
and of an uncapped electrode (b)

Preliminary tests have been performed at wafer level. By using acoustical or electrical actuation, optical and electrical detection, they have proven:

- ✓ Correct operation of the hinges, establishing the link between the electrodes and the piston.
- ✓ Expected out-of-plane translation of the piston.
- ✓ 19 kHz resonance frequency
- ✓ Expected 6±0.5 fF/Pa sensitivity

Perspectives
Dicing and die level tests are the next steps, to confirm the expected good performance. at the same time, the process flow is fine-tuned to reduce its cost by 50 %.
It would be interesting to use this technology on absolute and relative pressure sensors.

RELATED PUBLICATIONS:
[1] S. Dagher et al, IEEE TRANSDUCERS & EUROSENSORS XXXIII, (2019), https://doi.org/10.1109/TRANSDUCERS.2019.8808741
[2] S. Dagher et al, IEEE MEMS (2020),10.1109/MEMS46641.2020.9056307

Near-Zero Energy Computing Based On Contactless MEMS

RESEARCH TOPIC:

Electromechanical computing, ultra-low-power computation, capacitive adiabatic logic, energy-recovery computation, MEMS

AUTHORS:

G. Pillonnet, H. Fanet, L. Hutin, Y. Perrin, A. Galisultanov, (P. Basset)[1]

To overcome the inherent trade-off between leakage and conduction losses in transistor-based computing circuits, we have currently studied a novel computing solution mixing controlled slew-rate logic switching, logic-energy recovery and inherent zero-leakage operation. We have reported a hardware implementation based on gap closing and comb-drive MEMS. This logic paradigm avoids any mechanical contact, thus dramatically improves the main limitation of other MEMS-based logic systems. In 2019, we have published the gap-closing MEMS topology and associated model to predict the scaling performance (speed, surface, energy). We have also reported the fringing effect of symmetrical comb-drive actuators on the non-adiabatic loss *i.e.* the minimal achievable energy by these devices.

SCIENTIFIC COLLABORATIONS: [1]ESYCOM (ESIEE Paris)

Context and Challenges

Considerable efforts have been devoted to the design of low-power digital electronics. However, after decades of improvements and maturation, CMOS technology could face a power efficiency ceiling. This is due to the trade-off between leakage and conduction losses inherent to the limited subthreshold slope of any semiconductor junction *e.g.* FET. Consequently, the lowest dissipation per operation (~10's aJ) remains nowadays a few decades higher than the noise floor (100 K_BT) and the theoretical Landauer's limit (3 zJ at 300 K). CMOS scaling, better electrostatic gate control (FinFET, FDSOI…) or alternative FET structure (TFET, NC-FET…) do not drastically change this previous statement. It is therefore clear that there is room for new devices eventually based on new logic operation concepts to dramatically reduce the power dissipation of digital operations.

On the logic operation side, energy-recovery computation (also called adiabatic) is a good candidate for reducing the dynamic losses due to charge-based information coding. But adiabatic operation reduces operating frequency, thus exacerbating the inherent leakage loss of FET devices. Consequently, we propose new Boolean systems with contactless logical operations called CAL. The contactless property eliminates the leakage loss, breaking the previously mentioned trade-off to efficiently work in adiabatic style.

Main Results

Papers [1] and [2] report the design, energy analysis and logic functionality of four-terminal variable capacitors based on silicon nano/micro technologies and intended to achieve adiabatic logic functions with a better efficiency than by using field effect transistors (FET). By removing any mechanical contact, we have solved the inherent reliability problem of microrelays to allow billions of billions of logic operations over the lifetime of the future MEMS-based processors.

The proposed MEMS device consists of two capacitors mechanically coupled and electrically isolated, where a comb-drive input capacitor controls a gap-closing capacitor at the output (Fig. 1). To fully implement the adiabatic combinational logic, we propose two types of variable capacitors: a positive variable capacitor (PVC) where the output capacitance value increases with the input voltage, and a negative variable capacitance (NVC).

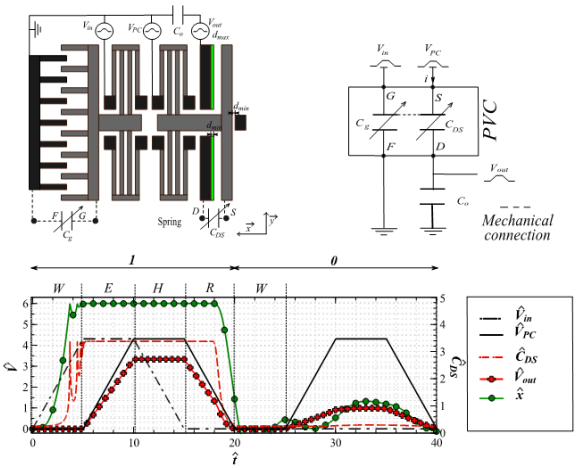


Figure 1: 4-terminal MEMS mixing gap-closing and comb-drive actuation as an elementary element of the CAL logic

A compact and accurate electromechanical model has been developed. The electromechanical simulations demonstrate high logic states differentiation larger than 50 % of the full-scale input signal and cascability of both buffers and inverters. Based on the presented analysis, 89% of the total injected energy in the device can be recovered, the remaining energy being dissipated through mechanical damping (0.9 fJ).

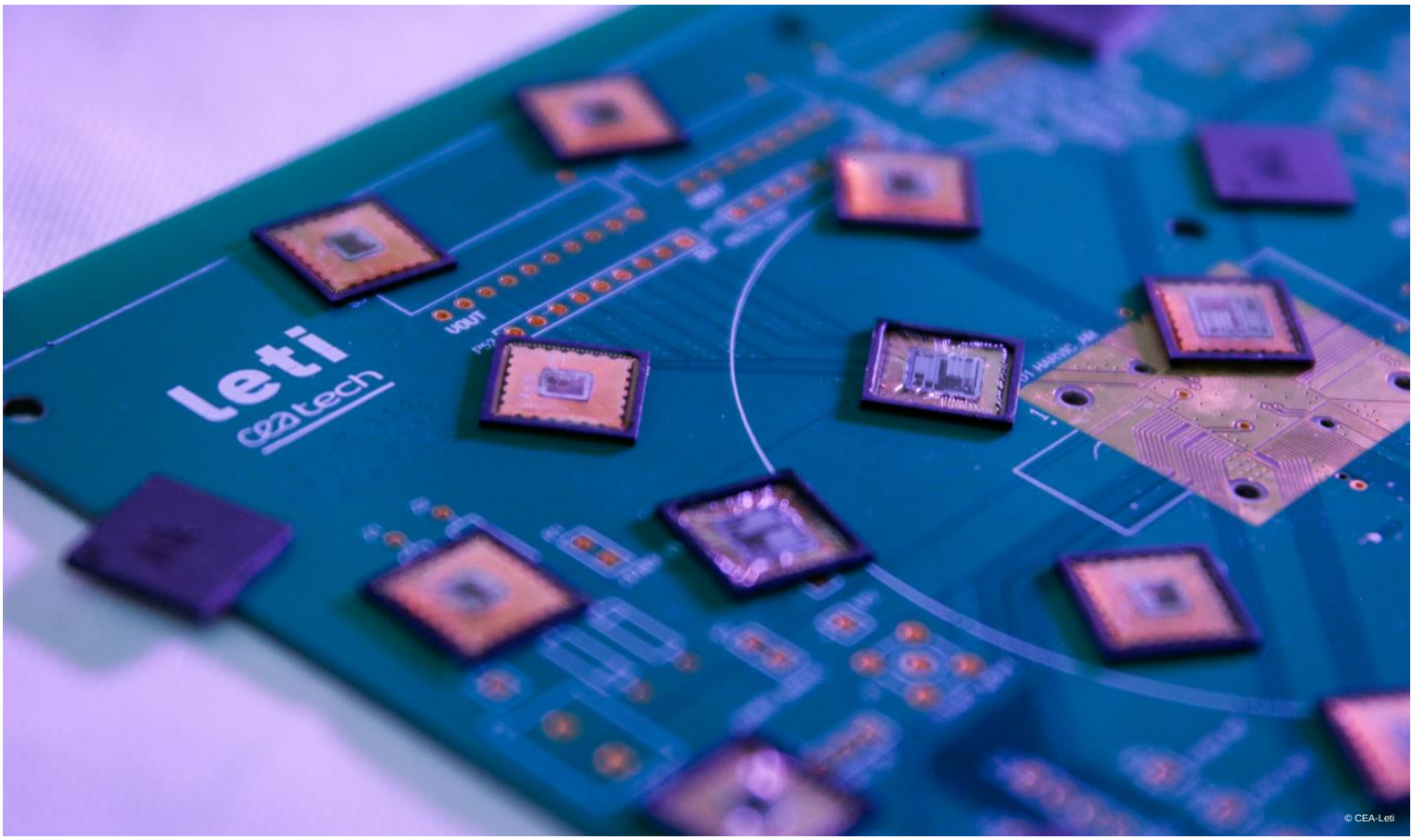
Perspectives

We are currently studying parallel-plate MEMS operated in a liquid dielectric to reduce the gate sizing and increase the operating frequency. We are also considering non-MEMS devices to implement the CAL.

RELATED PUBLICATIONS:

[1] H. Samaali et al., Nano Energy, (2019), https://doi.org/10.1016/j.nanoen.2018.10.059

[2] A. Galisultanov et al., Journal of Physics: Conference Series, (2019), https://doi.org/10.1088/1742-6596/1407/1/012087



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05 POWER & ENERGY

- Advanced AlN and InAlN Barriers in GaN Based Hetero-Structures for High Electron Mobility Transistor (HEMT) Devices
- TCAD to Support Threshold Voltage Instabilities in GaN-on-Si E-mode MOSc-HEMT
- Traveling Wave Piezoelectric Transformers for AC-AC Power Converters Integration
- Frequency and Damping Adjustments of Electromechanical Resonators by the Electrical Interface: Exploiting the Piezoelectric Coupling
- Millimeter Scale Thin Film Batteries to Power up Extended Applications

Advanced AlN and InAlN Barriers in GaN Based Hetero-Structures for High Electron Mobility Transistor (HEMT) Devices

RESEARCH TOPIC:

Development of nitride barrier layers with lower sheet resistance to improve power and RF transistor performance

AUTHORS:

M. Charles, M. Mrad, J. Kanyandekwe, R. Bouveyron, Y. Mazel, E. Nolot, P. Ferret, M. Veillerot, Y. Baines, J. Richy, S. Favier, C. Leroux, D. Blachier, J-P. Barnes, C. Weise, G. Feuillet

Typical power or RF transistors for HEMT devices use AlGaN barriers on GaN channel layers. However, with this alloy it is difficult to achieve sheet resistance values much below 300 Ohm/sq. In this work, we have developed both InAlN and AlN barrier layers in order to achieve lower values, and so to enable higher performance transistors. For InAlN, we have managed to eliminate the known problem of gallium pollution, using regrowth, gas flow and hardware modifications. We now have excellent control of InAlN layers, leading to sheet resistance values below 200 Ohm/sq.

AlN layers were found to be very sensitive to thickness and growth conditions, but despite these difficulties we achieved sheet resistance values approaching the best seen for AlGaN barriers.

Context and Challenges

For both RF and power applications, there is a desire to reduce the sheet resistance of the layers to lower the device resistance, and to improve high frequency operation. AlGaN layers are typically used for these devices, but it is difficult to achieve values much below 300 Ohm/sq with this material. LETI has therefore developed both AlN and InAlN layers, which should allow values below 200 Ohm/sq.

Main Results

Previous studies of InAlN barriers have shown that for AIXTRON close coupled showerhead growth chambers, as shown in Fig.1, gallium is unintentionally integrated into the InAlN layers. This has the effect of reducing the performance of the layers, and making their control more difficult.

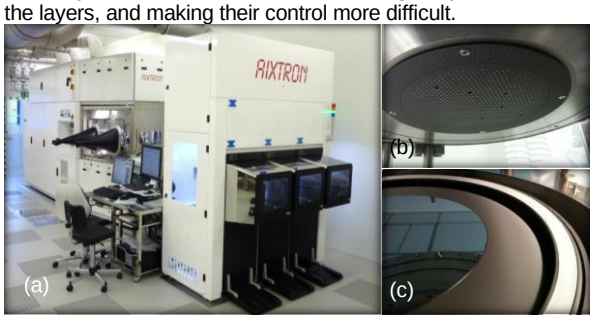


Figure 1: (a) AIXTRON growth tool, (b) showing showerhead with shield, (c) wafer on chuck

Having demonstrated (see 2016 scientific report) a link between gallium pollution and the indium precursor flow, we showed that by using regrowth after chamber cleaning, we could produce InAlN layers without gallium contamination [1]. We also showed that the pollution depends additionally on the quantity of gallium deposited in the chamber. Although these InAlN layers were gallium free, their electrical properties were impacted by the regrowth interface.

We hypothesised that the gallium pollution was coming from metallic gallium condensing on the shield on the showerhead, and so to avoid it, we looked at ways to heat the shield. By changing the main gas flow (from H_2 to N_2) and also by modifying the hardware, we managed to increase the shield temperature from 185°C to over 300°C. This resulted in a significant decrease in gallium pollution from 20% to less than 2%, as seen in Fig.2 [2].

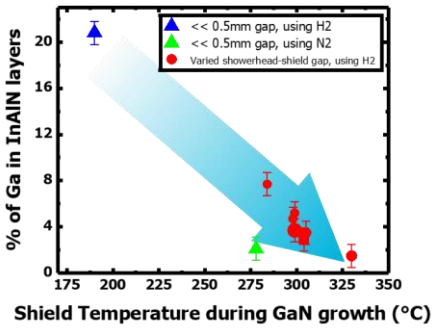


Figure 2: Strong reduction in gallium pollution using higher temperature showerhead shield and N_2 or H_2 carrier gas

In parallel, work on AlN barrier layers showed that they are very sensitive to thickness and to growth conditions, and it is suspected that this is also linked to gallium incorporation in the layers. It was, however, very difficult to prove this as small quantities of gallium are very difficult to detect in 3 nm thick AlN layers on GaN. Despite these difficulties, we achieved state of the art sheet resistance values <330 Ohm/sq.[3]

Perspectives

Having achieved very low or no gallium pollution in InAlN layers grown in a showerhead reactor, shown for the first time worldwide at LETI, we can now correctly control these layers. Along with the understanding of AlN barrier layers, we are now well positioned to achieve very low resistance layers, with our current unpublished values below 180 Ohm/sq.

RELATED PUBLICATIONS:

[1] M. Mrad et al., Journal of Crystal Growth, (2019), https://doi.org/10.1016/j.jcrysgro.2018.10.039
[2] M. Mrad et al., Applied Physics Express, (2019),https://doi.org/10.7567/1882-0786/ab0bbb
[3] J. Kanyandekwe et al., Journal of Crystal Growth, (2019), https://doi.org/10.1016/j.jcrysgro.2019.03.007

TCAD to Support Threshold Voltage Instabilities in GaN-on-Si E-mode MOSc-HEMT

RESEARCH TOPIC:

GaN-on-Si, MOS channel HEMT, TCAD, GaN HEMTs, nBTI, pBTI

AUTHORS:

M.-A. Jaud, W. Vandendaele, A. Viey, R. Gwoziecki, (F. Lucolano)[1], (G. Meneghesso)[2],(G. Ghibaudo)[3]

Leti and STMicroelectronics are cooperating to develop and industrialize advanced GaN-on-Silicon diode and transistor technologies for low loss power switching. In this context, transistor threshold voltage (Vth) instabilities are a great concern since they are known to severely affect the dynamic performance of the transistor during operation. This year we have investigated these instabilities by using ultra-fast negative and positive Bias Temperature Instabilities (nBTI & pBTI) supported by TCAD simulations on MOS-channel HEMT devices. This advanced characterization/TCAD simulations coupling allowed us to clarify the nBTI and pBTI transients as a function of the gate length and the stress conditions.

SCIENTIFIC COLLABORATIONS: [1]STMicroelectronics, [2]Padova University, [3]IMEP-LAHC

Context and Challenges

GaN-on-Silicon HEMT technologies draw significant attention for medium power applications (650V and below) due to GaN high breakdown electric field and transport properties such as mobility and saturation velocity compared to SiC technologies. Specifically, to limit power loss during switching and to simplify circuit configuration, normally-off devices, such as MOSc-HEMT architecture, are required for power switching applications. However, recent n/pBTI on E-mode pGaN gate HEMTs or on MIS gate configuration start to show significant Vth instabilities, which would severely affect the dynamic performance of the transistors during operation. Consequently, Vth instabilities of our transistors have been characterized through ultrafast Vth Measurement Stress Measurement (MSM) sequences, also called ultrafast BTI, as well as through TCAD simulations to support experimental interpretations.

Main Results

TCAD simulations are of great interest for in-depth understanding of experimental results especially when 2D and coupling effects become predominant as it is the case for a full gate recess MOSc-HEMT with specific epitaxy stack embedding a back barrier. We demonstrate experimentally that, contrary to pBTI, nBTI transients exhibit a dependence with gate length and stress voltage (Fig. 1) [1].

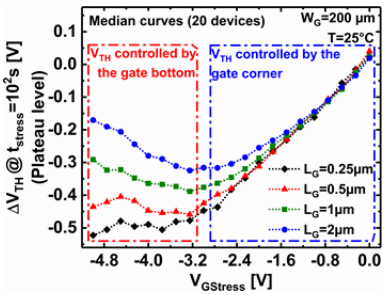


Figure 1: ΔVth after a stress time of 100s. A strong divergence can be noticed between the short and long gate lengths

For pBTI, electric field distributions obtained by TCAD simulations show the same electric field whatever the gate length and the stress voltage, which is in accordance with experimental measurements. On the contrary, electric field modulus in the case of nBTI is complex because it depends on gate length and evolves differently in the gate corners or in the bottom of the gate as a function of stress voltage (Fig. 2) [1]. Consistent analysis of these 2-dimensionnal electric field distributions coupled with experimental nBTI allow us to propose a model for Vth instabilities for fully recessed gate as detailed on Fig. 1.

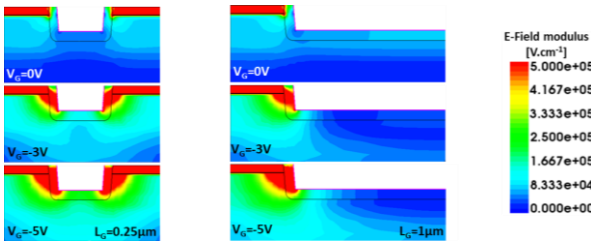


Figure 2: TCAD electric field modulus distribution of the gate for L_G=0.25um and 1um at V_G=0,-3 and -5V. This illustrates a reverse evolution of the electric field as a function of stress voltage for L_G=0.25um and L_G=1um

Perspectives

TCAD simulation is a strong asset to support electrical characterization and to confirm hypothesis but also to precisely understand device operation [2], mechanisms and phenomena. At LETI, TCAD intensively support GaN-on-Silicon power device developments. To improve Vth instabilities and also reduce current collapse as well as current in the OFF state, it is crucial to understand vertical leakage currents and trapping effects in GaN substrates on Si. In close collaboration with the electrical characterization team, we plan to use simulation to model these effects with the aim to reduce device instabilities.

RELATED PUBLICATIONS:

[1] A. G. Viey et al., IEEE IRPS conference, (2019), https://doi.org/10.1109/IRPS.2019.8720554

[2] A. G. Viey et al., IEEE IEDM, (2019), https://doi.org/10.1109/IEDM19573.2019.8993588

Traveling Wave Piezoelectric Transformers for AC-AC Power Converters Integration

RESEARCH TOPIC:
Piezoelectric transformers, power converters, traveling wave transformers.

AUTHORS:
G. Pillonnet, (T. Martinez, F. Costa, D. Vasic)[1]

We propose a new working principle to enhance the piezoelectric transformer inherent properties in AC-AC power converters. Instead of using standing waves to electromechanically transfer the energy from the primary to the secondary side, a traveling mechanical wave is generated from multiple piezoelectric primary electrodes then transduces into multiple phase-shifted electrical signals in the secondary side. This concept allows a new type of cycloconverters i.e. the generation of isolated output AC signal directly from AC sources without rectification. As no DC-AC conversion in the power path is needed, the power efficiency, bill of material and footprint can be reduced. The results pave the way to a seamless integration of power converters on silicon without magnetic material.

SCIENTIFIC COLLABORATIONS: [1]Laboratoire SATIE, ENS Paris-Saclay

Context and Challenges

The use of piezoelectric transformers in large applications, despite being explored during the 1950's, increased in the beginning of the 1990's for applications in backlighting of LCD screens, especially the Rosen-type piezoelectric transformer. In addition to their high voltage gain and compactness, the piezoelectric transformers present high power density, high efficiency due to their high quality factor, strong galvanic isolation and low electro-magnetic emissions compared to magnetic transformers. Nowadays, their inherent advantages find a new interest in the isolated gate-driving circuit, resonant DC-DC converters, ozone generation for medical and sanitary applications, plasma generation, in space applications or for start-up and impedance matching in harvesting applications.

In all aforementioned cases, piezoelectric transformers always work following the same principle: a generated standing wave from primary side is exploited to produce a single electrical signal in secondary side as the magnetic transformers operate. Contrary to magnetic one, the mechanical wavelength permits to catch the wave at different phases with multiple electrode configurations. The combination of the generated multiple signals allows a direct AC-AC conversion. To ensure this operation mode, a travelling wave has to be generated instead of a standing wave in the piezoelectric transformer, leading to the objective of this work.

Main Results

We propose a new working principle for piezoelectric transformers where longitudinal or flexural traveling waves are generated. This traveling wave piezoelectric transformer (TWPT) allows the creation of a multiphase system of voltages at the secondary side that would enable different power conversions: multi-phased rectification or DC to AC conversion with variable frequency. In the prototype presented in fig.1, the TWPT consists in a hollow thin cylinder with a particular electrode scheme using longitudinal waves. We proposed an analytical and black box modelling of the piezoelectric transformer based on the representation of the system by an admittance matrix characterizing the coupling between electrodes. This modelling allows to obtain electrical quantities based on material and geometrical properties of the TWPT.

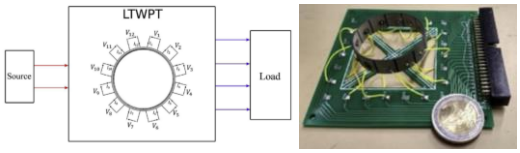


Figure 1: Multiple input/output electrodes in a cylinder geometry for longitudinal travelling wave and prototype [1]

Experimental validation is done on a TWPT based on a hollow thin cylinder with 12 electrodes. In this particular configuration, the proposed transformer can output a four-phase system. For input amplitude of 30 V, the TWPT delivers 6.5 W output power and reaches 90% efficiency for a cylinder of 20 mm radius, 1 mm thickness and 10 mm depth. This first prototype to validate the concept offers 0.52W/mm^3 power density. The simulation on the scaling effect shows a promising 5.4W/mm3 for 1.22cm^3 with manageable thermal considerations. The experimental data also validates the proposed modelling. We have now a simulation platform [1-3] to explore various geometry flavors. We have also validated the TWPT in a cycloconverter topology to generate various kHz output signals from 100kHz AC input with an open-loop control supervisor. We have also validated the TWPT principle using flexural travelling wave with a ring structure. This TWPT delivers 5.5mW in a 500µm thickness [2].

Perspectives

These first results validate the new working principle proposed by our team in collaboration with the SATIE research laboratory. The next step is to develop an integrated version of TWPT in our cleanroom. The expected higher resonant frequency allows to increase the operating frequency thus the power density and thickness to address point-of-load applications.

RELATED PUBLICATIONS:
[1] T. Martinez, et al., Sensors and Actuators, A: Physical, (2019), https://doi.org/10.1016/j.sna.2019.04.014
[2] T. Martinez, et al., Smart Materials and Structures, (2019), https://doi.org/10.1088/1361-665X/ab1945
[3] T. Martinez, et al., Proc. SPIE, vol. 10967, (2019), https://doi.org/10.1117/12.2514448

Frequency and Damping Adjustments of Electromechanical Resonators by the Electrical Interface: Exploiting the Piezoelectric Coupling

RESEARCH TOPIC:

Electromechanical coupling, piezoelectric generator, energy harvesting, integrated circuits.

AUTHORS:

A. Morel, G. Pillonnet, A. Quelen, P. Gasnier, S. Boisseau, G. Despesse, (A. Badel)[1], (E. Lefeuvre)[2]

One of the main challenges in energy harvesting from ambient vibrations is to find efficient ways to scavenge the energy, not only at the mechanical system resonance but also over a wider frequency band. Instead of tuning the mechanical part of the system, as usually proposed in the state of the art, we have developed extensively the possibility to tune the properties of the harvester using the electrical interface. Due to the progress in materials, piezoelectric harvesters can exhibit relatively high electromechanical coupling: hence, the electrical part can now have a substantial influence on the global parameters of the piezoelectric system. We have developed various harvesting strategies by introducing controlled energy transfers from mechanical, piezoelectric and electrical parts.

SCIENTIFIC COLLABORATIONS: [1]SYMME (Univ. Savoie Mont-Blanc), [2]IEF (Univ. Paris Sud)

Context and Challenges

The energy harvesting system from ambient vibrations suffers from low immunity against electromechanical transductor shifts (aging, temperature, process) or slight stimuli frequency variations, limiting the widespread deployment of vibration energy scavenging systems. To overcome their inherent low robustness, we propose to tune the damping and stiffness induced by the electrical interface through the electromechanical piezoelectric coupling. In the last decade, emerging high-coupling piezoelectric materials leveraged by adequate mechanical designs offer higher electromechanical coupling while maintaining high quality factor. Therefore, a system-level approach associating the resonator and electronic interface offers a room to enhance the frequency bandwidth where energy harvesters efficiently transduce various vibrations in a compact volume.

Main Results

Our paper [1] introduces a new strategy called SC-SECE to induce efficiently a shift of resonator dynamic based on piezoelectric coupling. By controlling the energy-harvesting phase, the electrical interface impacts on the equivalent stiffness and damping of the structure. We analyze and analytically derive the influences of electrical tunable parameters (here, the short circuit duration and the initial phase) on the harvester dynamics, and prove that they both affect the damping induced by the electrical interface on the mechanical resonator and its resonant frequency (Fig.1). Thereafter, we numerically evaluate the SC-SECE performances as a function of the intrinsic harvester's characteristics. We expose that if the coupling and/or mechanical quality factor of the harvester are important enough, the SC-SECE leads to enhanced power frequency responses compared to prior art. Experimental results on a high coupling PEH associated with the SC-SECE strategy have been obtained and are in good agreement with the analytical predictions. Under various vibrations amplitudes, the harvester's resonant frequency has been tuned on a frequency range as large as 35% of its natural resonant frequency. We have been able to harvest more than 92 µW for vibration frequencies ranging from 90 to 140 Hz, under an external acceleration of 0.2 G.

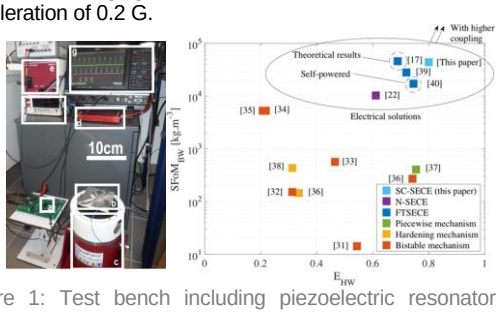


Figure 1: Test bench including piezoelectric resonator and electrical interface and comparison to prior art

In [2], we present an analytical analysis of the influences of the resistive and reactive behavior of the electrical interface on highly coupled piezoelectric harvesters. We develop a normalized study of the multiphysics interactions, reducing the number of parameters of the problem to a few physically meaningful variables.

In [3], we propose another strategy called Tunable Hybrid SSHI. This strategy combines features of the two existing SSHI techniques. We prove analytically and numerically that with a fine combination of those two strategies, the harvesting bandwidth can be sensibly increased. Associated with a high coupling harvester, the harvesting bandwidth is 3 times larger compared to the series and parallel SSHI.

Perspectives

The next step is to integrate these harvesting strategies into integrated circuits to allow self-powered operation even at low acceleration level. The technique could be also applied to other electromechanical transductions such as electrostatic or electromagnetic coupling. Other applications could benefit from the tunable frequency e.g. wireless energy transfer or N/MEMS-

RELATED PUBLICATIONS:

[1] A. Morel et al., Smart Materials and Structures, (2019), https://iopscience.iop.org/article/10.1088/1361-665X/aaf0ea

[2] A. Morel et al., Journal of Intelligent Material Systems and Structures, (2019), 10.1177/1045389X18810802

[3] A. Morel et al., Journal of Physics Conference Series, (2019), 10.1088/1742-6596/1407/1/012060

Millimeter Scale Thin Film Batteries to Power up Extended Applications

RESEARCH TOPIC:
Thin film, batteries, on-chip energy storage, solid state

AUTHORS:
S. Oukassi, A. Bazin, C. Secouard, I. Chevalier, S. Poncet, S. Poulet, J-M. Boissel, F. Geffraye, J. Brun, R. Salot

LETI's work on miniaturized energy-storage involves optimization of numerous elements in order to improve performance. Last year we developed a high energy-density millimeter-Scale thin film battery integrating 20 µm thick $LiCoO_2$ cathode in a Li-free anode configuration. We demonstrate an areal energy density of 890 µAh.cm^{-2}, the highest reported so far for such devices. Furthermore, we show that the new thin film battery architecture exhibits high power density, reaching capacities as high as 450 µAh.cm^{-2} under 3mA.cm^{-2} current density. Based on these superior properties, our TFBs show strong potential to be utilized as integrated energy storage units in various emerging applications, in particular for the medical field.

Context and Challenges
The sustained miniaturization of electronics has emphasized the need for highly integrated electrochemical energy storage. Energy storage at the point of load can reduce energy dissipated from power loss and I/O switching noise that can plague sensitive devices while enabling unique form factors. Thin film batteries provide some of the highest energy densities of electrochemical energy storage devices but the inability to increase the electrodes thicknesses and control the geometry on the micrometer scale has thus far hindered their effective areal energy density and integration in miniaturized devices.

Main Results
For the first time, we experimentally demonstrated thin film batteries (TFBs) with very high electrochemical energy density storage of 0.89 mAh.cm^{-2} at the device level. The 3.1×1.7 mm^2 TFB (Fig. 1.a) of 95 µm total thickness shows a discharge capacity of 25 µAh and maintains 60% of this value at 0.25mA. Upon cycling, TFBs exhibit excellent capacity retention, with an average loss of 0.05% per cycle. Furthermore, Results at 37°C exhibit almost similar performance, thus highlighting the great potential of these TFBs as integrated energy storage solution in particular for medical implantable, injectable and wearable solutions.
These results are explained by both a high lithium ion diffusion coefficient in $LiCoO_2$ measured around 5.10^{-9} cm^2.s^{-1} and a high LiPON ionic conductivity of 3.10^{-6} S.cm^{-1}. It is expected that lowering the LiPON thickness (3 µm for this work) will allow for a further decrease of total internal resistance and consequently a higher rate capability.
As compared with TFBs in the literature (Fig. 1.b), our devices exhibit the best performances. In addition, our TFBs show very good cycling behavior over 100 cycles, with an average capacity loss of 0.05% per cycle.
The fabrication process developed within this context is viable for industrial large-scale production and allows easy control and fine-tuning of the device electrochemical properties.

a.

b.

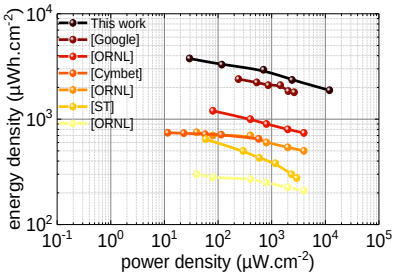
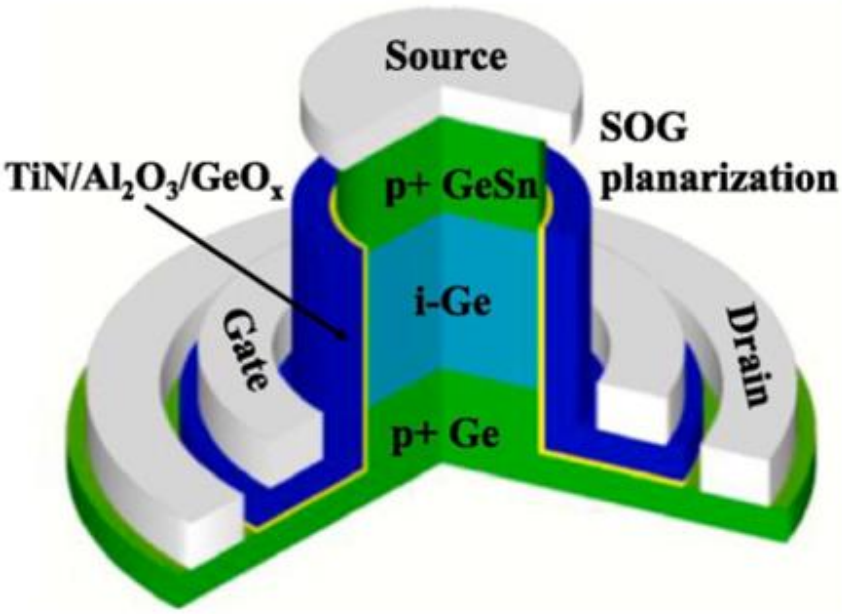
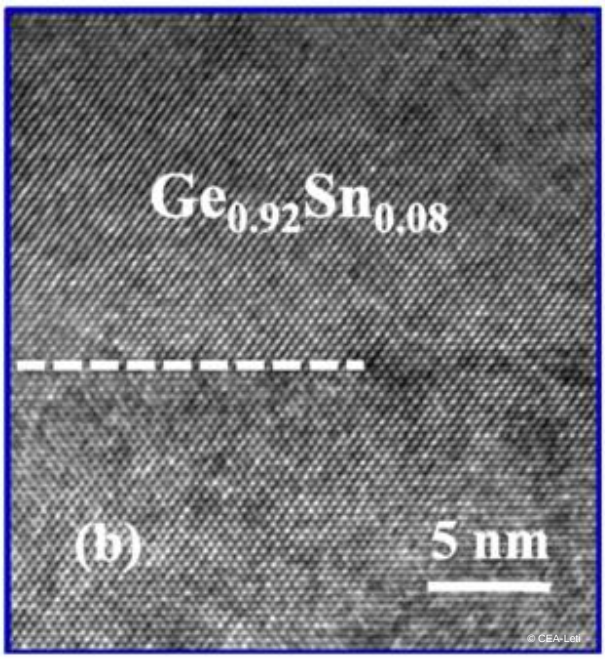


Figure 1: (a) photograph of a realized 3.1x1.7 mm^2 single device, (b) Ragone plot summarizing the study. To our knowledge, the developed TFBs exhibit the highest energy and power densities, in comparison to results from literature (Cymbet, ST, Google and ORNL)

Perspectives
The versatility of our TFB device architecture opens opportunities for further development such as stacking multiple devices, miniaturization, or exploring the implementation on ultrathin and flexible substrates.

RELATED PUBLICATIONS:
[1] S. Oukassi et al., 2019 IEDM, (2019), https://doi.org/10.1109/IEDM19573.2019.8993483.
[2] M. Lee, Nature Electronics, vol. 2, no 12, (2019), https://doi.org/10.1038/s41928-019-0346-7.


Source
SOG
planarization
TiN/Al2O3/GeOx
p+ GeSn
i-Ge
Gate
Drain
p+ Ge


Ge0.92Sn0.08
(b)
5 nm
© CEA-Leti

06 EMERGING MATERIALS & PROCESSES

- Epitaxy of GeSn for Field Effect Transistors
- Contact Technology on GeSn and III-V Semiconductors for Optoelectronics
- Nanosecond Laser Anneal for Nanoelectronics and Optoelectronics
- Unveiling of the Mechanism Behind Ovonic Threshold Switching in Chalcogenide Glasses Used as Selector Element for Ultimate 3D Non-Volatile Resistive Memories
- Selective Deposition Processing: A Toolbox for 3D Substrates

Epitaxy of GeSn for Field Effect Transistors

RESEARCH TOPIC:

Reduced Pressure Chemical Vapour Deposition of Ge/GeSn heterostructures, Field Effect Transistors and MOS capacitors.

AUTHORS:

J.M. Hartmann, J. Aubin (B. Salem, F. Bassani, T. Baron)[1], (Q.T. Zhao, D. Buca, D. Grutzmacher)[2]

Alloying Ge, an indirect bandgap semiconductor, with Sn, a semi-metal which also belongs to column IV of the periodic table, is very attractive for nanoelectronics and photonics. Compressive strain in pseudomorphic GeSn layers (grown on Ge) indeed yields higher hole mobility in p-type Metal Oxide Semiconductor Field Effect Transistors. Their reduced bandgap compared to bulk Ge results in lower operating voltages. CEA-Leti has explored, together with LTM, various surface preparations and interfacial layers to improve the electrical performance of high-K/metal gate pMOS capacitors on GeSn. CEA-Leti has also provided tailored-made Ge:B / Ge / $Ge_{0.92}Sn_{0.08}$ stacks on top of Ge strain relaxed buffers to FZJ for use as the core of vertical Nanowire pFETs.

SCIENTIFIC COLLABORATIONS: [1]LTM-CNRS, [2]Forschungs Zentrum Juelich (FZJ)

Context and Challenges

Alloying germanium, an indirect bandgap semiconductor (E_g = 0.74 eV), with Sn, a semimetal (E_g = 0 eV), is most interesting for a variety of reasons. Hole mobility is indeed higher in compressively-strained GeSn layers (grown on Ge) than in bulk Ge. Electron mobility is otherwise expected to be high when exceeding the Sn concentration above which GeSn becomes a direct bandgap semiconductor (~ 8% Sn without strain). CEA-CEA-Leti has acquired since 2016 a solid expertise on the low temperature epitaxy of complex Ge/GeSn stacks on 200 mm wafers. Such growth is far from trivial because of the huge lattice mismatch between Ge and Sn (5.66 Å <=> 6.49 Å) and Sn precipitation / surface segregation. This knowhow has been used to explore, together with LTM and FZJ, (i) various schemes to passivate GeSn surfaces prior to the deposition of high-K dielectrics and (ii) the interest of using Ge / GeSn stacks to fabricate vertical p-type Field Effect Transistors (pFETs).

Main Results

We have investigated with LTM the impact of different wet treatments on the electrical performances of $Ge_{0.9}Sn_{0.1}$ / Al_2O_3 / Ti / Au p-type Metal Oxide Semiconductor (MOS) capacitors. A high quality interface was obtained when the $Ge_{0.9}Sn_{0.1}$ surface was cleaned by HF then $(NH_4)_2S$. There was notably a lack of Sn or Ge diffusion into the Al_2O_3 layer. Capacitance−Voltage characteristics combined with a custom-analytical model yielded a low interface trap density (D_{it}) of 9×10^{11} cm^2 eV^{-1} s^{-1} (Fig. 1) [1]. The impact of interfacial layers on the electrical performances of $Ge_{0.9}Sn_{0.1}$ / HfO_2 / Ti / Au /Ti / HfO_2 p-MOS capacitors was also assessed. Plasma oxidized GeSn ($GeSnO_x$) interfacial layers yielded D_{it} as low as 5×10^{11} cm^2 eV^{-1} s^{-1} [2].

We have also provided tailored-made Ge:B / Ge / Ge or $Ge_{0.92}Sn_{0.08}$ stacks on top of Ge strain relaxed buffers to FZJ for use as the core of vertical NanoWire pFETs (Fig. 2). Ge NW pFETs exhibited a low Sub-threshold Slope of 66 mV/dec, a small Drain Induced Barrier Lowering of 35 mV/V and a high I_{ON}/I_{OFF} ratio of 3×10^6. Adopting $Ge_{0.92}Sn_{0.08}$ as the source yielded even better electrical performances, with notably a ~32% I_{ON} enhancement over Ge control devices [3-4].

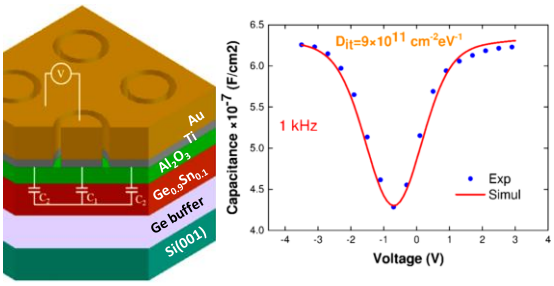


Figure 1: Stacks used to probe with C-V measurements, various GeSn passivation schemes prior to high-K deposition.

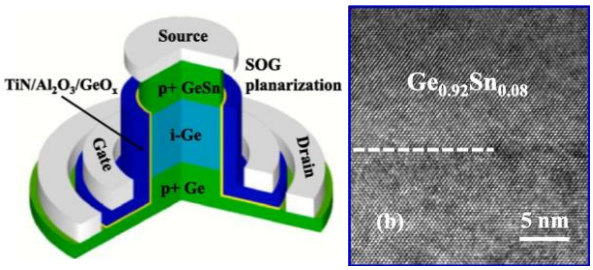


Figure 2: Schematics of the vertical pFET devices fabricated with Ge:B/Ge/GeSn stacks.

Perspectives

LTM is using the know-how acquired on MOS capacitors to fabricate GeSn stacked NW and Nano-Sheet devices, while FZJ is exploring Equivalent Oxide Thickness scaling as a mean to further boost the performances of their NW transistors. Both entities are taking advantage of the expertise CEA-Leti has acquired on the low temperature epitaxy of complex Ge/GeSn stacks.

RELATED PUBLICATIONS:

[1] M.A. Mahjoub et al., ACS Applied Electronics Materials 1, 260 (2019). https://doi.org/10.1021/acsaelm.8b00099.

[2] T. Haffner et al., Applied Physics Letters 115, 171601 (2019). https://doi.org/10.1063/1.5121474

[3] M. Liu et al., Solid State Electronics (2019). https://doi.org/10.1016/j.sse.2019.107716

Contact Technology on GeSn and III-V Semiconductors for Optoelectronics

RESEARCH TOPIC:
Metallization, Contacts, GeSn, InP, InGaAs, Ni alloys

AUTHORS:
A. Quintero, F. Boyer, P. Gergaud, J.M. Hartmann, V. Reboud, C. Jany, P. Rodriguez, (M. Grégoire)[1], (Q. Rafhay)[2], (E.Cassan)[3]

Ohmic contacts on semiconductors such as GeSn and III-V (n-InP and p-InGaAs, in particular) are mandatory for the fabrication of performant optoelectronics devices on 200 and 300 mm Si-platforms. CEA-Leti has thus developed an innovative contact technology fully compatible with a Si fabrication line. As far as GeSn layers are concerned, the impact of alloying elements such as Co, Pt on nickel stanogermanide formation was studied. A first reliability study of Ti / n-InP and Ti / p-InGaAs ohmic contacts for hybrid III-V / Si lasers was otherwise conducted and the Ni / n-InP system investigated using morphological, structural, and electrical characterizations.

SCIENTIFIC COLLABORATIONS: [1]STMicroelectronics, [2]IMEP-LAHC, [3]C2N/CNRS/Université Paris-Saclay

Context and Challenges
The integration of optoelectronics devices on 200 and 300 mm Si-platforms requires the development of dedicated CMOS-compatible contact technologies on new kind of materials such as GeSn and III-V semiconductors (InP, InGaAs). This involves physico-chemical and electrical characterisations of systems such as Ni / GeSn, Ti / InP, Ti / InGaAs and Ni / InP.

Main Results
The impact of Pt or Co as alloying elements for Ni-based metallization of GeSn layers was investigated. The overall phase sequence was the same for all types of metallization: at low temperature, a Ni-rich phase was obtained; it was then consumed to form the low resistivity mono-stanogermanide phase. Nevertheless, the addition of an alloying element had an impact on Ni consumption, Ni-rich and monostanogermanide phase formation temperatures (Fig. 1). Moreover, the addition of Co or Pt positively impacted Sn segregation by delaying it. Co had a weak influence on morphological and electrical properties. On the other hand, Pt improved the surface morphology by delaying the Ni(GeSn) phase agglomeration and enhancing the process window in which the sheet resistance remained low [1,2].

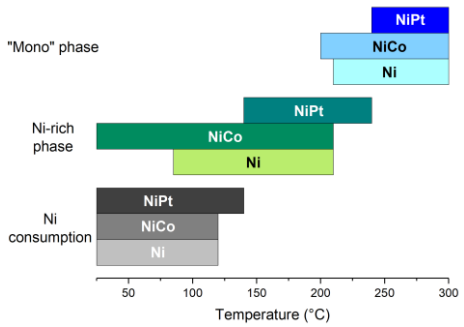


Figure 1: Impact of Co or Pt addition on Ni consumption, Ni-rich and monostanogermanide phases formation temperatures.

The impact of integration steps, BEOL and laser operations on Ti / n-InP and Ti / p-InGaAs contacts for III-V / Si hybrid lasers was studied for the first time [3]. Both systems exhibited a very good thermal stability.

The Ni / InP system with either He or Ar plasma preclean prior to Ni deposition was investigated [4]. We showed that the preclean used to remove the native oxides had a significant impact on the InP surface (Fig. 2). Indeed, Ar preclean resulted in a rough surface with a high concentration of In dots, while He preclean yielded a smoother surface with little or no In dots.

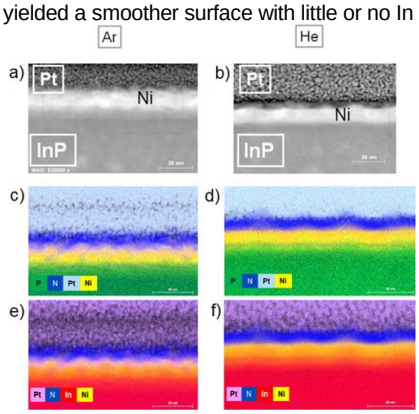


Figure 2: TEM images and EDX mapping of the TiN / Ni /InP as-deposited stacks with Ar and He preclean.

Electrical characteristics showed that Ar-precleaned contacts exhibited a non-ohmic behavior. This was due to the rough InP surface with some In accumulation. Meanwhile, He-precleaned contacts were ohmic from the as-deposited state up to 350 °C.

Perspectives
Studies conducted on GeSn and III-V semiconductors resulted in a fully fledged contact technology for optoelectronics applications. It will be used during the elaboration of silicon photonic devices.

RELATED PUBLICATIONS:
[1] A. Quintero et al., 19th International Workshop on Junction Technology (2019), https://doi.org/10.23919/IWJT.2019.8802618
[2] A. Quintero et al., ECS Trans. 93, 51-55 (2019), https://doi.org/10.1149/09301.0051ecst
[3] F. Boyer et al., IEEE 16th International Conference on Group IV Photonics (GFP-2019), https://doi.org/10.1109/GROUP4.2019.8926115
[4] F. Boyer et al., J. Vac. Sci. Technol., B 38, 012209 (2020), https://doi.org/10.1116/1.5128554

Nanosecond Laser Anneal for Nanoelectronics and Optoelectronics

RESEARCH TOPIC:

Thermal treatment, laser annealing, SiGe, dopant activation, plasmonics, 3D integration, crystallization, gate stack

AUTHORS:

S. Kerdilès, P. Acosta Alba, A.S. Royet, L. Dagault, L. Brunet, C. Fenouillet-Béranger (K. Huet, P.E. Raynal, T. Tabata, F. Mazzamuto)[1], (F. Cristiano)[2]

Thanks to its extremely short duration and high temperature capability, Ultraviolet Nanosecond Laser Annealing (UV-NLA) is a very promising approach to overcome process limitations and develop alternative schemes to achieve better device performance and enable 3D architectures. Its potential applications cover a wide spectrum, from dopant activation, contact formation to semiconductors or metals grains size engineering. CEA-Leti has explored, with its partners SCREEN and LAAS, the behavior of strained SiGe epilayers upon UV-NLA in view of advanced contacts, and dopant activation in Si nanoparticles (Si-NPs) embedded in a SiO_2 matrix for plasmonics. For 3D sequential integration, a low temperature gate stack has been implemented, taking advantage of UV-NLA.

SCIENTIFIC COLLABORATIONS: [1]SCREEN and its french subsidiary LASSE (Gennevilliers), [2]LAAS-CNRS (Toulouse)

Context and Challenges

Thermal treatments performed in classical furnaces, Rapid Thermal Processing or even millisecond systems face several technical limitations: dopant diffusion undesirable for shallow junctions, active dopant concentrations limited by the solid solubility, no local nor selective heating capability but global wafer treatment, which is not compatible with some of the steps required for 3D sequential integration. UV-NLA has a good chance of overcoming some of these technical barriers. Thanks to its high temperature capability and extremely fast ramps, UV-NLA offers the possibility of reaching unprecedented active dopant concentrations with little or no diffusion. Moreover, UV-NLA can be laterally limited by the laser scan itself and/or by optical masking. Finally, UV-NLA can be selective in depth thanks to the absorption of the UV radiation in the first nm and a very limited heat diffusion due to the short pulse duration. In 2019, CEA-Leti explored, together with its partners, the behavior of strained SiGe epilayers upon UV-NLA (for advanced contacts), and dopant activation in Si nanoparticles embedded in a SiO_2 matrix for plasmonics. For 3D sequential integration, a low temperature gate stack was otherwise implemented.

Main Results

UV-NLA was performed on 30 nm-thick $Si_{0.8}Ge_{0.2}$ epitaxial layers. The various regimes encountered, from sub-melt to partial and total melt, were identified. Energy densities ≥ 2.00 J/cm^2 led to the formation of pseudomorphic layers with a strong Ge redistribution (Fig. 1.a). Starting from uniform $Si_{0.8}Ge_{0.2}$ layers, Ge segregation toward the surface resulted in the formation of a Ge-rich surface layer with up to 55 at.% Ge [1]. Such strained SiGe layers with a graded composition and a Ge-rich surface may find promising applications such as contact resistance lowering for doped layers.

We also performed numerical simulations of UV-NLA on plasmonic structures based on Si-NPs embedded in a SiO_2 matrix [2]. It provided guidelines for the design of the structures, forecasts on the effect of the Si-NPs density and predicted quite accurately the UV-NLA process window observed experimentally later on.

For 3D sequential integration, a low temperature gate stack for the upper level was finally obtained by converting a phosphorus doped amorphous Si layer into poly-Si thanks to the depth selectivity of UV-NLA [3, 4]. By simulating the required conditions in advance, full recrystallization and low resistance of the poly-Si gate were obtained experimentally (Fig.1.b, 1.c) in the melt regime whilst preserving the underlying active region. The thermal budget is compatible with a high performance bottom level.

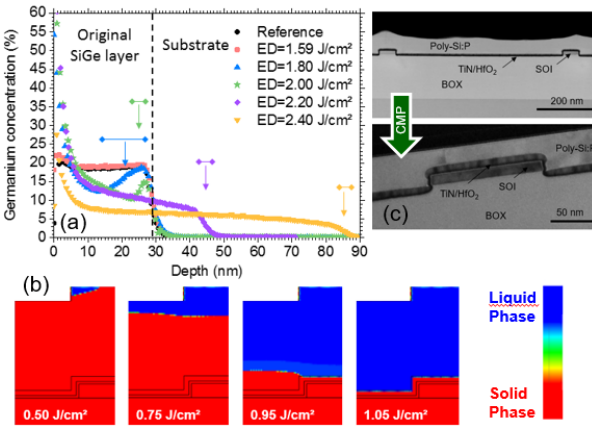


Figure 1: (a) Ge redistribution upon UV-NLA of $Si_{0.8}Ge_{0.2}$ epilayers [1]. (b) 2D simulations of the melting front in the gate stack submitted to UV-NLA. (c) TEM cross-section observations of the gate stack after UV-NLA and after CMP [3]

Perspectives

Dopant activation in laser annealed SiGe epilayers and in Si-NPs embedded in SiO_2 matrix for plasmonics will be further investigated. The electrical performance of the cold gate-stack proposed for our 3D integration will also be optimized.

RELATED PUBLICATIONS:

[1] L. Dagault et al., ECS J. Solid State Science & Technology, **8** (2019), https://doi.org/10.1149/2.0191903jss

[2] A.-S. Royet et al., Int. Conf. on Simulation of Semiconductor Processes and Devices,(SISPAD), 8870529 (2019), https://doi.org/10.1109/SISPAD.2019.8870529

[3] S. Kerdilès et al., ECS Transactions, **93** https://doi.org/10.1149/09301.0019ecst

[4] C. Fenouillet-Béranger et al., Electron Devices Technology & Manufacturing Conf.(EDTM), 8731192 (2019), https://doi.org/10.1109/EDTM.2019.8731192

Unveiling of the Mechanism Behind Ovonic Threshold Switching in Chalcogenide Glasses Used as Selector Element for Ultimate 3D Non-Volatile Resistive Memories

RESEARCH TOPIC:

Ovonic threshold switching, amorphous chalcogenides, advanced selector devices, ultimate 3D resistive memories.

AUTHORS:

P. Noé, A. Verdy, J.-B. Dory, G. Navarro, M. Bernard (J.Y. Raty)[1], (F. d'Acapito)[2], (J.B. Jager)[3], (J. Gaudin)[4]

Fifty years after its discovery, the origin of the OTS (Ovonic Threshold Switching) phenomenon has been revealed. By combining advanced electrical, optical and X-ray absorption spectroscopy measurements with an original *ab initio* calculation method, CEA-Leti's scientists were able to describe at the atomic level the processes involved in the OTS phenomenon and to propose design rules for these materials at the atomic-scale level. Under the application of an electric field, certain glasses of the chalcogenide family suddenly become metallic due to subtle rearrangements in the positions of the atoms. This OTS effect is at the basis of selector devices, which, associated with a resistive memory, results in new memories with a 3D architecture bridging the performance gap between fast volatile memories, such as DRAM, and the much slower non-volatile Flash memories.

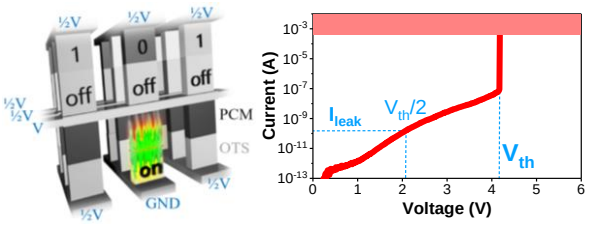
SCIENTIFIC COLLABORATIONS: [1]FRS-FNRS (Univ. Liège), [2]CNR-IOM-OGG C/O ESRF, [3]CEA DRF/IRIG, [4] CELIA (Univ. Bordeaux)

Context and Challenges

The unique phenomenon called OTS (Ovonic Threshold Switching) has recently led to a major technological breakthrough in the field of memories [1]. Indeed, it yielded high-density 3D non-volatile resistive memories thanks to the combination of a phase-change memory (PCM) element and an OTS selector, both based on chalcogenide materials (Fig. 1.a). This opens the way to storage class memories (SCM) and innovative brain-inspired neuromorphic circuits. However, fifty years after its discovery, the origin of the OTS effect, which is a unique non-linear conductivity behaviour observed in some chalcogenide glasses during the application of high electric fields (Fig. 1.b.), was still not explained nor fully understood.

Main Results

CEA-Leti has elucidated the mechanism of OTS switching by studying new state-of-the-art OTS materials based on GeSbSeN compounds using advanced electrical, optical and X-ray absorption spectroscopy (XAS) experiments as well as an innovative *ab initio* molecular dynamics (AIMD) simulation method [1, 2].



(a) (b)

Figure 1: (a) Memory cell obtained by stacking a PCM and an OTS selector in a cross-point memory element used in 3D memories. (b) I-V characteristics of an OTS thin film. When the applied V exceeds V_{th} the OTS material experiences a spectacular resistivity drop enabling high current flow. The latter enables to program and read the selected memory cell within the 3D cross-point network without undesired programming of adjacent cells by limiting the leakage current to the I_{leak} value with a $V_{th}/2$ polarization strategy. When the high voltage is removed, the OTS material recovers its highly resistive state.

While the subthreshold conduction mechanisms in chalcogenide glasses are now well understood, the underlying physical mechanism involved in OTS switching is still much debated. Recently, the OTS mechanism was shown to involve subtle atomic rearrangements upon high electric field application in OTS thin film glasses [1]. The latter led to the alignment of certain bonds and the appearance of local structural patterns reminiscent of the new metavalent bond (MVB) recently described in crystalline phase of chalcogenide-based phase-change materials [2]. Such MVB are responsible for a huge change in electronic Density of States (eDoS) accompanied by a drop in the electronic conductivity of the materials (Fig. 2). Such a fundamental understanding enabled CEA-Leti to draw design rules to further optimize the OTS properties of amorphous chalcogenides [3].

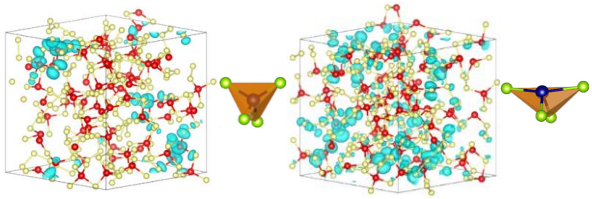


Figure 2: Snapshots of amorphous OTS glass in the (left) pristine and (right) excited state. The huge increase of conductivity upon electric field application observed at threshold switching in OTS materials can be explained by the strong delocalization of the electronic states around E_F wave functions (blue isocurves). Although the global topology of the network is kept upon excitation, important changes can be observed on the proportion of quasi-aligned bonds giving rise to structural arrangements reminiscent of metavalent bonds.

Perspectives

Our current OTS switching model establishes for the first time the common link between chalcogenide materials belonging to the phase-change materials (PCM) and those of the OTS family. In both systems, the MVB mechanism is responsible for the unique properties that led to the recent breakthrough in non-volatile memories. As shown here, the main difference between PCM and OTS materials lies in their ability to stabilize the MVB mechanism and in the energy barrier to crystallization.

RELATED PUBLICATIONS:

[1] P. Noé et al., Sci. Adv. 6, (2020). https://doi.org/10.1126/sciadv.aay2830

[2] J.Y. Raty et al., Phys. Status Solidi RRL, 1900581 (2019). https://doi.org/10.1002/pssr.201900581

[3] A. Verdy et al., Phys. Status Solidi RRL, 1900548 (2019). https://doi.org/10.1002/pssr.201900581

Selective Deposition Processing: A Toolbox for 3D Substrates

RESEARCH TOPIC:
Area Selective Deposition, Plasma Enhanced Atomic Layer Deposition, Plasma Etching

AUTHORS:
R. Gassilloud, N. Possémé (C. Vallée, M. Bonvallot)[1]

Area Selective Deposition (ASD) strategies are under study to reduce the manufacturing cost of nanometer scale devices, with advantages in reduced process complexity and improved pattern fidelity. CEA-Leti and LTM are exploring different approaches to grow self-aligned features on patterns at the ~10 nm length scale. A first bottom-up process is based on a modified plasma enhanced atomic layer deposition (PE-ALD) sequence with a chemical plasma etching step. The second relies on a physical plasma etching step, i.e, namely a sputtering step, inserted in an ALD conformal process, leading to the deposition of an oxide on the sidewalls of deep structures. These elegant and reliable processes expand the available toolbox for the growth of self-aligned materials at the nanometre scale.

SCIENTIFIC COLLABORATIONS: [1] Laboratoire des Technologies de la Microélectronique (CNRS-LTM)

Context and Challenges

The increased fabrication complexity of new devices made of various layers of nanoscale materials with 3D features has led to a need to add to the current portfolio of deposition and etching techniques novel selective processes. Area Selective deposition by ALD is a recent bottom-up approach firstly developed to overcome strong critical patterning issues, such as lithography edge placement errors and related expanding cost. In collaboration with CNRS-LTM, we have developed new selective processes using chemically or physically assisted alternatives. We recently evaluated a new selective process using in-situ reactive etching to deposit nanometre scaled oxides exclusively on surface walls in deep structures.

Main Results

As illustrated in Figure 1, a selective deposition process results in the growth of a thin film on one type of surface (for instance an oxide) without any growth on another (such as a metal).

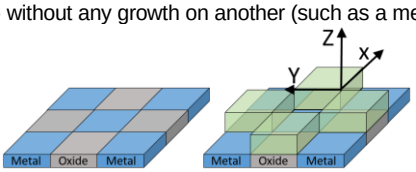


Figure 1: Principle of an area selective deposition process.

Our first approach in Figure 2.a. takes full advantage of the inherent nucleation delay commonly observed in chemical deposition processes. R. Vallat *et al* showed on 300 mm silicon substrates that, by adding and finely tuning a chemical plasma etching step in ALD cycles, it was possible to enhance the growth of TiO_2 on one type of region (here, a TiN metallic surface) with respect to another (a silicon-based surface, i.e. Si, SiO_2 or SiN). Indeed, both regions have different chemical surface compositions [1]. The second selective deposition approach exploits anisotropic energetic ions from the plasma to locally sputter matter away. The process is based on the alternate use of plasma enhanced atomic layer deposition (PEALD) and sputtering steps within a PEALD reactor equipped with a radio-frequency substrate biasing kit. The sidewall deposition illustrated in Figure 2.b. can be obtained without modifying the nature of the deposited film. A proof of concept for the topographically selective deposition of Ta_2O_5 in 3D Si features was achieved by A. Chaker *et al* [2], with the insertion of several argon plasma sputtering steps under biasing assistance in standard Ta_2O_5 PEALD cycles.

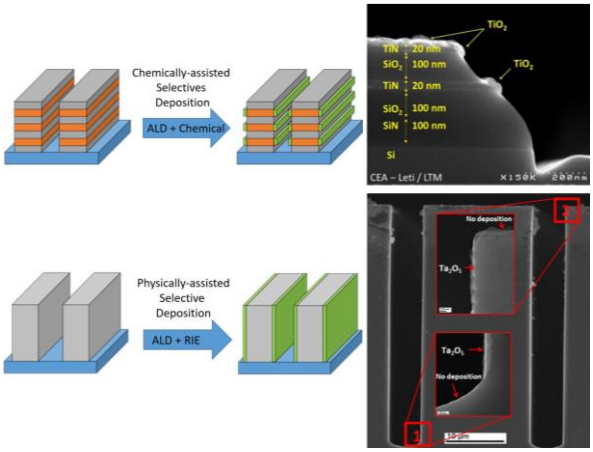
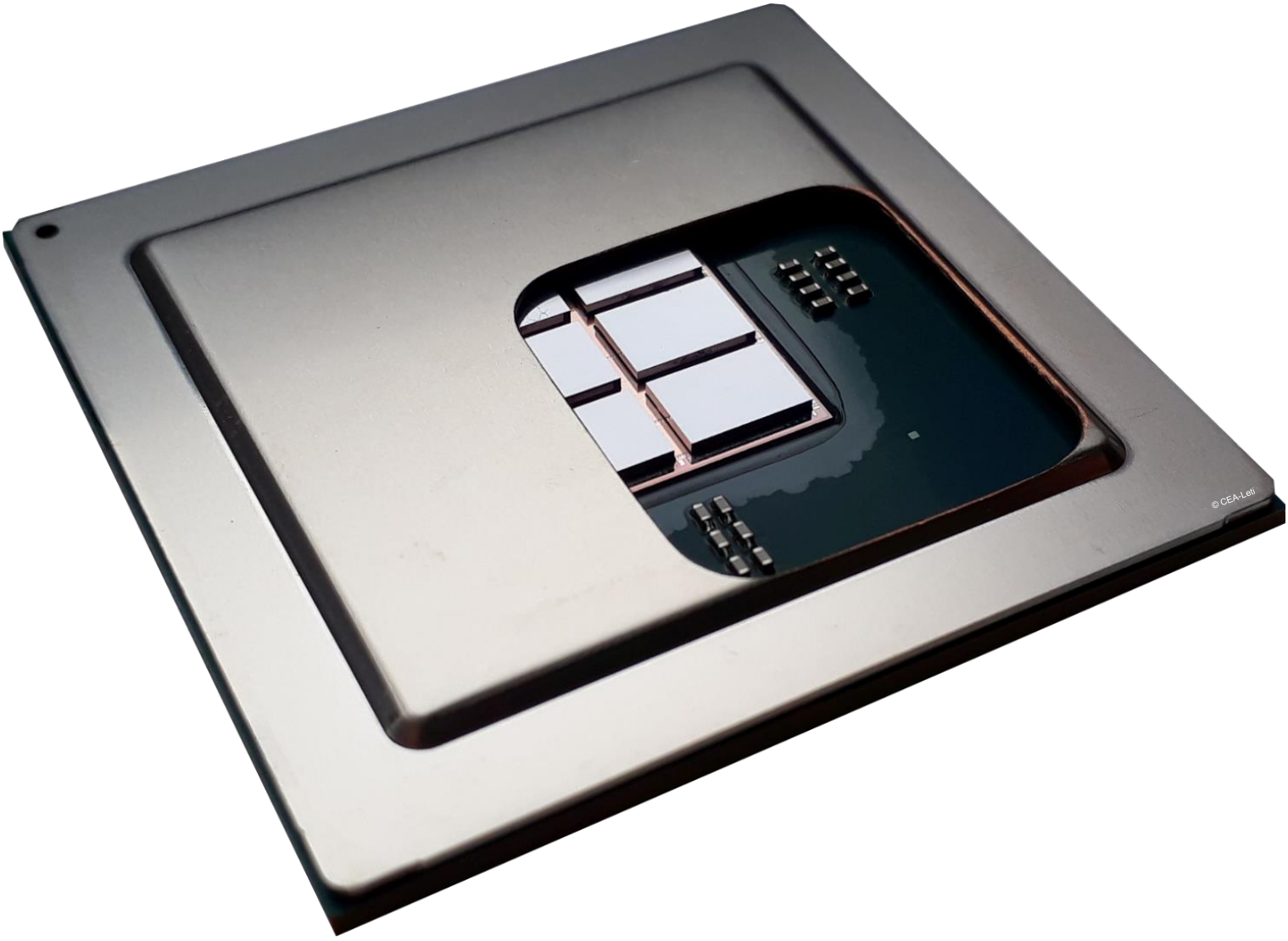


Figure 2: (a) Selective chemically-assisted deposition solution of TiO_2 on metallic TiN surfaces, (b) Illustration of a physically-assisted process leading to side walls deposition in deep structures by combining super cycles of PEALD + anisotropic etching.

Perspectives

This collaborative activity started in 2015 is still going on in the framework of a PhD dissertation to develop innovative elegant ASD solutions, including smart plasma densifications and self-assembled monolayers (SAMs) approaches

RELATED PUBLICATIONS:
[1] R. Vallat et al., Journal of Vacuum Science & Technology A, (2019), https://doi.org/10.1116/1.5049361
[2] A. Chaker et al., Applied Physics Letters, (2019), https://doi.org/10.1063/1.5065801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07 INTEGRATION & PACKAGING

- ChipInFlex
- 3D Integration: How to Make Die-to-Wafer Direct Hybrid Bonding an Industrial Reality?
- Technologies for Chiplet-Based 3D System Architectures – From Passive to Active and Photonic Interposers
- Die to Wafer Direct Bonding as a Key Enabler in 3D Integration for Photonics

ChipInFlex

RESEARCH TOPIC:
Flexible electronics, packaging, flip-chip, thin silicon die

AUTHORS:
J-C Souriau, L. Castagné, A. Itawi, C. Ladner

New developments in the integration of ultra-thin silicon dies within a flexible film lead to a new paradigm. Indeed, thanks to the thinness and flexibility of devices, it is conceivable that functions can be added around any object without changing its aspect. A new technology called ChipInFlex proposes the integration of ultra-thin silicon dies within a flexible label made on a wafer carrier in the manufacturing microelectronic line. This study is the first step towards a full electronic system in a flexible label.

SCIENTIFIC COLLABORATIONS: CNRS Renatech network

Context and Challenges

Currently, only electronic tracks between components are flexible in major flexible electronic products. This is due to the fact that the silicon components are already packaged or are too thick. In order to get fully flexible devices, silicon dies have to be thinned to less than 50 µm. Three formats can be processed to build flexible electronic systems: ribbon, panel or wafer. The first two are well adapted for large devices, are low cost and allow high throughput. However, patterning resolution in these formats is only medium. It was chosen in our study to work at the wafer level in a microelectronic manufacturing line because this achieves a high resolution of integration.

Main Results

The choice of the flexible material in which to integrate silicon dies is critical. In the this study, we tested the commercialized photosensitive siloxane polymer SiNR, which is available in spin-on or dry film and has low-cure temperature. The manufacturing process experiment is detailed in Figure 1. Dies were flip-chip bonded on the wafer and collective thinned to reduce the die thickness to 40 µm. An additional SINR layer was laminated under vacuum to encapsulate.

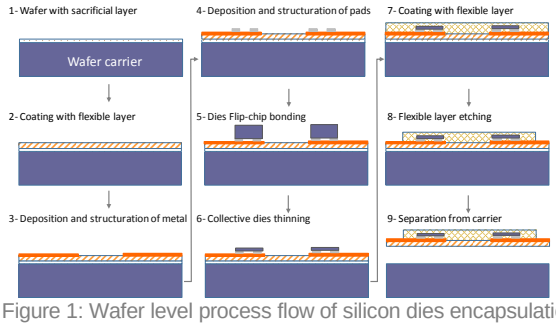


Figure 1: Wafer level process flow of silicon dies encapsulation

Flexible labels were diced using a laser and peeled from the wafer carrier (Fig. 2). One challenge is to offer a process compatible with bare dies. It was chosen for the electrical interconnection gold stud bumps because it enables the hybridization by thermo-compression at low temperature (<150°C) and it is compatible with polymer.

Technological elementary bricks to manufacture the flexible label have been assessed and the process was validated on an electrical test vehicle with success. A test vehicle being designed to optimized the process. The 200 mm wafer included 24 labels (30x25mm²) and each one could receive two dies. One is 5x5mm² size and the second is 10x10mm² size. The electrical continuity of silicon chips within the label was tested thanks to specific test patterns (Kelvin and daisychain). Electrical tests were performed during the manufacturing process after the main steps: flip-chip bonding, backside thinning, final encapsulation and peeling from wafer carrier.

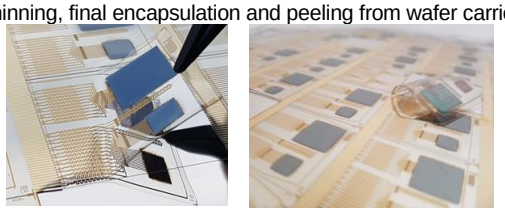


Figure 2: Label including silicon dies flip-chip bonded and thinned down to 40µm

Several wafers were fully populated and electrically characterized. Two wafers included a bottom SINR layer 80µm thick and one wafer included a bottom SINR layer 30µm thick. The resistance of a single contact between dies and label was found between 8 to 15 mOhm according to the thickness of the SINR underneath. The percentages of valid daisy chains were over 75%.

Perspectives

This study is the first step towards a full electronic system in a flexible label. A demonstrator is currently under development with applications ranging from strain sensors to radio frequency identification (RFID) dies.

RELATED PUBLICATIONS:
1] J.-C. Souriau et al., 69th Electronic Components and Technology Conference (ECTC),(2019), https://doi.org/10.1109/ECTC.2019.00242
[2] J-C. Souriau et al. ChipScaleReview, 23, 5, (2019), http://fbs.advantageinc.com/chipscale/sep-oct_2019/files/assets/basic-html/page-10.html#

3D Integration: How to Make Die-to-Wafer Direct Hybrid Bonding an Industrial Reality?

RESEARCH TOPIC:

3D Integration, Direct hybrid bonding, Die-to-Wafer stacking, High density Interconnection.

AUTHORS:

A. Jouve, E. Bourjot, N. Bresson, P. Stewart, E. Rolland, V. Balan, F., L. Sanchez, C. Castan, Y. Exbraya, F. Servant, S. Cheramy, (P. Metzger)[1].

Die-To-Wafer (D2W) direct hybrid bonding is foreseen as a major breakthrough for the future of 3D components since it offers the ability to assemble heterogeneous Known-Good Dies (KGD) dies with small interconnection pitches. However, its industrialization poses some additional challenges compared to Wafer-To-Wafer processing which is in production since the early 2010's, especially in term of throughput and die handling strategies. The CEA-Leti was a pioneer in demonstrating the feasibility of such techniques and an important ramp up has been made since 2017 to develop High Volume Manufacturing Integration flows and equipment to brings this technology to industry as fast as possible.

SCIENTIFIC COLLABORATIONS: [1]SET

Context and Challenges

Die-To-Wafer hybrid bonding process, using copper/TEOS interfaces is foreseen by major microelectronic industrials as essential for the success of future memory stacks, HPC or photonic devices, due to the heterogeneous integration and known good die selection capability. However, compared to Wafer-To-Wafer bonding, the Die-To-Wafer process flow is more complex and new challenges arise in enabling a transfer to mass production units. To overcome these challenges, CEA-Leti has recently developed a complete foundry-compatible solution to improve bonding yield of D2W hybrid bonding until the assessment of the connection electrical performances thanks to a dedicated electrical test vehicle. Furthermore, CEA-Leti is not only considering the stacking process, but studies are aimed at ensuring a complete D2W line including a direct bonding specific Known-Good Die (KGD) and post bonding contact recovery strategies. Finally, CEA-Leti is also exploring the potential of breakthrough processes, as D2W assisted by self-assembly phenomenon, which could improve alignment and throughput performances in the future.

Main Results

The first part of our work focused on standard D2W bonding improvement. The priority was to find die preparation strategies as well as fully automated systems with particle-free environment. First of all, defect-free bonding interfaces have been observed, demonstrating the relevance of the surface preparation protocol (Fig. 1). Then a complete 300 mm electrical test vehicle with optimized hybrid bonding levels has been processed and successfully stacked. Electrical measurements shown that the Die to Wafer contact resistance could be neglected, even for Daisy-chains as long as 20900 connections. Thermal cycling results were very encouraging since no deviation of the contact resistance was observed [1].

To complete this work and develop a complete D2W process line, two additional modules are being developed at CEA-Leti: Known-Good Die selection and post stacking die planarization. An approach of KGD was demonstrated to be compatible with hybrid bonding where the dies are tested at the HB level. In our flow, the topography made by the test tips (>1µm) can be successfully flattened with an optimized CMP step. The planarization of stacked dies in a mineral encapsulation was achieved with a 90 nm residual topography, which reveals the potential of multi-die stacking with D2W hybrid bonding [2].

Finally, significant technical improvements of the self-assembly process has been made (water confinement control, new spin-coatable hydrophobic material, process automation) leading to a 63% of oxide dies perfectly bonded with an alignment lower than 1µm (Fig. 2) [3].

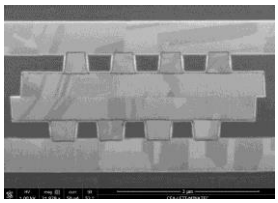


Figure 1: Perfect bonding interface obtained with standard D2W (10 µm pitch connection).

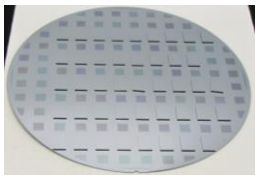


Figure 2: More than 40 dies stacked on 200 mm wafer with self-assembly process.

Perspectives

We continue to investigate the manufacturing potential of standard D2W hybrid bonding by challenging the throughput with a target of 1000 dies per hour. We also assess the bonding quality of even more complex electrical test vehicles.

New KGD process flows are being tested to match the variety of functional wafers to be stacked and prober capacities.

Self-assembly process stabilization will be pursued. Alignment performances will be improved below 500 nm and we aim to develop an automated system dedicated to this process to evaluated the throughput potential.

RELATED PUBLICATIONS:

[1] A.Jouve et al., Proceedings of 3DIC, 2019, https://ieeexplore.ieee.org/xpl/conhome/9043388/proceeding

[2] E.Bourjot et al., Proceedings of 3DIC, 2019, https://ieeexplore.ieee.org/xpl/conhome/9043388/proceeding

[3] A.Jouve et al., 69th Electronic Components and Technology Conference (ECTC), 2019, https://ieeexplore.ieee.org/document/8811276

Technologies for Chiplet-Based 3D System Architectures – From Passive to Active and Photonic Interposers

RESEARCH TOPIC:

3D integration, 3D interconnects, interposer, chiplet, through silicon via (TSV),

AUTHORS:

P. Coudrain, J. Charbonnier, A. Garnier, P. Tissier, R. Vélard, M. Assous, D. Saint-Patrice, R. Franiatte, F. Ponthenier, P. Vivet, D. Dutoit, D. Lattard, Y. Thonnart, (A. Farcy)[1], (Y. Beilliard)[2]

Large multi-core 3D systems with multiple chiplets integrated on an active silicon interposer have been proposed to support High Performance Computing (HPC) applications. Using fine-pitch 3D interconnects, chip-to-chip bandwidth is increased and the overall power consumption reduced. A chiplet approach allows optimization of industrial yield through smaller dies and reusable IP blocks. An active interposer allows intelligent features to be added to the final 3D system, such as advanced network-on-chip (NoC) interconnects, fast I/Os for off-chip communication, embedded power management and system-on-chip (SoC) infrastructure. This program addresses integration, packaging and test of chiplets on active silicon interposer with state-of-the-art 3D interconnects as well as ultra wide interconnects arrays for particle detection.

SCIENTIFIC COLLABORATIONS: [1]STM, [2]Université de Sherbrooke (Canada), CERN.

Context and Challenges

Breaking with the System-on-Chip paradigm, future systems will consist in smaller, less expensive and independently designed components called chiplets, connected by high bandwidth interconnections over silicon interposers. Benefits of stacking chiplets on an active interposer have been proposed for achieving large and scalable many-core systems for high performance computing.

Main Results

The INTACT prototype, embedding 96 cores within six chiplets, was developed (Fig. 1). We have detailed the full fabrication technology to be able to turn this concept into reality: 3D interconnects process including TSV and ultra-fine picth µ-pillars and the 3D packaging flow [1]. Special attention was paid to TSV process and defectivity performance, as well as the realization of 20 µm pitch µ-pillars for successful ultra dense 3D stacking and large dice [2]. The entire technology was successfully assessed morphologically (Fig. 2) and electrically with specific 3D test structures. Finally, the structural test of the INTACT prototype was reached and has shown results above expectations. The full extraction of the system performance associated to the architecture details will be published shortly. These results pave the way to the design of future high efficiency systems for high performance computing.

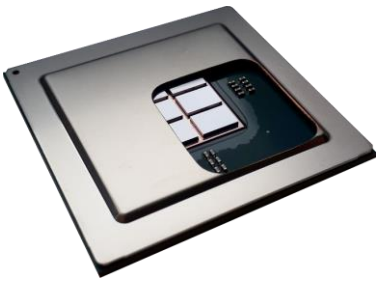


Figure 1: INTACT prototype with 6 chiplets on active Interposer

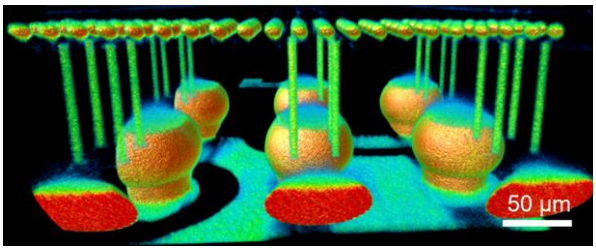


Figure 2: X-Ray tomography revealing internal 3D interconnects structure: C4 bumps, TSV and 20 µm pitch µ-connections

Perspectives

Chiplet integration with active interposer was also achieved on a second prototype, including the INTACT interposer with two chiplets and an additional FPGA on the BGA, in the frame of the Exanode European project. To meet the future needs of HPC, the chiplet-based system roadmap finally includes photonic interposers, capable of supporting a larger bandwidth between the chips. Among the work carried out in this program, the establishment of design rules allowing ultra-dense design of TSVs with photonic elements is a major objective (Fig. 3).

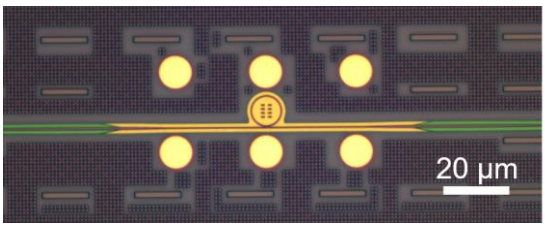


Figure 3: TSV Integration on photonic interposer for the future HPC roadmap (example of optical ring modulator surrounded by TSVs).

RELATED PUBLICATIONS:

[1] P. Coudrain et al., IEEE 69th Electronic Components and Technology Conference (ECTC), (2019), https://doi.org/10.1109/ECTC.2019.00092

[2] J. Charbonnier et al, IEEE 69th Electronic Components and Technology Conference (ECTC), (2019), https://doi.org/10.1109/ECTC.2019.00249

Die to Wafer Direct Bonding as a Key Enabler in 3D Integration for Photonics

RESEARCH TOPIC:

High quality III-V epitaxial growth on silicon using III-V bonded layer for photonic 3D Integration

AUTHORS:

F. Fournel, C. Dupré, L. Sanchez, C. Jany, V. Muffato, (C. Besancon, N. Vaissiere, J-P Le Goec, J. Decobert)[1], (S. David, F. Bassani, T. Baron)[2]

Since a few years now, CEA-Leti has developed a die to wafer process based on direct bonding technology. Using collective die handling, cleaning and bonding, III/V coupons can be transferred on 200 mm or 300 mm silicon based wafers. This permits the development of interesting photonic circuits merging the best from the III-V components and the silicon photonic platform. Recently a new step has been successfully achieved: III-V epitaxial regrowth on a silicon substrate using a high quality III/V seed layer. Instead of transferring the full III-V photonic devices, the latter could be directly grown after the bonding process on the silicon platform. It allows all the classical III-V epitaxial toolbox to be used, including several regrowth steps after the bonding process, directly on the silicon platform. In order to test this approach, an eight period strain compensated AlGaInAs MultiQuantum Well (MQW) heterostructure surrounded by two InP cladding layers was grown by MOVPE on an InP-SiO2/Si (InPoSi) substrate.

SCIENTIFIC COLLABORATIONS: [1]III-V Lab, [2]CNRS-LTM

Context and Challenges

The explosive increase in datacenter traffic challenges the current manufacturing of InP-based Photonic Integrated Circuits (PICs). III-V integration on silicon would enable low-cost large-scale fabrication of PICs. The direct growth of III-V materials on 300 mm Si wafers is the most promising approach to reduce the costs. However, the differences between III-V and Si in terms of lattice mismatch (8% for InP, 4% for GaAs) and thermal expansion coefficients are challenging issues to overcome. Hybrid silicon technology using a bonding process has the capacity to integrate III-V materials onto SOI (Silicon-On-Insulator) wafer with optimal III-V material quality without growth after the bonding. This is a huge limitation to extend all the III-V mature know-how. Transferring regrowth techniques to the hybrid silicon platform is of practical significance in improving individual devices.

Main Results

Using the CEA-Leti die to wafer process [1] which could be used also for the bonding of a small wafer onto a 200 or 300 mm silicon wafer, III/V components can be transferred on silicon photonic wafers. Recently, in order to study the possibility of III/V direct growth on silicon, an InP seed layer has been successfully transferred on silicon (InPoSi). After having understood the origin of some defect appearance during the epitaxial annealing temperature [2], a III/V heterostructure composed of 8 periods of strain-compensated AlGaInAs-based Multiple Quantum Wells (MQW) surrounded by two 120 nm-thick InP layers was grown by MOVPE simultaneously on InPoSi and on InP substrates. Not only is a smooth regrowth interface noticeable but also planar growth of MQW with sharp interfaces as shown on Figure 1 [3]. Besides other characterizations such as in-situ curvature and reflectance measurements and AFM growth surface quality observations showing a high regrowth quality, the X-ray diffraction and the photoluminescence comparison between the InPoSi or the bulk InP based wafer shows that there is no penalty in terms of crystal quality for the growth on InPoSi as shown on Figure 2.

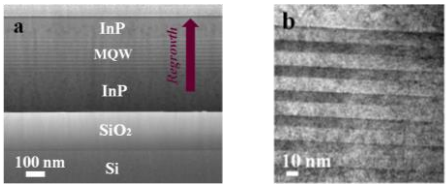


Figure 1. Cross-sectional images done on InPoSi: (a) STEM; (b) TEM cross-sectional images

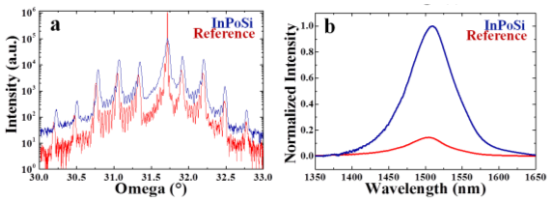


Figure 2. Characterizations done on InPoSi (blue) and on the reference (red): (a) High-Resolution X-ray Diffraction profiles; (b) Photoluminescence signals at room temperature

Perspectives

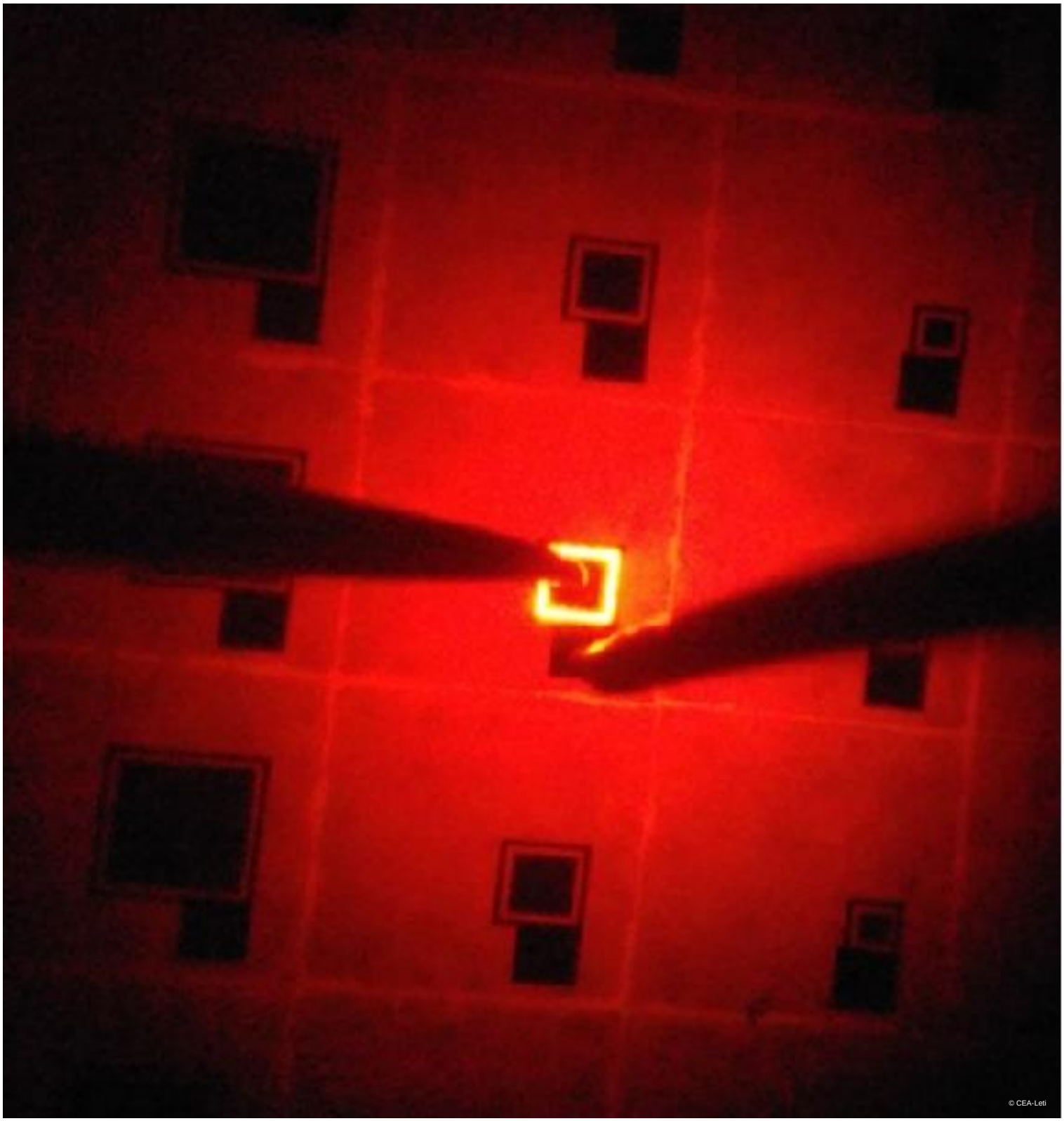
Altogether, these results demonstrate the excellent material quality obtained in regrown III/V heterostructures on InPoSi substrates, proving that this novel and versatile epitaxy technique is suitable for the development of hybrid III/V on Si optoelectronic devices. The next step will be to build lasers directly on this new substrate to show how powerful this approach could be. Indeed the transfer of standard prebonding epitaxial devices are already very interesting (laser source, MEA, amplifier, MZ or photodetector), but the possibility to perform epitaxy on a bonded seed layer could allow SAG or other classical growth approaches (BJ, SiBH, BRS) so that III/V devices could be precisely integrated with silicon photonic devices and ensure efficient light transport.

RELATED PUBLICATIONS:

[1] A.Jouve et al., Proceedings of 3DIC, 2019., https://ieeexplore.ieee.org/xpl/conhome/9043388/proceeding

[2] E.Bourjot et al., Proceedings of 3DIC, 2019., https://ieeexplore.ieee.org/xpl/conhome/9043388/proceeding

[3] A.Jouve et al., 69th Electronic Components and Technology Conference (ECTC), 2019, DOI: 10.1109/ECTC.2019.00041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08 MATERIALS & TECHNOLOGY FOR PHOTONICS

- Development of Sub-10µm Pitch HgCdTe Infrared Detectors
- High Internal Quantum Efficiency in InGaN Based Quantum Wells Emitting in the Red Range
- Hybrid MBE/MOVPE Tunnel Junctions for UV LEDs
- Nano-Pendeo Epitaxy of Nitride Compounds on Patterned SOI Substrates

Development of Sub-10µm Pitch HgCdTe Infrared Detectors

RESEARCH TOPIC:
Photonics, Infra-Red materials, bulk crystal growth and epilayers, II-VI technology

AUTHORS:
J.L. Santailler, J. Abergel, S. Bisotto, L.Mangin, (G.Guibaudo)[1]

A reduction of the pitch of MCT (Mercury Cadmium Tellurium) Focal Plane Arrays is required by our partner" customer needs and by market evolution. Many developments in the full technological elaboration and characterization chains were a pre-requisite to obtain infrared arrays with a pitch below 10 µm (VGA format 640*512, pitch 7.5 µm). First developments targeted middle wavelength devices (in the 3-5 µm range). Conducted between 2016 and 2019 this project managed by the Optronics' Division, was mainly transverse and benefited from technological contributions from many other teams from the Design and Technological Platform Divisions (respectively DACLE and DPFT). Improvement of CZT (Cadmium Zinc Tellurium) substrate preparation and thin MCT epilayer growth in the range of 10 µm were the main objectives of DPFT's material team.

SCIENTIFIC COLLABORATIONS: 1IMEP LAHC, LYNRED

Context and Challenges

At the beginning of the project, our partner production was mainly based on 15 µm pitch detection circuits with a classical VGA format (640x512). Improvements of Infra-Red detector performances enabled devices to work at rising temperature from 90K to 110K and up to 130K. These performances had benefits in terms of reduced cooling power and increased lifetimes and yielded Size Weight and Power (SWaP) improvements. A pitch reduction was demonstrated at 10 µm for a 1024x768 format in 2014. We started in 2016 to decrease the pitch value down to 7.5 and 5 µm by addressing the main issues of technologies available at that time.

Figure 1: Nanotec polishing set-up for CZT wafers up to 4 inches diameter.

Main Results

The detection circuit is built onto CZT substrates. In order to improve parallelism and flatness, we adopted a new approach based on specific polishing processes without any sample sticking (Fig. 1). Real improvements were achieved in term of CZT distortions, decreasing from 15 µm down to < 5µm (from 1.5 to 4 inches diameter). Samples prepared during the same batch had a more homogenous shape. Then, a liquid phase epitaxy process was used in order to get thin MCT layers (X_{Cd}=0,3) in the 10 µm range or less. Basic parameters like solution saturation, growth temperature and growth velocity were adapted to our partner's specifications. Two batches were successfully produced and delivered for subsequent technological processes.

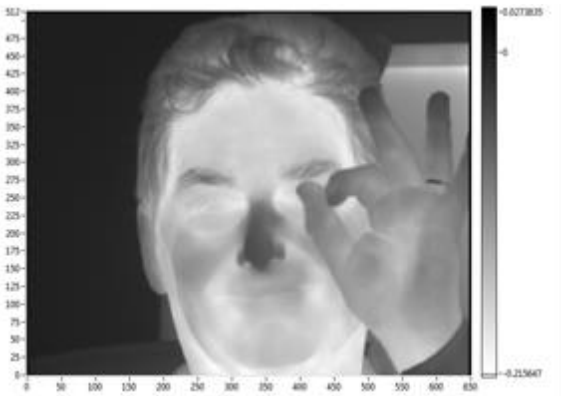


Figure 2: Picture in the MWIR band obtained with a VGA camera 640x512 VGA camera with a 7.5 µm pitch.

As a result, after extensive works on detection circuit, hybridization and ROIC, characterization teams succeeded in obtaining the first 7.5 µm pitch pictures with a CEA-Leti demonstrator camera [1-2] (Cf. Figure 2).

Perspectives

The next generation of 2k² arrays based on MCT technology with 7.5 µm pitch is now launched (starting early 2020). These new material bricks are currently used in all running infrared projects.

RELATED PUBLICATIONS:

[1] J. Abergel et al, Proceedings of SPIE, the International Society for Optical Engineering, Vol. 11002, N° 1100222 (2019), https://doi.org/10.1117/12.2520030

[2] S. Bisotto et al, Proceedings of SPIE, the International Society for Optical Engineering, Vol. 11002, N° 110021C (2019) https://doi.org/10.1117/12.2519330

[3] L. Mangin et al, Journal of Electronic Materials, Vol. 48, 6084–6092 (2019), https://doi.org/10.1007/s11664-019-07253-z

High Internal Quantum Efficiency in InGaN Based Quantum Wells Emitting in the Red Range

RESEARCH TOPIC:

Full native color micro-displays for augmented and virtual reality (AR/VR) applications

AUTHORS:

A. Dussaigne, F. Barbier, B. Samuel, R. Templier, F. Lévy, (O. Ledoux, M. Rozhavskaia, D. Sotta)[1], (S. Chenot, B. Damilano)[2]

A full InGaN structure is developed to demonstrate an efficient red emission with the InGaN alloy. The advantage of this new structure is to enhance the In incorporation rate in the quantum wells, by comparison to the conventional structure on GaN. The InGaNOS substrate fabricated by Soitec is used, as it is a relaxed InGaN pseudo-substrate. An InGaN/GaN superlattice buffer is overgrown on InGaNOS to get a better material quality and a surface free of V shaped defects. InGaN/InGaN multiple quantum wells are grown on top of this buffer. A red emission with a central emission wavelength of 624 nm and a linewidth of 58 nm is obtained. An internal quantum efficiency of 6.5% at 624 nm is measured, which is, to our knowledge, at the state of the art in the case of planar InGaN based light emitting diodes.

SCIENTIFIC COLLABORATIONS: [1]SOITEC, [2]CNRS-CRHEA

Context and Challenges

Micro-displays for virtual and augmented reality (AR/VR) is a new emerging application for inorganic light emitting diodes (LEDs). While for large multi-color displays, the pick and place technique can be used to merge different types of material families (nitrides for blue and green, and phosphide for red emission), it is no longer possible for AR/VR as the pixel size has to be reduced below 10x10 µm². The three primary colors should then be achieved with the same material family, and in a monolithic approach. $In_xGa_{1-x}N$ alloy seems to be the best candidate as it can theoretically cover the whole visible range by tuning its InN mole fraction x. However, for x higher than 25%, strong material degradation is observed when grown on a conventional structure (GaN on sapphire). To overcome this, the strain has to be reduced in the multiple quantum wells (MQWs). Our solution is to use a *full InGaN structure*: a full InGaN LED structure grown on a relaxed InGaN pseudo-substrate.

Main Results

To grow this full InGaN structure, the InGaNOS substrate fabricated by Soitec was employed, as it is a partially relaxed InGaN pseudo-substrate. A full InGaN LED structure has been then overgrown on this substrate which provides an *a* lattice parameter of 3.205Å, compared to 3.184Å for the conventional structure on GaN.

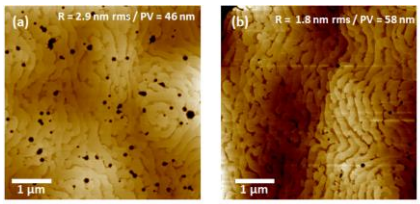


Figure 1: Atomic force microscopy images (5x5 µm² scan) of an InGaN buffer layer grown on InGaNOS (a) without superlattice, (b) with InGaN/GaN superlattice.

The LED structure is composed of an InGaN/GaN superlattice buffer, 5x InGaN/InGaN MQWs, and a 125 nm thick p doped InGaN layer. Red electroluminescence was previously demonstrated [1], and the growth optimizations continued to increase the efficiency. A particular InGaN/GaN superlattice was introduced to cover the V shaped defects (V pits) native from the substrate (Fig. 1) [2]. A reduction of the V pit density by one decade was observed. The material quality was also improved with a strong reduction of the X-ray diffraction rocking curve linewidth (from 3000 arcsec to 780 arcsec). Red emitting InGaN/InGaN MQWs were grown on this buffer. The InN mole fraction expected in the wells is 40%. Fig. 2 exhibits the photoluminescence (PL) spectra as a function of the temperature. At 290K, the central emission wavelength is 624 nm with a linewidth of 58 nm. The internal quantum efficiency, obtained by plotting the PL efficiency as a function of the excitation power at 15K and 290K, is 6.5% at 624 nm [2]. This value is, to our knowledge, at the state of the art for planar InGaN based LEDs.

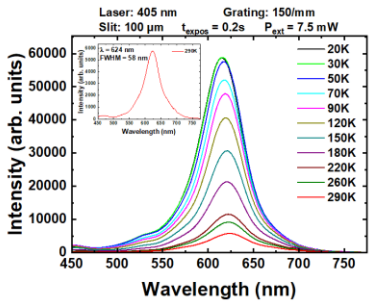


Figure 2: PL spectra as a function of the temperature for red emitting InGaN/InGaN MQWs. Inset: PL spectrum at 290K.

Perspectives

Optimizations of the full InGaN structure are ongoing. In particular, the p-InGaN layer is studied to improve the injection efficiency, and to obtain a better external quantum efficiency in the red range.

RELATED PUBLICATIONS:

[1] E. Guiot, A. Dussaigne et al., International Conference on Compound Semiconductor Manufacturing (CS MANTECH) (2019), https://s3.amazonaws.com/kc-assets/GMI62266/2019_CSMANTECH.zip - article 18.16

[2] A. Dussaigne et al., J. Cryst. Growth, (2020), 10.1016/j.jcrysgro.2020.125481

Hybrid MBE/MOVPE Tunnel Junctions for UV LEDs

RESEARCH TOPIC:
UV Light Emitting Diodes

AUTHORS:
V. Fan Arcara and G. Feuillet (J.Y. Duboz, B. Damilano) [1]

The use of tunnel junctions (TJs) above UV- light-emitting diodes (LEDs) is a potential solution to poor p type contacts as they replaced by n type contacts. Indeed, as the wavelength decreases towards the UV-C range, AlGaN based UV LEDs are plagued by low injection efficiencies, principally because of the low p-type doping achievable in high Al concentration AlGaN alloys. To implement such an idea, we have developed a hybrid MBE / MOVPE approach whereby the top n++ AlGaN layer is grown by MBE on top of the MOVPE grown UV emitting quantum well heterostructures. This combination prevents the re-passivation of Mg acceptors by hydrogen. For Ge doped AlGaN based TJs, the optical power of the UV LED (304 nm) was improved by at least a factor of 3, which was likely due to an enhancement of the hole injection efficiency.

SCIENTIFIC COLLABORATIONS: [1]CNRS-CRHEA

Context and Challenges

Ultraviolet (UV) sources other than Hg lamps would be useful in water and air purification systems. AlGaN based light-emitting diodes (LEDs) are being developed to that end. Their still poor efficiency limits their wide spread use, however. Indeed, the wall plug efficiency (WPE) of UV-LEDs decreases due to the deepening of Mg acceptor levels (necessary for p-type doping) as the bandgap increases. This results in an increase of the access resistance on the p-side of LEDs. Commonly, this issue is addressed by the deposition of a p-GaN layer on top of the LED, the Mg acceptors in GaN being shallower compared to AlGaN. This is used in most commercial UV LEDs, at the expense of light extraction efficiency (LEE) because of UV absorption in the top GaN:Mg layer. Tunnel Junctions (TJs) are a possible solution to this problem as both contacts of the UV-LED become “n” type. In addition, out-of-equilibrium hole generation will increase hole injection in the active region, improving the performance of the device.

Having efficient TJs made from high bandgap materials requires very high doping on n and p sides of the TJ and a tunnelling current as high as possible. To reach those goals, we developed a hybrid MBE / MOVPE approach whereby the top n++ AlGaN layer was grown by MBE on top of the MOVPE grown UV emitting quantum well heterostructures. We also used thin interlayers within the junction to improve the tunneling current.

Main Results

We used Ge instead of Si doping for the n++ MBE grown top layer of the TJ. This was compulsory as we used NH_3-MBE: Using Si as a dopant would have been difficult, as the Si cell would have been nitridated by NH_3. Ge doping was calibrated using GaN epilayers, and state-of-the-art mobility (67 cm^2/Vs) and resistivity ($1{,}7.10^{-4}$ Ω.cm) at an electron concentration of $5{,}5.10^{20}$ cm^{-3} for Ge-doped GaN were reached.

Ge-doped $Al_{0.5}Ga_{0.5}N$ tunnel junctions were deposited on top of MOVPE UV light emitting diodes emitting in the 300 nm range (with $Al_{0.3}Ga_{0.3}N$ quantum wells). Room temperature CW electroluminescence showed a single peak emission at 304 nm with weak deep-level emission in comparison with the band edge emission (Fig. 1a). The TJs caused voltage drops in the devices. This phenomenon was significantly reduced by the use of a 3.4 nm thick GaN interlayer between the p++ and n++ parts of the tunnel junction (Fig. 1b). The AlGaN TJs increased the optical power of UV LEDs, by factors of up to 6 for the AlGaN TJ with a thin GaN interlayer (Fig. 1c). This was due to higher electrical injection efficiencies thanks to the use of tunnel junctions in UV-emitting structures [1,2].

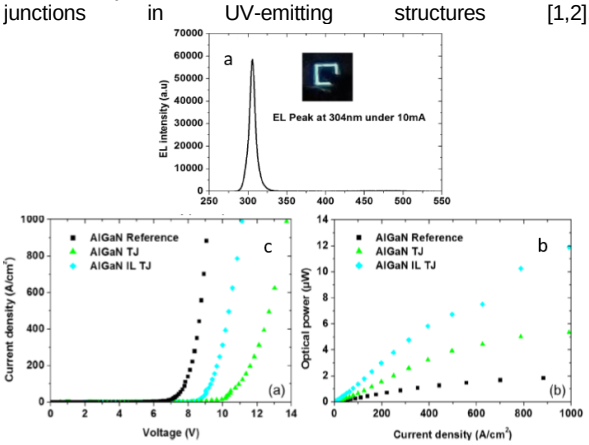


Figure 1: (a) Electroluminescence spectrum of an AlGaN UV-LED with a tunnel junction,(b) I-V characteristics of AlGaN LED with or without TJ, and with a TJ and a GaN interlayer (IL) (c) corresponding optical output powers.

Perspectives

This method should be evaluated for shorter wavelength UV-C LEDs, with InGaN interlayers for better tunnelling currents with even less voltage drops. Final aims would be EQE better than 10% with mW class UV-C LEDs and vertical emitters employing TJ UV-C LEDs.

RELATED PUBLICATIONS:
[1] V. Fan Arcara, G. Feuillet et al., J. Appl. Phys., 126, 224503, (2019), https://aip.scitation.org/doi/10.1063/1.5121379
[2] V. Fan Arcara, G. Feuillet et al., AIP. Adv, 9, 055101, (2019), https://aip.scitation.org/doi/10.1063/1.5092693

Nano-Pendeo Epitaxy of Nitride Compounds on Patterned SOI Substrates

RESEARCH TOPIC:

Strain and defect reduction in GaN templates for optoelectronic or electronic applications.

AUTHORS:

R. Dagher and G. Feuillet (J. Zuniga Perez, B. Alloing)[1], (C. Gourgon)[2]

Nanopendeo-epitaxy of gallium nitride (GaN) is a way of producing freestanding GaN with reduced strain and threading dislocation density (TDD). The novelty lies in the use of silicon on insulator (SOI) substrates patterned into nano-pillars down to the buried oxide (BOX). We take advantage of the creeping properties of SiO_2 at the GaN growth temperature to promote strain relaxation and grain-boundary dislocations reduction. We fabricate freestanding GaN vignettes, up to 10 µm-thick, and with lateral dimensions from 3 µm to 300 µm, spontaneously separated from the initial pillars. Structural and optical characterizations show that the vignettes are crack-free and almost fully relaxed, with a TDD of ~2-3×10^8/cm^2.

SCIENTIFIC COLLABORATIONS: [1]CNRS-CRHEA, [2]CNRS-LTM

Context and Challenges

Hetero-epitaxial growth implies lattice mismatched materials and most of the time materials with different thermal expansion coefficients. Hence, hetero-epitaxial layers suffer from high threading dislocation densities (TDD) and accumulated stress, which are detrimental to device efficiency. Many methods have been developed based on localized growth to tackle these issues. For GaN, nucleation areas can be reduced to minimize the dislocations at the substrate/nuclei interface with techniques such as epitaxial lateral overgrowth (ELO) through a dielectric mask, or pendeo-epitaxy (PE) without a mask. Although these techniques are advantageous, they have other issues such as an inhomogeneous TD distribution, concentrated in the window region (for ELO) or located at the coalescence boundaries of crystallites from different nucleation sites (for PE). Indeed, crystallites approaching each other from independent nucleation sites inherit the crystallographic misalignment associated to the hetero-epitaxial growth, which will generate threading boundary dislocations (BD).

Main Results

To overcome this misalignment problem and reduce the TDD, we have introduced a bottom-up approach based on pendeo-epitaxy of GaN on nano-patterned silicon on insulator (SOI) templates. The idea is to have crystallites on top of deformable nano-pillars (Fig. 1a), which would then act as "rotating" nano-pedestals. The buried SiO_2 layer of an SOI substrate enables us to do that because of its creeping properties at the growth temperature of GaN (~1100°C). Indeed, with the right pillar dimensions (< 200 nm) and growth temperature, it should be energetically favorable for crystallites to rotate on their deformable base to align crystallographically with each other instead of generating BD.

SOI substrates have been patterned using nano-imprint lithography, followed by a 2-step MOVPE growth by pendeo-epitaxy of GaN vignettes with different dimensions (300×300 down to 3x3 µm^2). 5 and 10 µm-thick GaN vignettes were produced on top of nano-pillars (Fig. 1b, 1c and 1e). They were crack-free with a TDD down to 5.10^7/cm^2 (typically 10^9 on Si and 4×10^8 on sapphire), as shown by AFM and cathodoluminescence. Most interestingly, fracture lines were found in the SiO_2 layer close to the nanopillars (Fig. 1d), resulting in freestanding GaN vignettes [1,2]. This opens up interesting opportunities for easy device transfer processes.

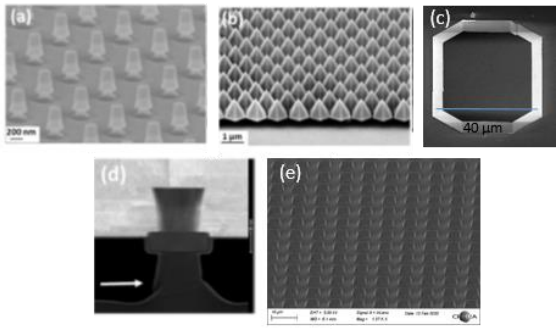


Figure 1: (a) SOI nano-imprint nanopillars, (b) 1st growth step: nanopyramids nucleation on the SOI nanopillars, (c) 2nd growth step: a 40x40 µm GaN vignettes after coalescence, (d) STEM image showing dislocations aligned parallel to the surface and pillar cracking, (e) array of 5x5 µm GaN vignettes.

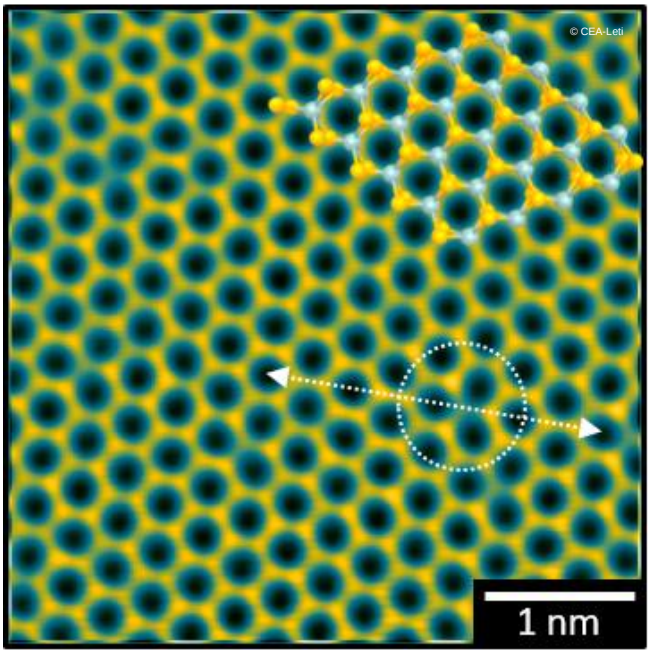
Perspectives

These first results open new possibilities for devices with reduced dimensions such as µ-displays. Indeed µ-LEDs are usually fabricated using a top-down etching of a full wafer quantum well heterostructure. Etching leaves a defective zone at the periphery of the µ-LED which becomes predominant as the dimensions of LEDs become smaller. Using the bottom-up approach as detailed above enables to avoid such etching, improving the overall efficiency of the µ-LEDs. We also want to go a step further in dislocation reduction in the template by resorting to bio-inspired growth process with very innovative nano-patterning geometries.

RELATED PUBLICATIONS:

[1] R. Dagher et al., J. of Crystal Growth 526 (2019), 125235; https://doi.org/10.1016/j.jcrysgro.2019.125235

[2] R. Dagher et al. 13th International Conference on Nitride Semiconductors 2019 (ICNS-13), 2019; https://mrs.org/icns-13/program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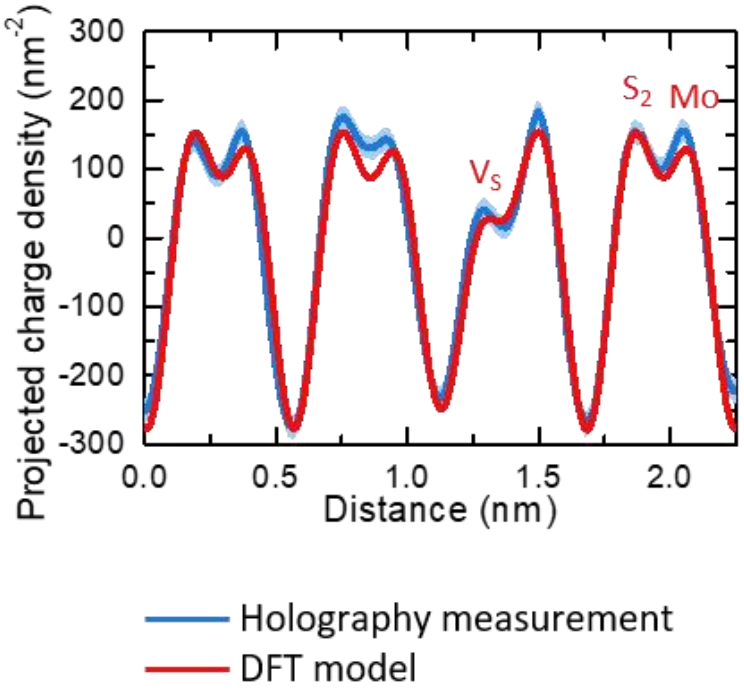
1 nm


Projected charge density (nm^{-2})
300
200
100
0
-100
-200
-300
0.0
0.5
1.0
1.5
2.0
Distance (nm)
S_2
Mo
V_S
Holography measurement
DFT model

09 CHARACTERIZATION

- Line Width Roughness: First Experimental Proof of the PSD Determination from a SAXS Pattern
- High Resolution Field Mapping through Computer Controlled Transmission Electron Microscopy and Advanced Analysis Techniques
- Operando Photoemission under Electrical Bias for Device Technology
- Non-Destructive Metrology of Elemental Depth-Profiles in Thin Layered Memory Stacks
- Contribution of Secondary Ion Mass Spectrometry (SIMS) to the Understanding of Switching Mechanisms and Optimisation of Advanced Random Access Memory Architectures
- Plasma Profiling Mass Spectrometry for the Development of Advanced Power & Memory Devices

Line Width Roughness: First Experimental Proof of the PSD Determination from a SAXS Pattern

RESEARCH TOPIC:
Lithography, nano-characterization, line roughness

AUTHORS:
J. Reche, P. Gergaud, Y. Blancquaert, (M. Besacier)[1], (N. Boudet)[2], (G. Freychet)[3].

For the most advanced nodes, line roughness reaches the same order of magnitude as the CD (Critical Dimension) with a huge impact on power consumption. Hence, the control of this morphological aspect requires a suitable metrology. CD-SEM is a widely used technique for roughness extraction. It relies on the determination of the Power Spectrum Density (PSD) that enables to obtain roughness information in frequency space. SAXS has been identified as one of the highest potential techniques for nanoelectronics by the ITRS. This study is based on programmed roughness simulations and first experimental measurements. It demonstrates that a complete PSD can be extracted from a SAXS analysis and that extended roughness information can be derived. Comparison of SEM and SAXS proves the capability of SAXS technique for the PSD extraction of line roughness.

SCIENTIFIC COLLABORATIONS: [1]LTM-CNRS; [2]BM02-ESRF; [3]NSLS-II-Brookhaven Nat. Lab.

Context and Challenges

As the semiconductor industry continues to pursue the miniaturization of transistor devices, or to stack them using to 3D integration, line roughness becomes critical. The link between line roughness and failure has been demonstrated and it is therefore essential to reduce it. The huge challenge of line roughness metrology in terms of accuracy and reliability has not been reached yet for the current targeted nodes. Over the past 15 years, the design and fabrication of line gratings with controlled periodic roughness have been used for the development of roughness extraction methodologies for SEM (scanning electron microscopy), AFM (atomic force microscopy) and optical scatterometry as well as for Small Angle X-ray Scattering (SAXS). Nevertheless, the specific case of periodic roughness is far from the real samples encountered in device fabrication. Our purpose within this study was to go further in the line roughness analysis with SAXS by analyzing realistic samples.

Main Results

The SAXS technique is based on the measurements and analysis of diffraction patterns, in reciprocal space. Usually, data analysis is performed through inverse problem solving based on sample modelling. Several studies were focused on correlated or anti-correlated edges of structures with periodical roughness. These studies were limited to the extraction of roughness amplitude without detailed information on frequency. For the first time, extraction of the Power Spectrum Density (PSD) of Line Width Roughness (LWR) with the SAXS technique is demonstrated. Firstly, results obtained from simulations (Fig.1) enabled to extract the PSD at some nodes in the diffraction patterns where the form factor induces complete extinction of the diffracted signal. In this case, the PSD can be fully determined. This methodology is then applied to real samples and experiments (Fig 2.a). The shape of the PSD, parameters α and ξ, could be determined while the values of σ needs more treatment or input parameters. Results were compared with CD-SEM as the technique of reference (Fig 2.b) and good agreements were found.

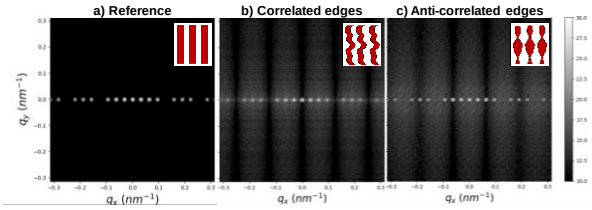


Figure 1: Diffraction pattern of different virtual samples generated with the same input parameters α = 0.5, ξ = 20 nm and σ = 2 nm: (a) Reference sample, (b) Correlated edges (pure Line Edge Roughness), (c) Anti-correlated edges.

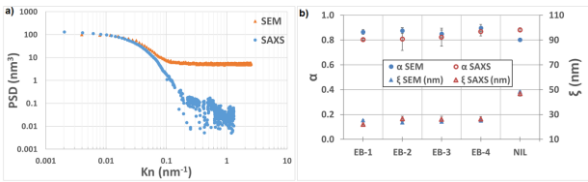


Figure 2: (a) PSD obtained on real sample with SEM and SAXS; (b) Roughness parameters α and ξ obtained from CD-SEM and CD-SAXS analysis for the considered samples

Perspectives

Raw PSD obtained with SAXS are less noisy than SEM PSD and allow access to very low frequencies. Nevertheless, fitting parameters errors are currently higher with SAXS mainly because of low counting statistics. This could be easily improved from an experimental point of view using a dedicated setup but also by averaging the PSD extraction on several form factor extinction positions. This aspect is currently in progress.

RELATED PUBLICATIONS:
[1] J. Rêche et al., Proc. SPIE Vol.10959, (2019), https://doi.org/10.1117/12.2514919
[2] J. Rêche, PhD thesis, Université Grenoble Alpes, (2019). http://www.theses.fr/2019GREAT050

High Resolution Field Mapping through Computer Controlled Transmission Electron Microscopy and Advanced Analysis Techniques

RESEARCH TOPIC:
Measurement of Electric, Magnetic and Strain Fields

AUTHORS:
D. Cooper, V. Boureau

The development of semiconductor devices such as light emitting diodes (LEDs) and 2D materials leads to a need to measure fields at high spatial resolution and sensitivity. Previously, off-axis electron holography had a spatial resolution of around 5 nm. However, from the use of aberration correction, computer control of the microscope for the automation of long experiments and from novel reconstruction techniques, it is now possible to measure fields such as the electrostatic potential and charge density with atomic resolution. These methods have been applied to a range of materials, from SOI CMOS devices, InGaN/GaN Quantum Well structures, Magnetic memories and 2D materials. This approach is now used routinely on the PFNC to provide valuable information to link these fields with the electrical and optical properties of the devices.

Context and Challenges

The fields in semiconductor devices arising from dopants, piezoelectric effects, strain change their conduction band and hence their electronic properties. The measurement of these fields has always been considered a difficult challenge. In addition, the recent focus on magnetic devices for both data storage and quantum computing mean that it is necessary to have a characterisation technique available to support developments for these novel devices.

Main Results

Off-axis electron holography is a transmission electron microscopy (TEM) based technique that uses an electron biprism to interfere an electron wave that has passed through a region of interest with a wave that has passed through vacuum. From the resulting interference pattern, known as the hologram, the electron phase can be reconstructed. The electron phase carries information about the electromagnetic fields in the specimen and as such we are able to provide maps with nm-scale information.

In this work a state of the art FEI Titan Ultimate has been used to optimize all aspects of electron holography. Firstly, correction is used to reduce the aberrations in the lenses. To improve the signal to noise, the microscope is controlled to acquire large series of electron holograms with the drift of the microscope aberrations and specimen being removed. Finally, by combining novel reconstruction techniques with advanced data acquisition methods, the spatial resolution can be increased by a factor of two. All of these methods are now routine using integrated software written at the PFNC.

Figure 1.a shows a map of the conduction band in a series of 2.2 nm wide InGaN quantum wells in a GaN LED acquired by electron holography. The spatial resolution is sub-nm. Comparison with simulations in Fig. 1.b and 1.c shows that the measurement is quantitative. For a more challenging specimen, the electrostatic potential has been measured in a monolayer of MoS_2 (Fig. 1.d). The excellent signal to noise allows the charge density to be calculated which shows the charge re-distribution in the Mo and S_2 atomic sites. These results are consistent with density functional theory (DFT) simulations.

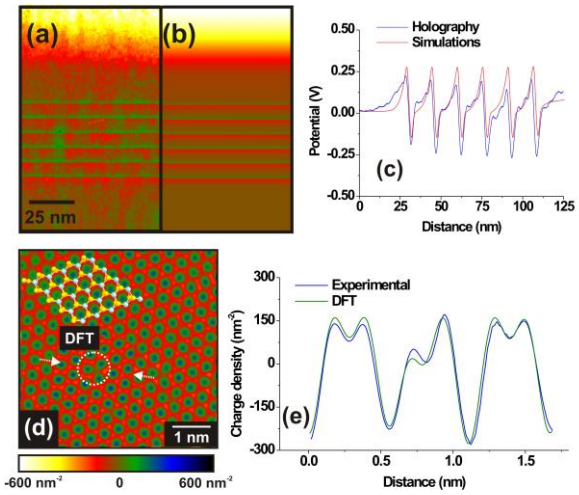


Figure 1: (a) A quantitative map of the conduction band in a InGaN/GaN LED. (b) and (c) Comparison with simulations and. (d) A map of the charge density for a monolayer of MoS_2. The charge density has been measured across a defect and the electronic redistribution is coherent with DFT simulations.

Perspectives

These developments are now being used routinely on the PFNC to aid the development of the next generation of semiconductor devices. The next steps are to combine these methods with *in situ* operation.

RELATED PUBLICATIONS:

[1] B. Haas, V. Boureau et al., Ultramicroscopy (2019) https://doi.org/10.1016/j.ultramic.2018.12.003

[2] V. Boureau et al., ACS Nano (2019) https://doi.org/10.1021/acsnano.9b06716

Operando Photoemission under Electrical Bias for Device Technology

RESEARCH TOPIC:

Operando photoemission under electrical bias for chemical and/or electrostatic analyses of critical interfaces in microelectronic devices.

AUTHORS:

E. Martinez, O. Renault, C. Leroux, B. Meunier, P. Kumar, V. Loup, F. Gaillard, (F. Domengie)[1], (C. Jimenez)[2], (J.-P. Rueff)[3]

Operando photoemission, i.e photoemission under *in situ* electrical bias, was developed to investigate the critical interfaces of device structures. Biasing the device while performing measurements is very helpful to better understand the materials behavior under real operating conditions. This is illustrated here firstly for high-k/metal gate stacks with Al and La additives to investigate interfacial dipoles. The relative core level shifts are directly correlated to the high-k/SiO_2 dipole modulation with Al or La insertion. Operando hard X-ray photoemission was also implemented at the SOLEIL synchrotron to probe resistive memories based on lanthanum manganite (LMO). Results highlight a redox reaction at the LMO/top electrode interface driven by oxygen drift when switching the memory.

SCIENTIFIC COLLABORATIONS: [1]ST Microelectronics, [2]CNRS/LMGP, [3]SOLEIL Synchrotron

Context and Challenges

X-ray photoemission techniques are often used to study chemical changes at critical interfaces of complex stacks in device technology. However, studying the interface behaviour during device operation is still very challenging. Operando XPS under electrical bias was implemented to address this key issue.

Main Results

Firstly, high-k/metal gate stacks with Al and La additives were analyzed to get information about interfacial dipoles [1]. Operando XPS under bias was performed on specific devices with thinner TiN gates (Fig. 1). Results were correlated to ex-situ electrical measurements, to estimate parasitic bias drops across the device. Relative core level shifts highlight the high-k/SiO_2 interfacial dipole modulation with Al(La) insertion (Fig. 1).

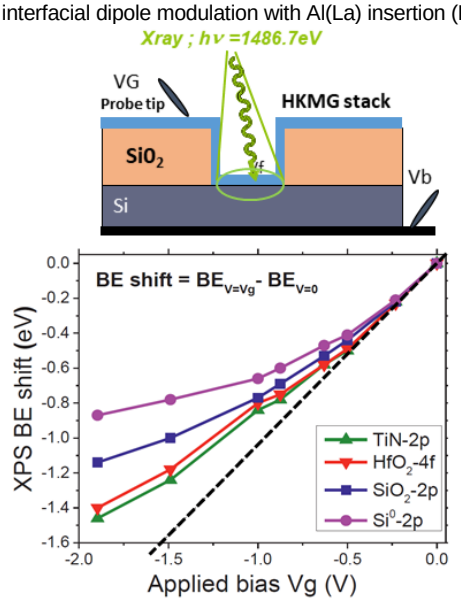


Figure 1: Setup for operando XPS and peak shifts versus bias.

Oxide resistive memories (OxRRAMs) based on perovskites such as $LaMnO_{3+\delta}$ (LMO), were investigated using operando hard X-ray photoelectron spectroscopy (HAXPES) at the SOLEIL synchrotron. Results help understanding chemical changes at the critical LMO/top electrode (TiN) interface when switching the resistive state of the memory (Fig. 2). A redox reaction at the TiN/LMO interface triggered by oxygen drift under electrical bias was evidenced [2].

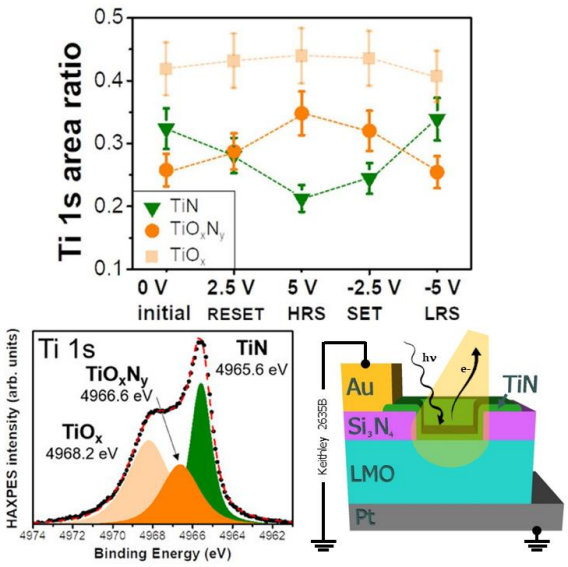


Figure 2: Relative areas and fit of the Ti1s peak, setup for operando HAXPES.

Perspectives

Operando photoemission under *in situ* electrical bias is very promising to understand the devices behavior in real operating conditions. It is especially helpful to investigate changes at critical interfaces upon device operation. In fact, not only chemical information such as oxidation states can be obtained, but also the distribution of charges.

RELATED PUBLICATIONS:

[1] P. Kumar, E. Martinez et al., 2018 IEEE International Electron Devices Meeting (IEDM), https://doi.org/10.1109/IEDM.2018.8614554

[2] B. Meunier, E. Martinez et al., J. Appl. Phys. 126, 225302 (2019),https://doi.org/10.1063/1.5125420

Non-Destructive Metrology of Elemental Depth-Profiles in Thin Layered Memory Stacks

RESEARCH TOPIC:
Metrology, hybrid metrology, X-ray metrology, composition, advanced memory

AUTHORS:
E. Nolot, Y. Mazel, (P. Hönicke, B. Detlefs, B. Beckoff)[1]

The reliability and performances of the materials investigated for advanced non-volatile memory can be strongly influenced and fine-tuned by the stoichiometry, composition gradients, and surface/interface management. We investigate the combination of X-ray reflectometry (XRR) and X-ray fluorescence (XRF), both in grazing incidence geometry (GI). First, we show that GIXRF-XRR permits to reduce significantly the cross correlation effects that can falsify the modelling results in XRR-only analysis. Then, we demonstrate that GIXRF-XRR can reliably determine mass deposition, thickness, composition, and the elemental depth-profile in thin-layered stacks, thereby providing a relevant non-destructive metrology technique to support materials engineering for memory applications.

SCIENTIFIC COLLABORATIONS: [1]PTB (Physikalisch-Technische Bundesanstalt)

Context and Challenges
Thin layered materials are at the core of phase change random access memory (PCRAM) and oxide-based resistive switching memory (OxRAM). The reliability and performance of these complex materials are closely linked to their chemical and structural properties, which can be strongly influenced and fine-tuned by the stoichiometry, composition gradients, and surface/interface management. The development of dedicated non-destructive metrology schemes based on X-ray techniques permit to support and accelerate materials engineering, which enables the tuning and the improvement of the electrical performances of the memory device.

Main Results
X-ray reflectometry is a well-established in-fab technique for sample systems with sufficiently high electron density contrast and thickness larger than a few nanometers, where the angular oscillations provide a direct and traceable access to the thickness. However, an XRR-only strategy may suffer from inter-parameter dependencies when dealing with complex stacks of multiple layers, low electron density contrast, or very thin layers without any pronounced angular minima.

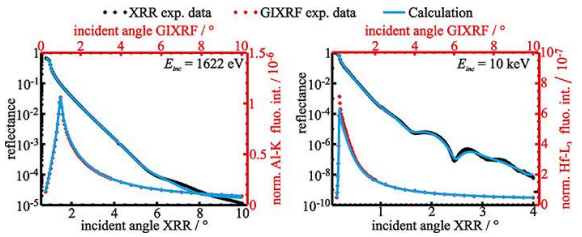


Figure 1: Combined analysis of XRR and GIXRF data for ultrathin $Al_2O_3/HfO_2/Al_2O_3/SiO_2$ stack deposited on Si [1]

This issue can be addressed with X-ray fluorescence, which determines the mass deposition (product of density and thickness) that can be used to independently validate any XRR modeling result. In addition, depth-dependent information can be deduced from the combination of electronic density and atomic density profiles, using hybrid grazing-incidence XRF (GIXRF) and XRR analysis

We used ultrathin Al_2O_3/HfO_2 stacks grown by ALD to demonstrate how cross correlation effects can degrade the uncertainty in XRR-only analysis [1]. Then, we showed that mass deposition deduced from reference-free XRF (Fig.1) performed at PTB (National Metrology Institute) does reduce the uncertainty in the quantitative analysis of ALD stacks. Finally, hybrid GIXRF-XRR was used to unambiguously reveal interfacial intermixing in ALD stacks after an annealing step at 800°C (Fig.2).

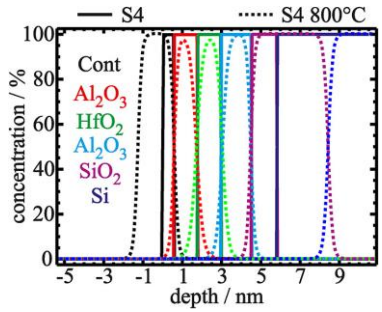


Figure 2: GIXRF-XRR-deduced elemental depth-profile of $Al_2O_3/HfO_2/Al_2O_3/SiO_2$ stack, as deposited and after annealing.

Perspectives
Inline metrology tools with GIXRF-XRR capability are now emerging, which may accelerate material engineering for advanced memory, providing evidence of the influence of the surface/interface and elemental depth-distribution on the material performances, which are so far deduced from advanced scanning transmission electron microscopy and high-resolution X-ray photoelectron spectroscopy [2].

RELATED PUBLICATIONS:
[1] P. Hönicke, E. Nolot et al., J. Vac. Sci. Technol. A 37, 041502 (2019), https://doi.org/10.1116/1.5094891
[2] A. N. D. Kolb, N. Bernier et al., ACS Appl. Electron. Mater. (2019), https://doi.org/10.1021/acsaelm.9b00070

Contribution of Secondary Ion Mass Spectrometry (SIMS) to the Understanding of Switching Mechanisms and Optimisation of Advanced Random Access Memory Architectures

RESEARCH TOPIC:
Chemical characterisation for memory applications

AUTHORS:
M. Veillerot, R. Gassilloud, G. Molas, (J.Chatterjee, E. Gautier, B. Dieny)[1], (C. Vallee)[2]

The digital conversion that is taking place over all human activities leads to growing needs for data storage and data management. Continuous efforts are made by the microelectronics industry to offer the most adapted devices to the growing number of applications. These efforts notably lean on sophisticated chemical characterization techniques such as SIMS which, through its exclusive, outstanding properties for all the elements of the periodic table (e.g., very high depth resolution in nm range and large sensitivity possibly down to the ppb level), helps to unravel the subtle switching mechanisms of these devices.

SCIENTIFIC COLLABORATIONS: [1]IRIG-SPINTEC, [2]LTM-CNRS

Context and Challenges
Post-CMOS (complementary metal oxide semi-conductor) alternative technologies are becoming critical for the chip industry. Recently, alternative emerging technologies have gained interest and target new applications such as embedded device market, new computer architecture paradigms, or flash memory replacement. For instance, Magnetic (M-) or hybrid resistive (HR-) Random Access Memories (RAM) are very attractive candidates because of the improved performances they offer in terms of retention, thermal stability, storage density or speed.

Main Results
Whatever the type of the memory, the characterisation of the elemental depth distribution of the active layers is essential. For instance, the active part of one kind of M-RAM is a perpendicular magnetic tunnel junction (pMTJ) composed of a CoFeB/MgO/CoFeB stack, sandwiched by metallic layers (Fig. 1) aimed at limiting the B diffusion during crystallisation annealing steps.

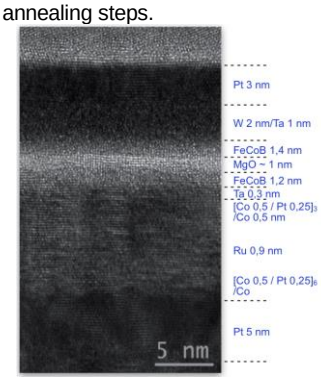


Figure 1: TEM cross section image of a pMTJ M-RAM stack, here after a 425°C anneal.

Such structures were studied with SIMS in very low impact energy conditions to limit primary beam induced damage. The interest of using tungsten (W) instead of tantalum (Ta) to limit the unwanted co-diffusion of iron (Fe) from the junction, even at higher annealing temperatures was demonstrated [1].

A second example is related to oxide-based conductive bridge random access memories where two distinct resistive states can be obtained based on a reversible filament formation. More specifically, the impact of transition metals and oxygen vacancy balance in filament composition is the key factor in memory performance. In Fig. 2, the elemental depth distribution of copper and oxygen obtained from SIMS characterisation are given for $CuTe_xGe_x/Ta_2O_5$ HR-RAM nanometric structures [2].

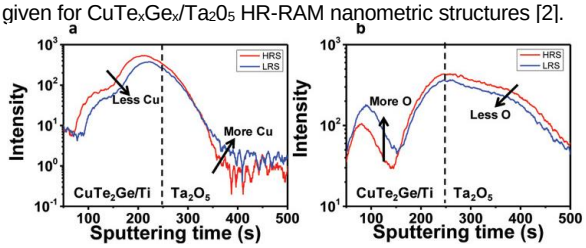


Figure 2: (a) Copper and (b) oxygen ToF-SIMS profiles in High (HRS-red lines) and Low (LRS-blue lines) Resistive States for Ta_2O_5/Cu memory.

From the SIMS depth profile acquired in careful, undamaging conditions, the balance between copper and oxygen vacancies can be established, depending the conductive state of the memory. In LRS state, the Cu intensity decreases in the $CuTe_2Ge$/Ti region and increases in Ta_2O_5 region. Reciprocally, oxygen decreases in Ta_2O_5 and increases in $CuTe_2Ge$/Ti indicative of the formation of oxygen vacancies in Ta_2O_5.

Perspectives
This type of result is actually of great benefit because it helps to support technological sectors at various degrees of maturity. In the case of M-RAM, it allows to demonstrate the compatibility of this very young field with standard microelectronics processes and thus make it a very credible path. In the case of HR-RAM, by a detailed understanding of the physico-chemical mechanisms of switching of these memories, a classification was made possible, providing insights on how to choose the most suitable technology (resistive layer and electrodes) for a given application with required specifications.

RELATED PUBLICATIONS:
[1] J. Chatterjee, M. Veillerot et al., Applied Physics Letters, (2019), https://doi.org/10.1063/1.5081912
[2] G. Molas et al., Advanced Electronic Materials, (2019), https://doi.org/10.1002/aelm.201800658

Plasma Profiling Mass Spectrometry for the Development of Advanced Power & Memory Devices

RESEARCH TOPIC:
Metrology, elemental depth profiling, mass spectrometry, material analysis

AUTHORS:
Y. Mazel, E. Nolot, J.-P. Barnes, (S. Legendre, A. Tempez)[1]

Plasma Profiling Time-Of-Flight Mass Spectrometry (PP-TOF-MS) is an innovative technique for the elemental depth profiling of single and multi-layered materials. The advantages of the technique are its analytical speed, its ability to provide semi-quantitative results for most elements as well as its ease-of-use. It is therefore ideally suited for in-line metrology, in complementarity with conventional Time-Of-Flight Secondary Ion Mass spectrometry (TOF-SIMS). In this work we present recent application cases in the fields of embedded memories and power electronics, illustrating the fast and reliable feedback process experts can benefit from using the technique.

SCIENTIFIC COLLABORATION: [1]Horiba France SAS

Context and Challenges
Accurate depth profiling of materials is a critical characterization step during process development since a wide range of properties are driven by elemental composition and depth distribution. Powerful techniques such as TOF-SIMS can fulfil this need but proper methodology and instrument operation are often complex. Moreover, instruments are in high demand and turnaround times can limit the number of iterations available for process development.
PP-TOF-MS is presented here as a complementary technique suitable for metrology, with its abilities to provide a fast semi-quantitative feedback while being easier to operate, reserving more complex characterization techniques for the final fine-tuning of the process. With a sputtering rate up to 10 nm/s, sample introduction and analysis typically require less than 5 minutes with the prerequisite of a few hours of training.

Main Results
The first example concerns a GeSbTe alloy used for embedded memories. The material properties are strongly related to its composition and surface modification plays a big role as devices shrink. Figure 1 illustrates how quickly the technique captures the surface stoichiometry modification undergone by the material when treated by different etching plasmas.

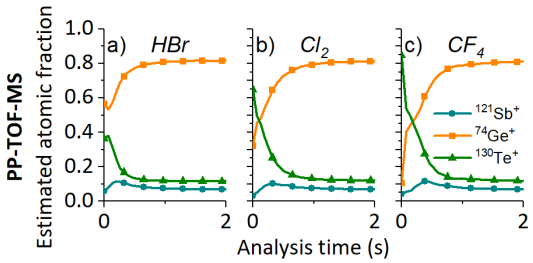


Figure 1: Elemental depth profiles obtained for GeSbTe etched with different halogen plasmas. Surface modification is clearly revealed using PP-TOF-MS.

PP-TOF-MS has been extensively used for etching plasma selection and the study of GeSbTe ageing under air exposure. More results and comparison with other characterization techniques can be seen elsewhere [1].
The second example is the quantification of Ga contamination in epitaxially grown InAlN used for high-power electronics and optoelectronics devices. Ga contamination is a major concern as it hinders reproducibility of the growth process and leads to lower than expected In content and electrical performances.
Depth resolved analyses are mandatory here as Ga is unwanted in some layers but required in others. Thanks to its fast feedback and ease-of-use, PP-TOF-MS was able to assist epitaxy experts in the understanding and fine-tuning of their epitaxy reactor and process conditions (Figure 2). State-of-the-art results were achieved with almost gallium free InAlN layers [2, 3].

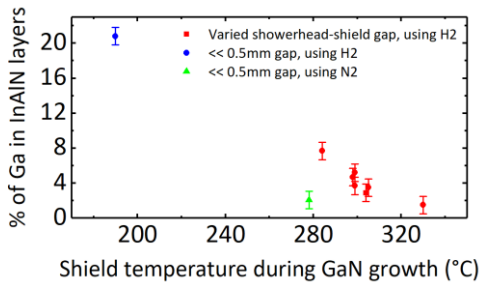


Figure 2: Quantification of Ga in InAlN layers as a function of the process conditions using PP-TOF-MS.

Perspectives
Despite its uniform sensitivity for a wide range of elements, the technique still lacks sensitivity for oxygen. Alternative gases for the sputtering plasma are being investigated and show great potential.
Post-treatment of the depth profiles is also under investigation. The objective is to improve the achievable depth resolution and come closer to reference techniques.

RELATED PUBLICATIONS:
[1] Y. Canvel, C. Boixaderas et al., J. Vac.Sci.Technol.,. (2019), https://doi.org/10.1116/1.5089037
[2] M. Mrad et al., Appl. Phys. Express, (2019), https://doi.org/10.7567/1882-0786/ab0bbb
[3] M. Mrad et al., J. of Crystal Growth (2019), https://doi.org/10.1016/j.jcrysgro.2018.10.039

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10 PHD DEGREES AWARDED IN 2019

- Lina KADURA, Thomas BEDECARRATS
- Neil ROSTAND, Mario BARLAS
- Rana ALHALAB, Alberto DRAGONI
- Corentin PIGOT, Anne PAQUET
- Guido RADEMAKER, Maxime HERMOUET
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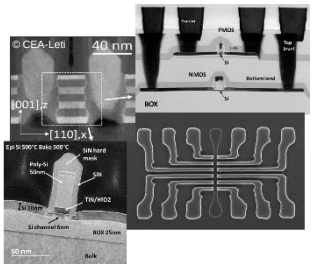
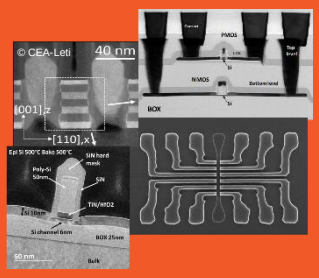


LINA KADURA

STUDIES OF FDSOI TECHNOLOGY-BASED NEW ARCHITECTURES OF INTEGRATED COMPONENTS SENSITIVE TO LIGHT FOR APPLCIATIONS SUCH AS IMAGERS

Université Grenoble Alpes (France)

A new type of light sensor called FDPix, composed of one transistor (1T) per pixel is investigated. It consists in co-integrating an FDSOI (Fully-Depleted Silicon-On-Insulator) transistor with a photodiode to enable light sensing through optical back biasing. The absorption of photons and resulting photogenerated charges in the diode result in a Light Induced VT Shift (LIVS). The LIVS is due to a capacitive coupling between the front and back gates of the FDSOI transistor and represents the key performance metric to be extracted and optimized. In this work, the device behavior in dc and transient domains was thoroughly investigated and modeled. Although not limited to this node, all the devices tested were fabricated using 28nm node FDSOI technology. By means of TCAD simulations and opto-electrical characterization, the device parameters such as Body Factor (BF) and junction profile were optimized to improve its performance. It was found that the FDPix is in fact a dual response sensor. It exhibits a linear response at low light intensity which results in high sensitivity, and a logarithmic response at higher intensities that ensures a high dynamic range (DR) of more than 120dB. The dedicated developed compact model is implemented in SPICE environment for circuit design. New pixel circuit in analog and digital domain, based on the FDPix were designed, fabricated, and tested. The results obtained and presented in this work, shows the potential of using the FDPix sensor for smart, highly embedded, low power image sensors for More-than-Moore applications.

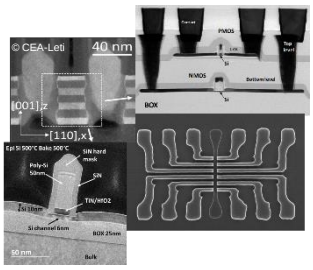


THOMAS BEDECARRATS

STUDY AND INTEGRATION OF A LOW POWER AND LOW FOOTPRINT BIMOS-BASED ANALOG SPIKING NEURON CIRCUIT IN 28 NM FD-SOI TECHNOLOGY

Université Grenoble Alpes (France)

While Moore's law reaches its limits, microelectronics actors are looking for new paradigms to ensure future developments of our information society. Inspired by biologic nervous systems, neuromorphic engineering is providing new perspectives which have already enabled breakthroughs in artificial intelligence. To achieve sufficient performances to allow their spread, neural processors have to integrate neuron circuits as small and as low power(ed) as possible so that artificial neural networks they implement reach a critical size. In this work, we show that it is possible to reduce the number of components necessary to design an analogue spiking neuron circuit thanks to the functionalisation of parasitic generation currents in a BIMOS transistor integrated in 28 nm FD-SOI technology and sized with the minimum dimensions allowed by this technology. After a systematic characterization of the FD-SOI BIMOS currents under several biases through quasi-static measurements at room temperature, a compact model of this component, adapted from the CEA-Leti UTSOI model, is proposed. The BIMOS-based leaky, integrate-and-fire spiking neuron (BB-LIF SN) circuit is described. Influence of the different design and bias parameters on its behaviour was deeply characterized during measurements performed on a processed demonstrator. A simple analytic model of its operating boundaries is proposed. The coherence between measurements, compact simulation results and predictions coming from the simple analytic model attests to the relevance of the proposed analysis. In its most successful achievement, the BB-LIF SN circuit is 15 µm², consumes around 2 pJ/spike, triggers at a rate between 3 and 75 kHz for 600 pA to 25 nA synaptic currents under a 3 V power supply.

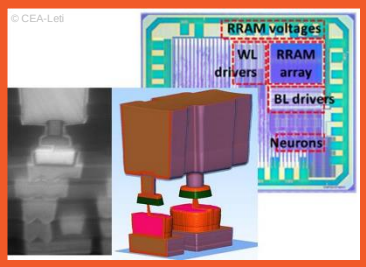


NEIL ROSTAND

PHYSICAL MODELING OF NATURAL RADIATION IMPACT ON SUB-28 NM TECHNOLOGIES

Toulouse ISAE (France)

The Impact of natural radiations on electronic devices is a major concern for reliability of circuits, regardless of their application (astronautics, aeronautics and even automotive at ground stage). Radiations only differ by the type of particles striking the circuits. When exposed to such particles, free carriers are generated in the constituting materials. At transistor level this results in current pulses collected at the electrodes known as “Single Event Transient”. Those current pulses can largely disturb circuit operation and more specifically generate errors during data processing/storage. Such errors are known as “soft errors”. Furthermore, permanent exposure of circuits can induce drift of the electrical characteristics of transistors known as “Total Ionizing Dose” effects.
Many SET models exist in literature. Some are derived from physical equations but do not fit with compact modelling constraints while some others are reduced to behavioural descriptions in Verilog-A with little physical content. Also, when passing from BULK to SOI technologies, new physical phenomena (such as bipolar amplification or significance of charge generation spatial distribution) are more dominant, requiring a more careful physical description.
In this PhD work, we propose a novel SET compact model for SOI technologies based on an equivalent electrical circuit. Using this model, transient SPICE simulations of a 6T-SRAM was performed to demonstrate the capability to reproduce “Single Event Upset” (SEU) which is the SET induced bit state inversion of a memory cell. TID effects were also included in the CEA-Leti compact model devoted to FDSOI technology “L-UTSOI” by considering irradiation of oxides and non-uniform interface traps energetic distribution. TCAD simulations have been widely used to support model developments and validation.

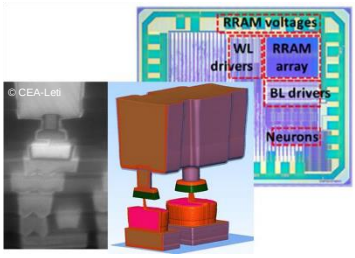


MARIO BARLAS

OXRAM NONVOLATILE MEMORY DEVELOPMENT AND CHARACTERIZATION FOR ADVANCED CMOS NODES ON SOI SUBSTRATES

Université Aix-Marseille (France)

Transition Metal Oxide Resistive RAM (ReRAM) is a class of non-volatile memory technologies where the switching between memory states is enabled by the reversible breakdown of the oxide by means of the creation and dissolution of a percolated conduction path (filament). The main advantages of the technology lie in the scalability of the memory cell mainly owed to the sub 10 nm dimension of the filament, its low power consumption (< 300 pJ/ switch) and material compatibility with advanced CMOS technologies. Nevertheless, there are two major roadblocks that have prevented so far the implementation of ReRAM in large arrays: First, the requirement for voltages significantly higher than the operating voltage range for initial breakdown happening, (forming) and second, the intrinsic and extrinsic variability components arising from material interaction to its environment as well as the fundamental stochastic nature of percolative conduction. This work, is focused on HfO_2 based ReRAM technology. In the first part, we investigate different dopants to engineer the conductive properties of HfO_2 by combining a first-principles simulation approach and in-depth material characterization techniques. In the second part, the proposed $HfSiO_x$ alloy is integrated in the BEOL of a 130 nm process and the impact of the integration on forming, switching, error rate evolution and data retention is investigated. In the last part, a HfO_2 based integration in the early MOL of an advanced FDSOI 300 mm CMOS process is demonstrated allowing investigating standard HfO_2 ReRAM performances and limitations.

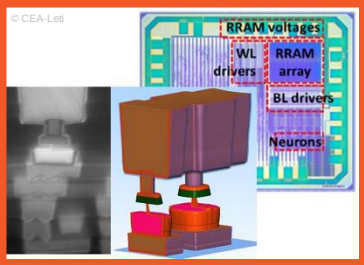


RANA ALHALABI

INNOVATIVE DESIGN OF LOGIC CIRCUITS AND MEMORIES IN CMOS/MAGNETIC TECHNOLOGY

Université Grenoble Alpes (France)

After many studies in recent decades, emerging nonvolatile memories are finally taking hold in the semiconductor market. Their main objective is to replace flash memories and DRAM, which are facing limitations in terms of density, miniaturization, consumption and speed improvement. Among the emerging NVM technologies, the magnetic memory MRAM has gained a lot of attention from the industry as an excellent candidate for the future nonvolatile memory market. Its performance allows integrating this memory into full custom and digital design flows. This would improve certain performances either at the elementary cell level or at the architectural level. Hence, we propose in the first part, the conception of CMOS / magnetic hybrid circuits of type LUT (Look Up Table) in STT-MRAM (Spin Transfer Torque) technology with the aim of realizing a demonstrator and testing it later. The full custom design involving a breadth of innovative LUTs has been implemented. We propose in the second part, the design of an embedded memory in SOT (Spin Orbit Torque) technology, for which a patent has been filed. Finally, both the SOT-MRAM and STT-MRAM have been integrated in a processor in order to evaluate the performances of these magnetic technologies in such circuits for widespread use.

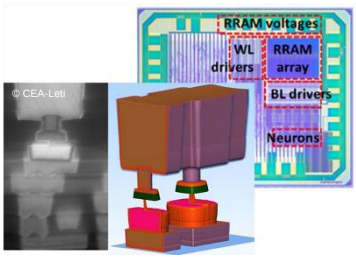


ALBERTO DRAGONI

AB INITIO SIMULATION OF ELECTRONIC TRANSPORT IN EMERGING OXRAM

Université Grenoble Alpes (France)

Resistive non-volatile memories based on oxides (OxRAM) are recently acquiring a wide interest for their performances, which make them promising candidates as storage memories to replace flash technology, and as embedded memories for neural network applications. Nevertheless, emerging OxRAM devices still present some drawbacks, like non-uniformity of switching parameters and switching failures. Overcoming these drawbacks requires a deeper comprehension of the OxRAM working principles, so far not completely understood. This can be achieved by means of ab initio simulations. Hence this work presents a careful characterization of HfO2, which is within the most promising materials to build OxRAM devices, by means of accurate quasi-particle (QP) calculations. A study of the electronic transport properties in OxRAM devices is also of primary importance. However, this requires a robust and reliable theoretical framework to compute the conductance of bulk metal/insulator junctions. The standard approach, based on density functional theory, Green function formalism, and Landauer formula, has some limitations and reliability issues. This work proposes a more reliable approach based on QP calculations, which provide a more accurate electronic structure to compute the conductance, and largely tests this new method on different junctions mimicking OxRAM devices.

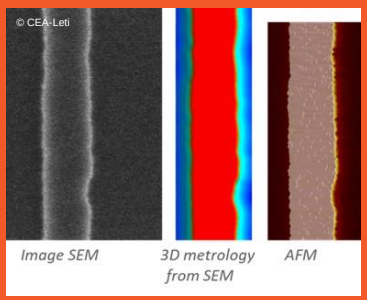


CORENTIN PIGOT

ELECTRICAL CHARACTERIZATION AND COMPACT MODELING OF ADVANCED EMBEDDED NON-VOLATILE MEMORIES

Université Aix-Marseille (France)

Phase-change memory (PCM) is arguably the most mature emerging nonvolatile memory, foreseen for the replacement of the mainstream NOR-Flash memory for the future embedded applications. To allow the design of new PCM-based products, SPICE simulations, thus compact models, are needed. Those models need to be fast, robust and accurate; Nowadays, no published model is able to fill all these requirements. In this work we propose a new compact model of PCM, enabling PCM-based circuit design. The model that we have developed is entirely continuous, and is validated on a wide range of voltage, current, time and temperature. Built on physical insights of the device, a thermal runaway in the Poole-Frenkel mechanism is used to model the threshold switching of the amorphous phase. Besides, the introduction of a new variable representing the melted fraction, depending only on the internal temperature, along with a crystallization speed depending on the amorphous fraction, allow the accurate modeling of all the temporal dynamics of the phase transitions. Moreover, an optimized model card extraction flow is proposed following the model validation, relying on a sensibility analysis of the model card parameters and a simple set of electrical characterizations. It enables the adjustment of the model to any process variation, and thus ensures its accuracy for the design simulation even in the early step of the technology development.

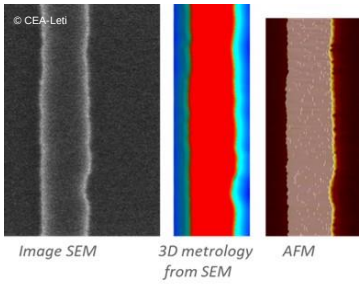


ANNE PAQUET

NEW CHEMOEPITAXY PROCESS DEVELOPMENT FOR BLOCK COPOLYMER ALIGNEMENT

Université Grenoble Alpes (France)

In order to offer a solution to constant evolution of microelectronics fab requirements in terms of lithography resolution, new lithography approaches are under study. One of these techniques consists of using self-assembling capabilities of Block Copolymer to form patterns such as contacts (cylinders) and line / space (lamellae). Two techniques are used to obtain a block alignment: grapho-epitaxy and chemo-epitaxy. Chemo-epitaxy, contrary to graph-epitaxy, offers space saving by aligning the blocs all over the studied field. Today, it is the most used technic. However, the current lithography requirements lead to the integration of high-chi block copolymers whose period are below 20 nm. With this dimension, the current chemo-epitaxy processes are not adapted anymore, due to the resolution limit of the standard lithography tools defining the guides. This thesis aims to introduce a new chemo-epitaxy process flow, called Process ACE, by using LETI 300mm process capability and Arkema's block copolymer advanced materials. In this new process, chemo-epitaxy guides are formed by combining standard lithography and established spacer patterning process. Spacer patterning technique is an option which, thanks to its aggressive dimensions, allows the integration of high-Chi block copolymers. A neutral underlayer, allowing perpendicular bloc copolymer orientation is located between the spacers. After the spacer removal, a selective grafting takes place to obtain an affine guide for one of the block. The final guide size corresponds to the one of the spacer processed earlier. In order to validate the process feasibility the thesis is divided in two parts. The first part investigates the critical process steps. The second part focuses on block copolymer alignment with process ACE.

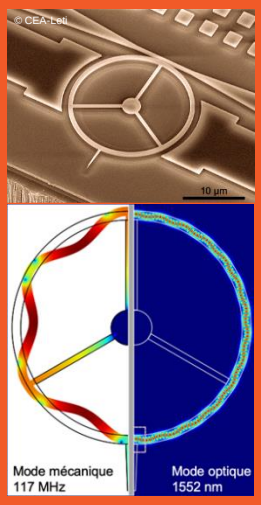


GUIDO RADEMAKER

ADVANCED METROLOGY FOR MULTIPLE ELECTRON BEAM LITHOGRAPHY

Université Grenoble Alpes (France)

To overcome throughput limitations of electron beam lithography, Mapper Lithography designed a machine that can expose with up to 649,740 parallel Gaussian electron beams. In the exposure process, the substrate is divided into 2.2-µm-narrow stripes with a 200 nm overlap. Several parameters need to be controlled: the critical dimensions of the features in the individual stripes; the stitching between the stripes; and the overlay with respect to a previous layer. In this thesis, different optical metrology techniques are explored. Six novel targets for an image based overlay have been developed to measure in-stripe overlay and stripe-to-stripe stitching and are evaluated by total measurement uncertainty (TMU) and measurement time. Scatterometry by spectroscopic reflectometry allows for measurement of non-uniform gratings using an effective critical dimension concept, resulting in a total measurement uncertainty metric down to 0.41 nm (3σ). Stitching can be measured by cross-resonant bow-tie antennae, consisting of four triangles straddling the stitching boundary. Simulations for three different stacks show that the DX and DY stitching errors can be reconstructed independently.

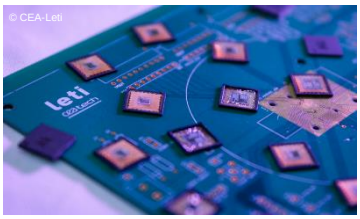


MAXIME HERMOUET

RESONANT OPTOMECHANICAL SILICON MICRODISKS FOR BIOLOGICAL DETECTION IN LIQUID MEDIUM

Université Grenoble Alpes (France)

Early detection of disease biomarkers such as cancer represents a major interest in the treatment process. Indeed, an eraly stage diagnosis considerably increases the chance of successful completion of the treatment. Practically, tools allowing the rapid detection of tiny amount of biological compounds (antibodies, proteins, DNA...) in real samples such as blood or serum are needed. Over the last years, the advances and progresses of micro and nanofabrication techniques have allowed the development of Micro-Nano Electro Mechanical Systems (M/NEMS) in various fields of application including mass sensing. Thus, nano mass sensors reaching resolutions down to the yocotgram level (10-24 g), the equivalent of a single proton have been demonstrated. Such resolution limit would theoretically allow these sensors to be used as potential biosensors. These results were nonetheless obtained in vacuum conditions which is incompatible with the biological world. Immersed in fluid, the performance of traditional M/NEMS are drastically degraded mostly due to the large viscous damping. A new type of object in the form of optomechanical microdisks resonators have recently emerged demonstrating a huge potential for sensing in liquid. While M/NEMS classical electrical or optical transduction methods become very challenging in liquid, the astonishing sensitivity of the optomechanical transduction overcomes this major issue. In this context, this thesis work aims at developing a biosensor based on silicon optomechanical microdisks resonators for biosensing in liquid. Design, fabrication along with the complete characterization of theses devices is described. A proof-of-concept of T5 virus detection at the pM level using these microdisks is presented.

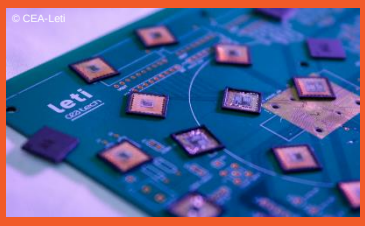


THOMAS LORIN

CONTRIBUTION TO UNDERSTANDING AND REDUCING THE EFFECT OF CURRENT COLLAPSE IN HEMTS AND DIODES BASED ON ALGAN / GAN HETEROJUNCTION ON SI SUBSTRATE FOR POWER APPLICATIONS

Université Grenoble Alpes (France)

The aim of this thesis is to study and reduce the "current collapse" effect in AlGaN/GaN HEMTs and diodes on Si substrate for power electronics. This effect is a degradation that appears after a high voltage stress, related to traps and leading to a degradation of devices ON state characteristics. A part of this work was to localize and to identify these traps. First, a state-of-the-art setup dedicated to the measurement of the relaxation of GaN diodes has been realized. Also, a study has been performed around the cathode field-plate environment and the related degradation. It enabled us to identify passivation and buffer related traps using appropriate electrical characterization on test structures and diodes. Another part of this work consisted to study the buffer related degradation and to improve the device performance by using appropriate buffer engineering. A buried layer showed a good behavior, generating holes that could compensate the negative charge of carbon related deep traps. We also worked on the effect of the ohmic contact integration and the use of a different epitaxial equipment on the charge distribution in the buffer. Using these information as well as TCAD simulations, the mechanisms leading to the "current collapse" effect are better understood and some recommendations to reduce this effect were proposed.

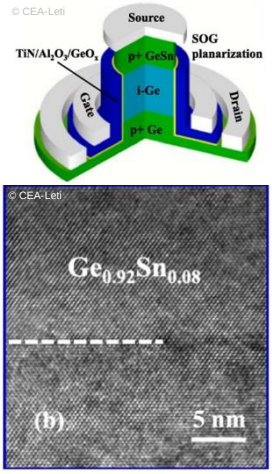


PIERRICK MORIN

STUDY OF THE PROPERTIES OF SOLID ELECTROLYTES AND INTERFACES IN ALL-SOLID MICROBATTERIES: CASE OF LIPON AND SULFUR ELECTROLYTES

Université Grenoble Alpes (France)

The link between the structure and the electrochemicalproperties of thin-film electrolytes and the interface formed with the cathode material LiCoO2 has been intensively studied by coupling Electrochemical Impedance Spectroscopy (EIS) and X-rayPhotoelectron Spectroscopy (XPS). Nitrogen incorporation into LiPON, reference solid-state electrolyte for microbatteries, is characterized by the formation of lithium and oxygen vacancies increasing the lithium ions transport. A sulfide based thin film electrolyte called LiPOS has been developed by radiofrequency sputtering, with the incorporation of sulfur into the initial Li3PO4 structure. The solid/solid interface between LiPON and LiCoO2 is characterized by a partial reduction of cobalt and oxidation of LiPON, which is in all probability responsible of the increase of the charge transfer resistance between the two materials.



MARION VANSTRAATEN

SYNTHESIS OF POLY(METHACRYLATES) THIN FILMS BY ICVD: FROM GROWTH MECHANISM TO REVERSIBLE-DEACTIVATION RADICAL POLYMERIZATION

Université Claude Bernard, Lyon (France)

Recent progress in micro and nanotechnologies require the development of new synthesis process for various material thin films. Polymers, thanks to their properties, are very interesting for fields like microelectronic or biomedical. To respond to this need, many Chemical Vapor Deposition (CVD) technologies are studied. This work focuses on a new method called initiated Chemical Vapor Deposition (iCVD). This deposition method gives many advantages such as its soft operational conditions (solvent free, low temperature), versatility and conformity. In order to improve the understanding of synthesis mechanism in iCVD, the first part of this work is about the poly(methacrylates) thin films growth kinetic. The study reveals a two-regime growth kinetics. A model for the growth mechanism based on the microscopic and macroscopic analysis of thin layers from the two regimes is proposed. It appears than iCVD is a deposition method that can allow fast filling of nanometrics pores with polymer Moreover, to have a better control on polymer synthesized by iCVD (molecular weight, macromolecular architecture), the possibility to used a Reversible-Deactivation Radical Polymerization (RDRP) method with iCVD process is discussed. The last part of this work concerns the use of Reversible Addition Fragmentation chain Transfer (RAFT) polymerization with the iCVD process thanks to silicon samples pre-functionalized with RAFT agent

EMILIE PROVOST

ULTRA-SELECTIVE ETCHINGS OF DIELECTRICS WITH REMOTE PLASMA FOR USE IN MICROELECTRONICS

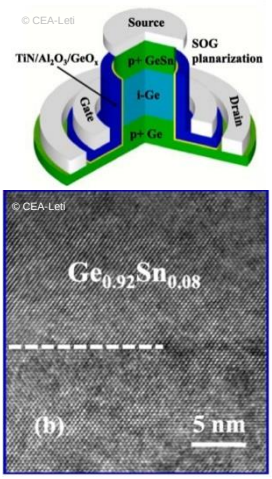
Université Grenoble Alpes (France)

The Moore's Law proposed in 1965 ran out of steam in the 2000s. Since 2016, the microelectronics industry follows the « More-than-Moore » Law, with optimizations underway to meet market's needs. The remote plasma etching studies carried out within the frame of this PhD thesis will be of use for the fabrication of « More-than-Moore » devices. The use of new materials, 3D integration, functionalization and the optimization of new structures require intensive R&D efforts. The appearance of new etching patterns which are deeper and more complex, with nanometer-scale constraints (etch stop layers, for instance), is problematic. Damages coming from ion bombardement and, on patterned wafers, loading effects, make the use of less intrusive etching processes mandatory. Plasmas are generated, in remote plasma reactors (CDE), in a cavity separated from the etching chamber itself. The deleterious impact of ion bombardement, photon and loading effects then is mitigated.

We focused, during the current PhD thesis, on remote plasma etching in a FrontierTM tool. Selective etching processes were optimized and characterized, the aim being to improve the fabrication of nanostructures in microelectronics. We notably focused on the selective etching of dielectrics present in the CDTI trenches of imagers which are currently developed by STMicroelectronics. The optimization of such processes required an in-depth understanding of tool parameters. We thus used various characterization techniques, be it for the gaseous phase or the surface of materials being etched. The impact of tool settings on competing chemical reactions happening on the surface, with a major impact of temperature, was evidenced.

Two kinds of processes were optimized:

- The selective etching of Si_3N_4 versus SiO_2 in high aspect ratio structures ;
- The selective isotropic etching of Si and poly-Si against the double SiO_2 shell lining the trenches.



MAROUANE MASTARI

GROWTH AND CHARACTERIZATION OF SIGE ALLOYS ON NANOMETRIC STRUCTURES FOR MICROELECTRONIC APPLICATIONS

Université Grenoble Alpes (France)

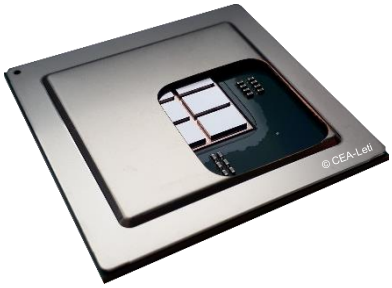
Nano-heteroepitaxy is a promising approach for the growth of high quality, thin and fully strain relaxed SiGe layers (for strained Si devices). In this PhD, an integration scheme based on diblock copolymer patterning was used to fabricate nanometer-sized templates, on which SiGe nano-heteroepitaxy was explored using a 300 mm industrial Reduced Pressure-Chemical Vapor Deposition tool. Si0.75Ge0.25 nano-heteroepitaxy on Si and Si0.75Ge0.25 nano-pillars were first studied. Results showed highly selective and uniform processes based on a chlorinated chemistry for the epitaxial growth of 20 nm high Si and Si0.75Ge0.25 nano-pillars. Smooth surfaces and full strain relaxation were obtained in the 650-700°C range for 200 nm thick Si0.75Ge0.25 layers grown on both types of nano-pillars. However, planar defects were identified as occurring during the coalescence process. Therefore, Si0.75Ge0.25 nano-pillars coalescence was investigated. Various integration schemes were designed in order to measure the impact of pitch, the use of a nano-template during coalescence and the nature of the masking material itself. Results showed more flexibility in terms of surface preparation with higher pitch size nano-templates. Removal of the nano-template did not improve the relaxation of coalesced layers. The nano-heteroepitaxy approach was extended to pure Ge. Results showed a highly selective and uniform process for the epitaxial growth of Ge nano-pillars at 600°C. A degraded surface morphology, with otherwise similar structural properties, were obtained for 2D Ge layers grown on Ge nano-pillars compared with growth on bulk Si. Usual coalescence related defects were once again found.

ADELINE LALLART

ULTRA CLEANLINESS : MICRODROPLETS WITH NANOPARTICLES

Université Grenoble Alpes (France)

With the evolution of microelectronics and the miniaturization of the various components at the nanoscale, the size of the critical particles to be removed during the manufacturing process has been drastically reduced. Indeed, this critical size is currently of the order of 10 nm. Cleaning processes must therefore be able to remove these particles without surfaces damage. In order to answer this challenge, two methods are studied in this work: the use of a spray and the joint application of a polymer layer and a spray.The spray has been used for many years in the microelectronics field. However, the mechanism of particles detachment by this method is still not fully understond. The purpose of this study is to better understand it. Thus, different parameters will be studied leading to the development of a detachment model, showing new variables related to the cleaning process, contamination (nature and particle size) or the storage conditions of surfaces. For its part, the process by using a combination of polymer layer and spray is in full development, but little information is available today. Nevertheless, early studies have demonstrated its ability to clean surfaces with patterns and its effectiveness regardless of the size of the contamination. In this work, different methods of the polymer layer removal will be compared as well as some physicochemical properties specific to it. The objective is to detect key parameters influencing particle removal and to propose a premise of elucidation of the physical mechanisms involved.



ANTHONY CIBIE

INNOVATIVE SUBSTRATES FOR GAN-BASED POWER COMPONENTS

Université Grenoble Alpes (France)

New materials such as gallium nitride (GaN) emerge as promising candidates for power electronics. The current trend is to fabricate the AlGaN/GaN power devices directly on (111) silicon substrates. It makes the expitaxy of the GaN challenging and affects the device performances. In this work, we focus on substrate approaches to solve these problems. A transfer process was developed to replace the silicon substrate by another material to enhance electrical performances of the devices. Especially, GaN devices were transferred on copper substrates without electrical degradation. Electrical and thermal characterizations were performed to study the impact of the transfer. This work offers a first approach on the transfer of GaN devices from 8 or even 12 inches silicon substrates.

JORIS JOURDON

HYBRID BONDING 3D INTEGRATION: CHALLENGES OF THE INTERCONNECTION PITCH REDUCTION

Université de Bordeaux (France)

With the beginning of the 4th industrial revolution and the Internet of Things, the number of integrated circuits in electronic devices increases. Since Moore's law becomes harder to keep up with, 3D integration is an alternative to produce multi-function chips with small form factor. Hybrid bonding enables a highly robust wafer-to-wafer assembly with a density of 106 interconnects/cm2. For these reasons, this technology is of special interest for image sensors. A pitch reduction down to 1.44 µm would enable a density of interconnects fifty times higher and the design of more performant architectures. However, the effects of such modification on the bonding mechanism, electrical properties and the robustness of interconnects remain unknown. This work aims to validate a Cu-SiO2 hybrid bonding integration with a pitch of 1.44 µm. For this study, electrical measurements and accelerated aging tests are performed on dedicated test vehicles with various pitches. A thorough morphological characterization of bonding pads with different sizes allowed the identification of voids and Cu2O nodules at Cu/Cu interface, which indicates a common bonding mechanism. A new method based on electrical measurements and finite element method simulation was developed in order to estimate contact resistivity. It appears that defects at Cu/Cu interface do not increase the resistance of interconnects. Test structures were specially designed to monitor copper diffusion at bonding interface by making compatible chemical and electrical analysis with hybrid bonding integration. Various conditions of bonding and passivation annealings were tested in order to lower the thermal budget of the bonding annealing and assure the compatibility of hybrid bonding process with the whole stack. The pitch limitation was determined thanks to the study of interconnect resistance sensitivity to wafer-to-wafer misalignment. This deep comprehension of effects related to pitch shrinkage and technological process will be valuable to create new architecture.

GABRIELLE ASPAR

3D PRINTING OF POLYMERS APPLIED TO MICROELECTONICS' PACKAGING

Université Grenoble Alpes (France)

In order to answer to industrial requirements and to withstand environment and functioning stresses, electronic components have to be packaged. State of the art of packaging technologies, such as lid sealing, brazing and molding, usually presents shape limitations, material issues and significant cost impact. These have to be specified at the beginning of the product design in order to fit with the whole package and assembly processes, without decreasing the device performances. A new approach used to build a specific packaging allowing flexibility, simplicity and cost competitiveness is presented. Using the polymer additive manufacturing (3D printing) we propose to build customized structures and packages perfectly fitting with component dimensions and specifications. This simplifies the packaging process by merging the steps of package manufacturing, die encapsulation and sealing. Moreover, it permits to easily package and encapsulate components off-the-shelf. In order to validate the feasibility of direct packaging by additive manufacturing, this study focused on understanding the physical and chemical adhesion mechanisms (mechanics, chemistry, etc.) involved between an ABS polymer printed by additive manufacturing and a substrate. Several research axes have been developed: (i) The choice of additive manufacturing process, based on the adhesion of the printed polymer on the substrate and the resolution of the process leading to the selection of the stereolithography process (based on polymerization of specifics UV-reactive resins). (ii) The study of adhesion mechanisms between an ABS polymer and a substrate based on materials database and chemico-physical. (iii) The realization of an operational prototype, based on the direct encapsulation of a chip with a conductive routing and electrical interconnections. This axis allowed us to validate the compatibility of 3D printing encapsulation with an electronic component.

In conclusion, our study demonstrates that the encapsulation of silicon-based microelectronic devices can be achieved by new techniques, including additive manufacturing.

ADRIEN MORARD

MINIATURIZATION AND RELIABILITY OF COPPER PILLAR INTERCONNECTIONS IN SYSTEM IN PACKAGE (SIP) ASSEMBLIES FOR AERONAUTICAL APPLICATIONS

The motivations of this study, in the field of aeronautics, defense and space are twofold, the first is to pursue the miniaturization of the electronics using 3D packaging approaches to gain a factor of 10 in integration density compared to a conventional 2D technology, the second is to improve the system in package reliability.

First this work was devoted to the design and the fabrication of a complete test vehicle composed by a daisy chain silicon chip made in the CEA-LETI silicon platform flipchiped on an organic substrate using copper pillars micro-bumps technology as interconnections.

In a second part we studied the flip chip interconnects behaviour when submitted to thermal cycles. The impact of different design and assembly parameters on the reliability of such assemblies were studied. The main findings were that the chip size should be limited to around 4 mm and that the presence of the underfill is the primary factor impacting the reliability during thermal cycling, the geometry of the copper pillars being on second order influence. Failures analysis during thermal cycles has then been studied by analysing the copper pillar interconnections with micro-sections and SEM with EBSD imaging. Thickness evolution in intermetallic phases, cracking in the solder as well as grain size evolution and recrystallization phenomena were analysed with respect to the different configurations.

In parallel, thermo-mechanical analysis by finite element modeling was performed to extract values of plastic strain energy per cycle and predict the failure mechanisms and the number of cycles to failure using Darveaux law. Correlation with the experimental trials proved the validity of this finite element model and the most critical parameters acting on thermal reliability were confirmed by the model.

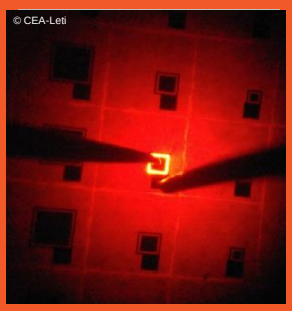
Finally, this work open the way for our industrial partner to initiate the conception of electronics modules based on SIP architecture by defining preliminary design rules and technological guide lines that can be used in their future systems.

IMED JANI

TEST AND CHARACTERIZATION OF INTERCONNECTIONS FOR HIGH DENSITY 3D INTEGRATION

Université Grenoble Alpes (France)

The integration of multiple chips in a 3D stack serves as another path to move forward in the more-than-Moore domain. 3D integration technology consists in interconnecting the integrated circuits in three dimensions using inter-die interconnects (µ-bumps or Cu-Cu interconnects) and Through Silicon Vias (TSV). This changeover from horizontal to vertical interconnection is very promising in terms of speed and overall performances (RC delay, power consumption and form factor). On the other side, for technology development of 3D integration before the production of the 300 mm wafers with all FEOL and BEOL layers, several short-loops must been carried out to enable incremental characterization and structural test of 3D interconnects in order to evaluate the electrical performances (R, L, C …). On the other hand, the test of application circuits consists in adding testability features (Boundary-Scan-Cells (BSCs), Built-In-Self-Test (BIST) and scan chains …) for functional test of the hardware product design (including the different stacked dies and the 3D interconnections). The added Design-For-Test (DFT) architecture makes it easier to develop and apply manufacturing tests to the designed hardware. Compared to µ-bumps, Cu-Cu hybrid bonding provides an alternative for future scaling below 10 µm pitch with improved physical properties but that generates new challenges for test and characterization; the smaller the Cu pad size, the more the fabrication and bonding defects have an important impact on yield and performance. Defects such as bonding misalignment, micro-voids and contact defects at the copper surface, can affect the electrical characteristics and the lifetime of 3D-IC considerably. Moreover, test infrastructure insertion for HD 3D-ICs presents new challenges because of the high interconnects density and the area cost for test features. Hence, in this thesis work, an innovative misalignment test structure has been developed and implemented in a short-loop way. The proposed approach allows to measure accurately bonding misalignment, know the misalignment direction and estimate the contact resistance. Afterwards, a theoretical study has been performed to define the most optimized DFT infrastructure for a given technology node.

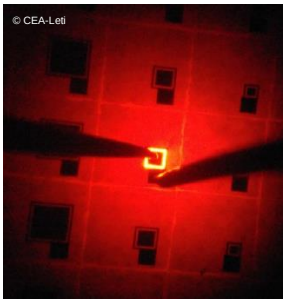


RAMI MANTACH

GROWTH OF SEMI POLAR GAN (10-11) ON SILICON ON INSULATOR SUBSTRATE SOI

Université Côte d'Azur (France)

The epitaxial growth of III-N semiconductors in non-or semi-polar orientations avoids the effects associated with the existence of internal fields in GaN-based hetero-structures usually epitaxy in the c-direction. This thesis work looks at ways to optimize the crystalline structure of the epitaxial layers in semi polar directions <10-11> on silicon substrates disoriented by 7 ° with respect to the direction <001>. Proper structuring of these substrates of particular orientation makes it possible to reveal facets inclined <111> on which the GaN epitaxies in the direction c. The number of emergent dislocations, created at nucleation, is then directly proportional to the surface of these facets of Si <111>. Reducing the density of dislocations to low levels as obtained on sapphire substrate requires reducing the size of the nucleation facets. The original solution we have developed is to use SOI substrates for which the upper layer of Si is disoriented by 7 ° with respect to the <001> direction and is as thin as possible. Optimization of both the substrate structuring process and the growth stages allowed us to reduce the emerging dislocation density in GaN <10-11> semipolar layers by a factor of 10 compared to state of the art on Si substrate. The residual stress, in tension when on Si, is here almost zero. Reduction of the nucleation surface has also resulted in the elimination of the "melt-back etching" phenomenon, usually impossible to prevent for semi-polar epitaxial layers on Si substrates. The so-called "Aspect Ratio Trapping", implemented for cubic symmetry materials is directly applicable to the case of semi-polar nitrides (which are of hexagonal symmetry) when epitaxied on SOI, causing another factor 10 in the reduction of the density of dislocations. Lastly, we used these semi-polar low-density dislocation layers to make metamorphic InGaN layers. Stress relaxation allows for greater incorporation of indium for the purpose of producing longer wavelength diodes. In this sense, we demonstrate the realization of the first semi-polar LED made on SOI substrates.

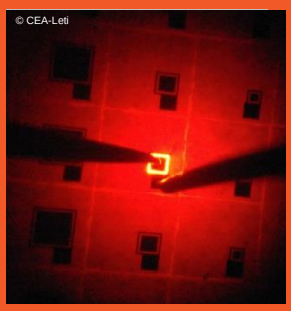


VICTOR FAN ARCARA

TUNNEL JUNCTIONS IN NITRIDE HETEROSTRUCTURES FOR OPTOELECTRONIC APPLICATIONS

Université Côte d'Azur (France)

Tunnel junctions provide an alternative solution to issues that limit the efficiency of ultraviolet light emitting diodes, such as the high resistivity of p-doped AlGaN layers and the resulting poor hole injection. The objective for this thesis is the optimization of GaN and AlGaN based tunnel junction LED structures and their structural and optoelectronic characterization. The growth of a TJ LED entirely by MOCVD is industrially appealing, but the p-doped (Al)GaN layers developed by this technique suffer from the repassivation of the Mg acceptors by the hydrogen present in the growth chamber. We have tried and succeeded to minimize this problem by modifying the growth conditions of the tunnel junction. Positive results have been achieved on blue LEDs, in particular with GaN tunnel junctions including an InGaN interlayer that increases its tunnel transparency. However, this all MOCVD process seems difficult to optimize and its extension to AlGaN materials difficult. Thanks to a hybrid MOCVD+MBE growth approach, p-doped GaN and AlGaN layers can be obtained with active Mg acceptors while taking advantage of high quality active regions provided by MOCVD. With a GaN-based hybrid TJ, we have been able to obtain, with both Si and Ge, higher levels of n++ doping than those of the MOCVD TJs, thus significantly reducing the operating voltage of the devices. The strong Ge doping of the GaN layers allowed us to obtain electron densities of the order of $5x10^{20}cm^{-3}$ with state-of-the-art mobilities and resistivities, without introducing a strong constraint in the network. In the second part of this work, we have developed AlGaN-based TJs doped with Ge on UV LEDs by gradually changing their Al concentration up to a value of 70%. In the UV range, the TJs become of paramount importance by increasing the injection efficiency without compromising light extraction. High levels of Ge doping have been obtained leading to thin junctions as shown by electronic holography. Even if the voltage drops introduced by the use of TJs remain significant (a few volts), the injection of out-of-equilibrium holes allows for a significant increase of the injection efficiency in the LED leading to a strong increase of the quantum efficiency of these devices.

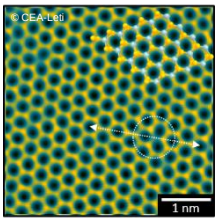


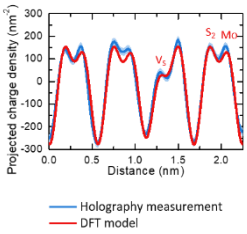
PIERRE GUINEDOR

LOW-FREQUENCY NOISES AND DEEP LEVELS STUDY IN COOLED INFRARED DETECTORS

Université Grenoble Alpes (France)

The current trend in the infrared market is to address HOT (High Operating Temperature) applications, which exacerbates the impact of low frequency noises (Random Telegraph Signal (RTS) and 1/f) and then degrades the image quality of cooled HgCdTe detectors. In this work, the focus was laid on the analysis of defects at the root of these noises to, eventually, improve the image quality. Two paths are introduced: the electro-optical characterization of low frequency noises and the spectroscopic characterization of electrically active defects in the material. First generalities on infrared detection and spectroscopic techniques used in this work are described. Then low frequency noises characterizations are realized to refine the comprehension of their physical mechanisms. Finally DLTS (Deep Level Transient Spectroscopy) studies are performed on two technologies for SWIR (Short Wave InfraRed, λc = 2.5 µm) and MWIR blue ((Mid Wave Infrared, λc = 4.2 µm) bands in order to get to the root of low frequency noises.





ERIC LANGER

ADVANCED CHEMICAL CHARACTERIZATION OF ORGANIC ELECTRONIC MATERIALS AND DEVICES

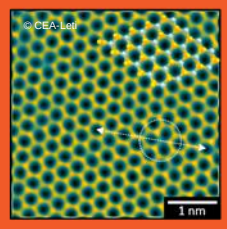
University of Namur (Belgium)

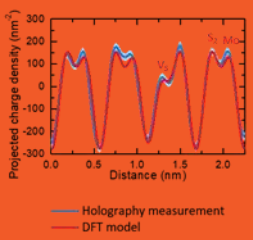
This thesis is directed towards the development of novel characterization protocols to probe the chemical composition at the nano scale of devices that are used in organic electronics. This enables the investigation of chemical processes like the degradation of molecules or dopant migration that occur during device operation as well as the detection of contaminants. This information is much needed to improve the lifetime and the efficiency of the device. Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS) and X-ray Photoelectron Spectroscopy (XPS) are two commonly used techniques to study the chemistry of inorganic and organic materials. Combined with a sputter gun, depth profiling can be performed to gain three-dimensional chemical reconstructions of the sample. However, modern organic electronic devices like OLEDs represent a real challenge for chemical depth profiling because of film thicknesses of only a few nanometers, molecules with very similar structure that can be damaged during analysis, and inorganic-organic interfaces that are problematic to sputter through because of substantial differences in sputter rates.

To overcome these obstacles, single layers and bilayers are studied as simplified systems to develop reliable and precise characterization protocols with minimal analysis induced damage to the organic materials. The combination of ToF-SIMS and XPS is key in this part.

Then, these protocols are adapted to study complete OLED devices. Electrically aged devices are compared to non-aged devices to study the degradation of the molecules.

Finally a new sample preparation technique with the creation of extremely shallow beveled craters is explored for an even gentler analysis. This technique is very promising and could lead to an improvement of the characterization protocol in the future.





MAIGLID-ANDREINA MORENO VILLAVICIENCIO

DEVELOPMENT OF 3D HIGH-RESOLUTION IMAGING OF COMPLEX DEVICES BY THE CORRELATION OF TOF-SIMS AND AFM

University of Lyon (France)

The continuous miniaturization and complexity of devices have pushed existing nano-characterization techniques to their limits. The correlation of techniques has then become an attractive solution to keep providing precise and accurate characterization. With the aim of overcoming the existing barriers for the 3D high-resolution imaging at the nanoscale, we have focused our research on creating a protocol to combine time-of-flight secondary ion mass spectrometry (ToF-SIMS) with atomic force microscopy (AFM). This combination permits the correlation of the composition in 3-dimensions with the maps of topography and other local properties provided by the AFM. Three main results are achieved through this methodology: a topography-corrected 3D ToF-SIMS data set, maps of local sputter rate where the effect of roughness and vertical interfaces are seen and overlays of the ToF-SIMS and AFM advanced information.

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