

COMMITTED TO INNOVATION, CEA-Leti CREATES DIFFERENTIATING SOLUTIONS WITH ITS PARTNERS

EA-Leti is a technology research institute of France's CEA and a global leader in miniaturization technologies enabling smart, energy-efficient, and secure solutions for industry. Founded in 1967, CEA-Leti conducts pioneering micro and nanotechnology research and custom develops differentiating application-specific solutions for global companies, SMEs, and startups. CEA-Leti

tackles critical challenges in healthcare, energy, and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pilot production lines to scale new technologies up. With a staff of more than

1,900, a portfolio of 3,140 patents, 10,000 sq. meters cleanrooms, and a rigorous IP policy, CEA-Leti has launched 69 startups and is a member of France's Carnot research network. based in Grenoble, France, the institute has offices in Silicon Valley and Tokyo.

Follow us at www.leti-cea.com and @CEA Leti.

Technological expertise

CEA (the French Alternative Energies and Atomic Energy Commission) is a leading global research organization whose mission is to transfer new scientific knowledge and innovations to industry. With a focus on electronics and integrated systems from micro to nano, CEA innovations make businesses in transportation, health, safety, and telecommunications more competitive by helping them develop high-performance, differentiating products and novel solutions.

www.cea.fr/english



CEA-Leti at a glance

450

publications per year

ISO 9001 certified since 2000

114 European projects Founded in

1967

Based in

France (Grenoble) with offices in the

US (San Francisco) and Japan (Tokyo)

300 industrial partners

1,904 researchers

3,140 patents in portfolio

10,000

sq. meters of cleanrooms 100-200-300 mm wafers

69

startups created

Within CEA Tech and Leti, silicon technologies and components research activities are shared between two divisions gathering together around 600 researchers:

The Technology Platform Division carries out innovative process engineering, materials research and development as well as advanced nano-characterization. It operates 24/6 year round, and has $1100 \, \text{m}^2$ of state-of-the-art cleanroom space divided into four different technology platforms.

The Silicon Components Division carries out research on nanoelectronics and heterogeneous integration on silicon and is focusing on two mains areas: on-going shrinking of CMOS devices to extend Moore's Law for faster, less-expensive computing power, and the integration of new capabilities into CMOS, such as sensors, power devices, imaging technology, and new types of memory, to enable new applications.

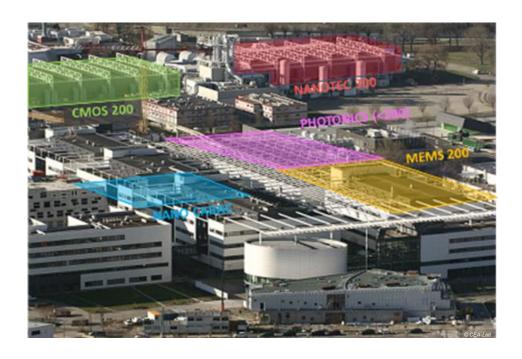
This booklet contains 46 one-page research summaries covering advances in the focus areas of our Silicon Devices and Technologies Divisions, highlighting new results obtained during the year 2020.

Technological Platforms

The silicon divisions operate 11000 m² of state-of-the-art cleanroom space divided into three platforms, gathering 700 process tools and a combined staff of more than 520; they run industry-like operations, 24 hours a day, 6 days a week, all year round.

- 1 The Nanotech200&300 platform provides 200mm and 300mm CMOS wafer processing, which can be applied to both semiconductor and microsystem devices.
- 2 The MEMS200 platform produces non-CMOS Micro-ElectroMechanical Systems (MEMS)
 - Both platforms are focused on the More than Moore initiative to develop new semiconductor capabilities. An innovative cleanroom shuttle system links the two platforms to add process flexibility and faster processing.
- 3 The 3D Integration platform aims to integrate various microelectronics objects together in order to juxtapose complementary functions, such as sensing, storing, processing, actuation, communication and energy scavenging. This provides advanced system solutions in three dimensions. This line is open to our customers for prototyping through the Open3D service.
- 4 The fourth platform that was recently added is dedicated to photonics. It covers conception, III-V and II-VI semiconductor technology fabrication and packaging capability. Applications as diverse as lighting, micro-screens, visible and infrared detectors and devices for astrophysics ...

All research carried out in our cleanrooms benefits from the Nano-Characterization Platform, which is located on the MINATEC campus. This platform, unique in Europe, covers eight domains of competencies, including electron microscopy, X-ray diffraction, ion beam analysis, optics, scanning probe, surface analysis and sample preparation, magnetic resonance.



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FOREWORD



Laurent Clavelier,
Head of the Technology
Platform Division

Although the year 2020 will certainly be remembered for the sanitary crisis, it was above all the year in which we had to adapt to a unique new context.

The scientific activity of the Technology Platform Division was inevitably impacted by the constraints imposed by the pandemic and our capacity to adapt was one of our best assets in maintaining our scientific excellence.

The confinement, for example, was the opportunity to boost our scientific output both in terms of quantity with 125 scientific articles in 2020 compared to 90-100 on average whilst maintaining the number of conference proceedings constant compared to previous years, but also in quality with an improvement in our average impact factor (3.9 vs 3.5 in 2019).

Of course, these good results should not mask the difficulties encountered, especially those experienced by our PhD students, the majority of whom had their contracts extended from 2 to 4 months to take into account the period during which they were unable to access the CEA laboratories.

Without trying to be exhaustive, this editorial is also the opportunity to highlight some of the excellent results obtained in 2020 such as those in the domain of resistive memories based on chalcogenides and hafnium oxide that underline our position as a world leader in the domain of embedded artificial intelligence, our work on the growth of III-N materials and their advanced characterization (correlation of atom probe tomography, TEM; CL/PL), or the recent progress in 3D technology where innovative low temperature growth processes have been developed for sequential 3D applications and film transfer techniques compatible with 5 μm interconnect pitch for 3D stacking technology.

The last point that I wish to address in this editorial is the link between research and engineering activities on the platform. Since late 2019 we have held regular meetings to ensure a strong link between these two activities to ensure that our scientific research feeds into our engineering "tool box", benefiting our industrial partners, and thus fulfilling our mission statement "from research to industry". For example, since 2020, certain aspects of our research on 2D materials found an application with STMicroelectronics for RF components. This is one of many illustrations of the continuum – research – engineering – maturation and industrial transfer that is our raison d'être

I hope you will enjoy reading the 2020 Silicon Technologies and Components scientific report.

Laurent CLAVELIER

FOREWORD



Olivier Faynot, Head of Silicon Components Division

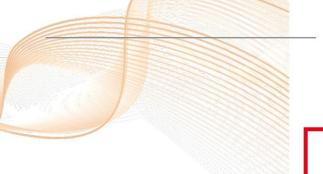
Dear Reader,

The developments of energy efficient silicon technologies and solutions is the priority of the Silicon Components Division, in order to provide answers to many societal issues such as mobility, communications with Smart, green, efficient transportations, secure and energy efficient communications. The coupling of technology, simulation, characterization, modeling, design environment and circuit design is essential to understand the behavior and to highlight the benefit of our solutions.

In spite of the 2020 COVID crisis, many significant achievements have been demonstrated this year and we have published more than 160 papers, with significant contributions to the most relevant conferences. Let me now highlight a few of our main successful achievements:

- Multilevel resistive-RAM cells have been demonstrated for Neuromorphic applications. This opens the way for denser and more efficient Neural networks.
- Silicon based quantum devices have been demonstrated and the flow has been transferred into a more robust flow using immersion lithography. Wafers are about to be finished and electrical tests will be done soon.
- First RF characterizations of GaN/Si transistors with optimized epitaxial layer have been performed and the first results are encouraging.
- First demonstration of SAW filters integrated on 200mm POI wafers, with similar results compared to 100 and 150mm wafers.

I would like to thank all the teams involved in those achievements and I hope you will enjoy reading the overview.



FOREWORD





Jean-Charles Barbé and Jean-Paul Barnes Chief Scientists for the Silicon Components Division and the Technology Platforms Division

We are delighted to share with you our eleventh Silicon Technologies and Components Annual Scientific Research Report. This report contains 46 one-page research highlights from the Silicon Components and Technology Platforms Divisions that was published over the course of the year 2020.

2020 was an exceptional year by many standards and it illustrates the resilience and capability of the Silicon Divisions to meet new challenges. This is particularly reflected in the number and quality of our scientific publications in 2020. We are able to maintain the same level of publications as in previous years, with a greater number of journal publications making up for the limited opportunities for conference papers due to the cancellation of many events. We note a net increase in number of articles in high impact journals with 17 publications in journals with an impact factor greater than ten compared to 10 in 2019. A few examples amongst these illustrate some of our major topics that are currently being developed.

Again this year, our international collaborative contributions to the rapid progress in the field of Silicon based Quantum technology has been published in Nature Comm., Nature Nanotech., Phys. Rev. X, Appl. Phys Rev and NANO Letters covering aspects from technological developments to design through to cryogenic electronics.

An article in Nature Photonics shows how, in the framework of an international collaboration, our expertise in epitaxy has played an important part in demonstrating ultra-low-threshold continuous-wave and pulsed lasing in tensile-strained GeSn alloys.

Two articles in Advanced Materials demonstrate how we are working to better understand the fundamentals of chalcogenide materials and exploring applications beyond memory devices. These contributions are strengthened by a theoretical collaborative paper on ionic transport paper published in Nature Communications which pave the way for more rational numerical design of materials.

Finally important developments in advanced nanocharacterisation are showcased in two publications in ACS Nano and Advanced Function Materials.

2020 was a difficult and uncertain year for our interns, PhD students and post-doctoral researchers. Despite this they made a significant contribution to our scientific output in 2020 and participated to make the first all-virtual PhD days event a success. Many PhD vivas, initially planned for 2020 were shifted to 2021 due to contract prolongations and will be included in next year's report, so check back soon!

Lastly we would like to express our gratitude not only to the editorial team and all the authors of the 2020 Scientific Report, but also to the entire department staff who contributed to minimize the impact of the pandemic on our research activities. We hope you find this report instructive and that it may nurture the seeds of many future collaborations.

KEY FIGURES



475 researchers

176 Industrial residents

131 PhD students in 2020

13 Post-docs in 2020



11000 m² of cleanrooms 24/6 operation 700 tools



3000 m² Nanocharacterization platform

50 advanced instruments

3 CEA institutes (LETI, LITEN, IRIG) working together



22 Joint Research Agreements with Industry

143 patents filed in 2020

1455 patents in portfolio

405 Scientific communications in 2020

SCIENTIFIC ACTIVITY

Publications

405 publications in 2020 (WoS, SCOPUS, ACM) 170 international conference communications in 2020.

Prize and awards

ECS PRIME 2020, Best Paper Award in SiGe, Ge and related compounds session "Analysis of Sn behavior during Ni/GeSn solid-state reaction by correlated X-ray diffraction, atomic force microscopy, and ex-situ/in-situ transmission electron microscopy". A. Quintero et al.

Best paper of the 2020 Electronics System-Integration Technology Conference (ESTC) "Dieto-Wafer 3D Interconnections Operating at Sub-Kelvin Temperatures for Quantum Computation", C. Thomas et al.

Winners of the 2020 3D InCites Awards as "Research Institute of the Year:

https://www.3dincites.com/2020/02/and-the-winners-of-the-2020-3d-incites-awards-are/

Best paper award "Integrated Variability Measurements of 28nm FDSOI MOSFETs down to 4.2K for Cryogenic CMOS Application", B. Cardoso Paz, et al, 33rd IEEE International Conference on Microelectronic Test Structures (ICMTS), Avril 2020

European Star Award for the project 'REFERENCE' (Grant n° 692477), Mention 'Innovation'

Experts

- 7 International Experts
- 4 Research Directors
- 38 Senior Experts
- 56 Experts
- 27 of them holding an HDR

Scientific committees

- National Research Agency committee.
- Technical Program committees of:

IEEE IEDM, IEEE VLSI Technology and Circuits, IEEE IRPS, IEEE TRANSDUCERS, IEEE IMW, IEEE ECTC. **IEEE** ESTC. **IEEE** ESSDERC/ESSIRC, IEEE SISPAD, IEEE 3DIC, IEEE ISSCC, IEEE IITC, AMC, ICSI/ISTDM, ECS Transactions AIMES, JNTE, AVS, Advanced Lithography, FCMN, EMRS Spring, l'E\PCOS, CIMTEC, MRS spring 2021 (symposium BEOL), Plathinium 2021, RAFALD, MAM-2020, European FIB Network Workshop

Invited editor of:

Special Focus Issue on « Phase-Change And Ovonic Materials » at Wiley-PSS:rrl,

« Phase-change memories: materials science,

technological applications and perspectives » J. Phys. D: Appl. Phys,

Conferences and Workshops organizations

4emes Journées des Spectroscopies d'Electrons (French Workshop on Electron Spectroscopy).

29th Materials for Advanced Metallization 2020 (MAM) Grenoble-2020.

International Collaborations

Forschungs Zentrum Juelich (Germany), Stanford University (USA),

Caltech (USA),

The University of California (USA),

Fraunhofer institutes (Germany),

Università degli Studi di Ferrara (Italy)

University of Cambridge (GB),

Université Catholique de Louvain (Belgium),

University of California at Berkeley (USA),

Politecnico Di Milano (Italy),

Paul Scherrer Institute (Switzerland),

École Polytechnique Fédérale de Lausanne (Switzerland),

ETH - Zürich (Switzerland),

CNR (Italy),

University of Chicago (USA),

Sherbrooke, University (Canada)

NIMS (Japan), SPring-8 Synchrotron (Japan)

University of Southern Denmark

University Cagliari (Italy),

Institute for Technical Physics and Materials

Science (Budapest),

Hungarian Academy of Sciences (Budapest),

Korea University (Seoul)

Centro universitario FEI (Brazil),

University of Tsukuba (Japan),

AIST (Japan),

Herzen University (St Petersburg, Russia).

IMEC, Leuven (Belgium), EMPA, ETH

(Switzerland),

Mons University (Belgium),

University of Surrey (UK)

Université de Liège (Be)

Universitatea Politehnica din Bucuresti (UPB);

National Physical Laboratory, London (UK)

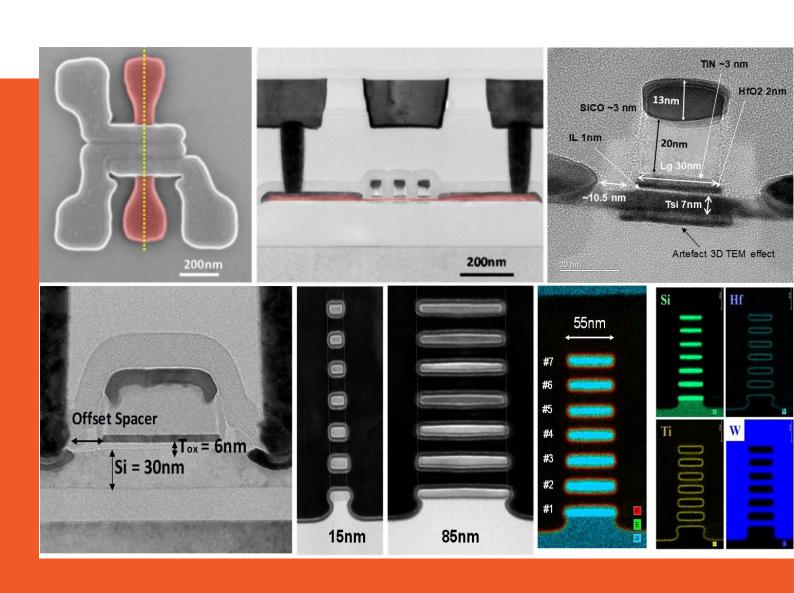
Elettra Synchrotron, Trieste (Italy)

NSLS-II, Brookhaven Nat. Lab. (USA)

Fondazione Bruno Kessler, Trento (Italy)

Physikalisch-Technische Bundesansalt, Berlin, Germany.

Varsaw University, IHPP (Poland)



01

CORE & BEYOND CMOS

- New advances in 3D VLSI integration through the first demonstration of both low temperature CMOS (500°C) and analog FDSOI devices and 28nm FDSOI FEOL & BEOL stability accros yield
- 7-level-stacked nanosheet GAA transistors for high performance computing
- Modelling variability of silicon spin qubits
- Cryo CMOS electronics for quantum computing ICs: electrical characterization and modeling of 28FDSOI technology

New advances in 3D VLSI integration through the first demonstration of both low temperature CMOS (500°C) and analog FDSOI devices and 28nm FDSOI FEOL & BEOL stability across yield

RESEARCH TOPIC:

Low temperature FDSOI transistors, High voltage analog devices, 3D sequential integration, FDSOI devices stability, Yield

AUTHORS:

C. Fenouillet-Beranger, L. Brunet, C. Cavalcante, L. Brevard, 1W-H. Kim, ²X. Federspiel, ³G. Ghibaudo, F. Andrieu, P. Batude

For the first time, the thermal stability of a 28nm FDSOI CMOS technology is evaluated with yield measurements (5Mbit dense SRAM and 1 Million Flip-flops). It is shown that 500°C 2h thermal budget can be applied on a digital 28nm circuit including Cu/ULK BEOL without yield nor reliability degradation. In parallel, the first FDSOI CMOS transistors with Simonocrystalline channel have been fabricated at a temperature below 500°C. Regarding analog devices, we built an original stackable 2.5V device on FDSOI with analog performance comparable to high temperature (HT) reference and passing the PBTI reliability criteria. All these results pave the way for high-performance (HP) digital and analog 3D sequential CMOS integration with the introduction of Cu/ULK BEOL between tiers.

SCIENTIFIC COLLABORATIONS: ¹Samsung electronics, Gyeonggi-do (South Korea); ²STMicroelectonics, Crolles (FR); ³IMEP-LAHC, Grenoble (FR).

Context and Challenges

3D sequential integration becomes more and more attractive for more Moore and more than Moore applications. However, one of the most important challenge is to implement at low temperature (LT≤500°C) HP CMOS digital devices and analog devices for the upper level, without degrading the bottom one previously integrated. The goal of this study is to demonstrate the feasibility of both LT digital and analog FDSOI devices through relevant electrical Figure Of Merit. Finally, 28nm FDSOI transistors stability is studied versus industry yield characterization.

Main Results

The thermal stability of both BEOL Cu/ULK interconnects and FEOL devices upon additional TB has been investigated, with anneal after M8 level. The characterization of Time to Breakdown of BEOL dielectrics show no degradation after 500°C anneal and no degradation of the SRAM yield even at 525°C 2h [1]. FDSOI CMOS transistors with Si-monocrystalline channel have been fabricated below 500°C [2] with HP PMOS and first functional RO (FO1) and LT SRAM bitcells. We built an original stackable 2.5V device on FDSOI enabling to conclude on the feasibility of stacking HV analog devices in 3D VLSI Integration for More-than-Moore applications [3].

Thanks to this first LT 500°C CMOS demonstration and 500°C 2h Cu/ULK BEOL stability, a full 3D sequential Integration with Intermediate BEOL should be demonstrated. The analog LT HV devices can be used for sensor read out operation, paving the way to ultraminiaturized smart sensor arrays.

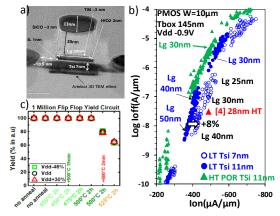


Figure 1: LT digital lon/loff & Yield [1-2]

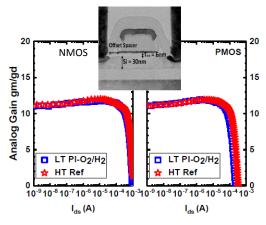


Figure 2: FDSOI analog gain (2.5V) [3]

- C. Cavalcante et al., IEEE Symposium on VLSI Technology, 2020, https://doi.org/10.1109/VLSITechnology18217.2020.9265075
- [2] C. Fenouillet-Beranger et al., IEEE Symposium on VLSI Technology, 2020, https://doi.org/10.1109/VLSITechnology18217.2020.9265092 [3] C. Cavalcante et al., IEEE International Symposium on VLSI-TSA, 2020, https://doi.org/10.1109/VLSI-TSA48913.2020.9203691

7-level-stacked nanosheet GAA transistors for high performance computing



RESEARCH TOPIC:

CMOS, sub-5 nm node, VLSI, Gate-All-Around, Nanosheet, Nanowires

AUTHORS:

B. Previtali, C. Vizioz, J.-M. Hartmann, J. Sturm, C. Perrot, Ph. Rodriguez, A. Grenier, F. Andrieu, and **S. Barraud**.

In this work, CEA-Leti experimentally demonstrates, for the first time, gate-all-around (GAA) nanosheet transistors with a record number of stacked channels. Seven levels stacked nanosheet (NS) GAA transistors fabricated using a replacement metal gate process, inner spacer and self-aligned contacts show an excellent gate controllability with extremely high current drivability (3 mA/µm at VDD = 1 V) and a 3× improvement in drain current over usual 2 levels stacked-NS GAA transistors.

Context and Challenges

Until now, scaling of FinFET (FF) technology has involved smaller fin width with taller fin and smaller fin pitch (FP) in order to maximize the ratio Weff/FP (with Weff defined as the effective channel width). However, further fin width (and FP) reduction with even more current drivability is complex from the processing and variability points of view. This is the reason why Gate-All-Around (GAA) technology is today proposed for sub-5nm nodes. In addition to have a better gate control (vs FF), GAA transistors offer higher DC performance thanks to higher Weff. The wide range of NS width also provides more design flexibility, which is not possible for FF. In order to improve the current performance of GAA transistors, we explored a new performance lever by increasing significantly the Weff/footprint ratio. Increasing the stacked layers and targeting 7-levelsstacked NS increases process complexity, but the beneficial impact of NS effect is significantly improved while keeping a relaxed FP and lower aspect ratio (vs FF) for fin patterning.

Main Results

For the first time, seven levels stacked NS GAA transistors are fabricated using a replacement metal gate process, inner spacer and self-aligned contacts. The backbone of our process flow remains very similar to the one used for FinFET, with nevertheless some extra work on specific modules. The fabrication starts with the epitaxial growth of 150 nm thick Si0.7Ge0.3/Si multilayers (with 7 silicon layers). Thanks to an optimized patterning process, tall and straight (SiGe/Si) fins are fabricated. In fig. 1, we show that a wide range of NS width can be considered (between 15 nm and 85 nm). After that, a challenging etching of SiO2/Poly-Si dummy gates on tall (SiGe/Si) fins is successfully performed. Then, a selective etch of the SiGe layers is performed beforehand to have SiN inner spacers. A lateral growth of in-situ phosphorus-doped Si was carried out to have thick enough S/D. The process then continued with the dummy-gate removal, the release of Si NS, the HfO2/TiN/W deposition and the self-aligned-contacts.

Thanks to the GAA architecture, gate controllability is very

efficient even for wide NS. An excellent immunity to short-channel-effect is demonstrated with a subthreshold slope lower than 70 mV/dec and a DIBL lower than 20 mV/V. In comparison to NS GAA transistors integrating two stacked channels, the seven-channel devices exhibit a threefold improvement in drive current. Thanks to higher Weff/footprint, NS outperform FF transistors with an IODSAT up to 5 mA/µm. This clearly shows the benefit of increasing the number of stacked channels to boost DC performances.

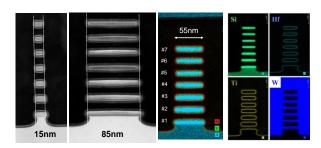


Figure 1: GAA NS FET with 7 stacked Si channels

Perspectives

Further developments are still ongoing in order to improve the performance of GAA transistors. But alternative applications are also considered, such as the co-integration of GAA stacked nanosheet transistors with 3D resistive RAMs.

RELATED PUBLICATIONS:

[1] S. Barraud et al., 2020 IEEE Symposium on VLSI Technology, 2020, https://doi.org/10.1109/VLSITechnology18217.2020.9265025

Modelling variability of silicon spin qubits

RESEARCH TOPIC:

Quantum information, silicon spin qubits, modeling of materials and devices

AUTHORS:

L. Hutin, B. Martinez Diaz, B. Venitucci, J. Li, V. Michal, G. Troncoso Fernández-Bada, S. de Franceschi, M. Vinet, Y.M. Niquet

Modeling is a major challenge for quantum computing in silicon and shall help to design the devices and provide support for the interpretation of the experiments, and for the exploration of the physics of these complex devices. New numerical models were developed to simulate silicon-on-insulator qubits and extract the impact of the different sources of variability on the qubit figures of merit.

SCIENTIFIC COLLABORATIONS: ¹Institut Néel (CNRS)

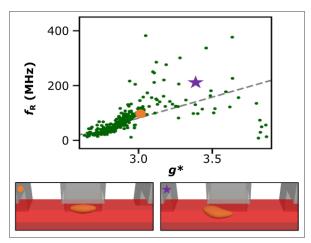
Context and Challenges

Spin qubits in silicon are attracting much interest owing to the very long spin lifetimes and incomparable technological knowhow in this material. The qubit information is stored in the spin of carrier(s) trapped in quantum dots. Silicon-on-Insulator (SOI) is one of the appealing platform to realize such qubits: quantum dots are etched in a thin silicon film on SiO2 and controlled by a set of gates. This interplay between structural and electrostatic confinements allows, in particular, to reduce the number of gates per device. These SOI qubits are compatible with scalable CMOS fabrication and are developed in 1D and 2D topologies.

The implementation of a realistic quantum computing device will require quantum error correction protocols to ensure the protection of the quantum information against noise. This usually comes with a large overhead in qubit number that will imply a large scale integration of MOS devices. Because of this high number of devices and the very small energy scales implied, variability management is a major issue that will drive the choice of future architectures [1].

Main Results

We have numerically simulated how variability would impact some key figures of merit of spin qubits, for instance the gyromagnetic factor, determining the excitation frequency of the qubits at a given magnetic field (Larmor frequency), and the Rabi frequency, determining the qubit control speed [2]. We studied more specifically the impact of the Si/SiO2 interface roughness and the density of interface traps. The study cover the case of hole spin qubits (with a control mediated by the intrinsic spin-orbit interaction) and electron spin qubits (with an artificial spin-orbit interaction induced by a micro-magnet). In both cases, charge disorder is the main source of variability and is significantly larger for hole qubits. The results are Illustrated by the figure below highlighting distribution of Zeeman splittings (É_Z=g*μ_BB) and Rabi frequency f_R for different charge disorders and iso-surfaces of squared wave functions for two different configurations.



Impact of interface traps on hole gubits

Perspectives

Important aspects such has a quantitative description of valley splitting, spin-orbit coupling or paramagnetic defects remain extremely complex to model. In order to address these challenges, the current models should be complemented with advanced ab initio modeling of materials, interfaces and defects. Such calculations, which are "at or beyond the state-ofthe-art", require huge computational facilities, but shall be achievable within the next few years.

RELATED PUBLICATIONS:

[1] M. Vinet et al., Bulletin of the American Physical Society 65 (1), 2020, http://meetings.aps.org/Meeting/MAR20/Session/J17.1 [2] Y. M. Niquet et al., IEEE International Electron Devices Meeting (IEDM), 2020, https://doi.org/10.1109/IEDM13553.2020.9371962

Cryo CMOS electronics for quantum computing ICs: electrical characterization and modeling of 28FDSOI technology



RESEARCH TOPIC:

28nm FDSOI CMOS transistors, cryogenic temperatures characterization, quantum information

AUTHORS:

B. Cardoso Paz, G. Ghibaudo¹, E. Vincent², G. Billiot, M. Vinet, S. de Franceschi, T. Meunier³, F. Gaillard, M. Cassé

28nm FDSOI technology is thoroughly electrically characterized aiming at cryogenic applications. Electrostatics, transport, variability and self-heating are evaluated and compared lowering temperature down to 4.2K. FDSOI versatility is shown over a wide temperature range of operation, as the back gate tuning efficiency is preserved at low temperatures. Insights on back gate bias behavior at room and low temperature are obtained. In particular intersubband scattering have been evidenced and modeled at low temperature, with a possible impact for analog designers. The first statistical results ever published on FDSOI variability at 4.2K, using an addressable matrix of transistors, provide valuable information for future compact modeling and circuit design.

SCIENTIFIC COLLABORATIONS: 1 CNRS IMEP-LAHC, 2 STMicroelectronics, 3 CNRS Institut Néel

Context and Challenges

To design efficient quantum computers, high performance and low power control electronics in the vicinity of the qubits is a need, i.e. with operation temperatures ranging from 4.2K down to well below 1K. FDSOI technology appears as a valuable solution for the co-integration of qubits and control electronics, taking advantage of its threshold voltage tunability allowed by the back bias. So far however, advanced CMOS nodes have not been extensively explored for deep cryogenic operation. Because these aspects are essential for the development of compact models and robust design tools, this work presents extensive electrical characterization and analysis of 28nm FDSOI MOSFETs down to 100mK, with regard to devices electrostatics, variability or thermal effects.

Main Results

We have demonstrated that FDSOI transistors are fully operating down to 100mK, including the ability to tune the threshold voltage with the same efficiency as at room temperature (RT) thanks to the back bias [1]. Improved ON current (from x5.6 on long devices to x1.6 on short NMOS) OFF current (below our equipment accuracy <1fA) and subthreshold slope (as low as 9mv/dec.) contribute to the very good performances of FDSOI technology at cryogenic temperature, as demonstrated in a quantum integrated circuit on a single chip in industrial 28nm FDSOI CMOS technology (https://doi.org/10.1109/ISSCC19947.2020.9063090). Statistics and mismatch analysis were carried out down to 100mK, through an automated measuring system implemented with an on-chip multiplexed matrix arrangement of addressable transistors arranged in matched pairs (see Figure 1) [1,2]. We thus demonstrated for the first time that 28nm FD-SOI outperforms other CMOS technologies at low temperature (LT) in variability and that the latter remains low enough so that its impact could be mitigated for circuit operation at LT. Additional feature appear on the drain current in long channel devices when forward back bias is applied, as the consequence of a discontinuity in the mobility due to intersubband scattering at LT

[3]. This behavior, specific to thin film devices, has to be taken into account into future cryo-CMOS compact models. Low frequency noise (LFN) has also been investigated down to 4.2K; our results have shown that LFN can be well described by the carrier number with correlated mobility fluctuations model

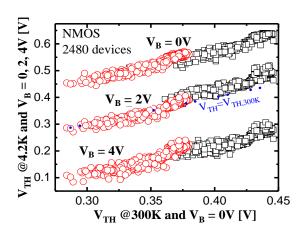


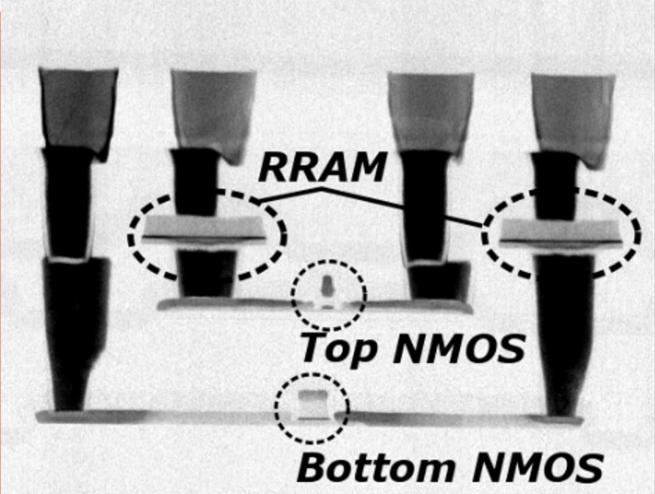
Figure 1: Comparison of VTH at 4.2K and RT.

Perspectives

These results provide a ground for future compact models at LT and the first guidelines for design optimization at deep cryogenic temperatures. Same work has to be done on RF electrical characterization, for which even less data have been published so far.

- [1] B. Cardoso Paz et al., Symposium on VLSI Technology, 2020, https://doi.org/10.1109/VLSITechnology18217.2020.9265034
 [2] B. Cardoso Paz et al. ICMTS, 2020, https://doi.org/10.1109/ICMTS48187.2020.9107906 (Best paper award)
 [3] M. Cassé et al., Appl. Phys. Lett., 2020, https://doi.org/10.1109/ICMTS48187.2020.9107906 (Best paper award)
 [4] B. Cardoso Paz et al., IEEE Trans. Electron Devices, 2020, https://doi.org/10.1109/ICM.2020.3021999





02

MEMORIES

- Exploiting resistive memory randomness with Bayesan neural networks
- High density RRAM arrays for neuromorphic applications based on 3D monolithically Integrated technology and multi-level programming strategies
- 3D RRAM with Gate-All-Around stacked nanosheet transistors for in-memorycomputing.
- Phase change memory: electro-thermal and phase field simulations to explore Innovative PCM architectures and PCM crystallization mechanisms
- Ovonic threshold switching and phase-change memory devices for storage class memory
- Co-integration of resistive memories with backend selectors for future high energy efficient systems
- BEOL compatibility of Si:HfO₂ ferroelectric films and demonstration of nanosecond laser anneal to boost their remanent polarization

Exploiting resistive memory randomness with Bayesian neural networks

RESEARCH TOPIC:

Development of resistive memory based Bayesian neural network hardware and machine learning algorithms

AUTHORS:

T. Dalgaty, N. Castellani, D. Querlioz¹, E. Vianello

For decades, resistive memory devices (RRAM) have been heralded as a means of reducing the energy requirements of neural networks deployed on edge devices. However, their adoption in industrial neural network products remains challenging and scarce. This is because the intrinsic random and noisy properties of RRAM do not offer the high-precision programmable memory element demanded by traditional "deterministic" neural networks. Bayesian neural networks, whose synapses and neurons are described by probability distributions, can in contrast actively harness this randomness. This emerging research activity aims to explore how these intrinsic 'non-ideal' device properties can be leveraged in low-energy Bayesian neural network hardware and learning algorithms.

SCIENTIFIC COLLABORATIONS: 1 CNRS, Université Paris-Saclay

Context and Challenges

Resistive memory devices efficiently implement the dot-product operation that underpins neural network models. However, neural networks and learning algorithms implemented using RRAM perform poorly compared to software counterparts realized on microprocessors. The reason for this is that "deterministic" neural networks require memory elements that can be precisely controlled - intrinsically RRAM doesn't offer this.

Main Results

We argue that it is the modelling approach, not the technology, that is the problem. Synaptic parameters and neurons in **Bayesian neural networks** are described using random variables. RRAM effectively also behave as nanoscale, physical random variables. Could RRAM and Bayesian neural networks be a better pairing? In two recent publications this year, we have argued this is the case [1,2]. Notably we demonstrated that the random properties of RRAM could be harnessed to by reduce by five orders of magnitude the energy required in implementing Bayesian machine learning algorithms.

Perspectives

Bayesian neural networks based on RRAM offer a means of bringing inference and learning to extremely energy and memory constrained edge devices. Our attention is turning towards the question of edge learning systems might operate given that labelled datasets do not exist at the edge and how Bayesian learning algorithms can be applied in the unsupervised, reinforcement and self-supervised settings.

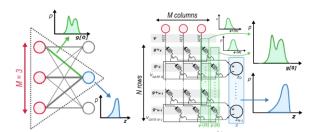


Figure 1: An RRAM-based Bayesian neuron

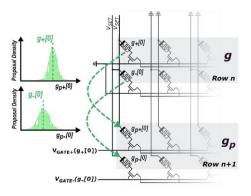


Figure 2: Ideal properties for Bayesian learning

- [1] T. Dalgaty, Advanced Intelligent Systems, 2021, https://doi.org/10.1002/aisy.202000103
- [2] T. Dalgaty, Nature Electronics, 2021, https://doi.org/10.1038/s41928-020-00523-3

High density RRAM arrays for neuromorphic applications bases on 3D monolithically integrated technology and multi-level programming strategies



RESEARCH TOPIC:

Emerging Non-Volatile Memory Circuits, 3D Integration, Neuromorphic Systems

AUTHORS:

E. Esmanhotto, L. Brunet, N. Castellani, JM. Portal¹, S. Mitra³, F. Andrieu, C. Fenouillet-Beranger, E. Nowak, E. Vianello.

CEA-Leti showed, for the first time, a 3D monolithically integrated multiple 1T1R Resistive RAM (RRAM). Our recent studies combines the mentioned new stack technology with a Multi-Level Cell (MLC) programming strategy allowing up to 3.17 bits to be stored in a single RRAM device. The proposed high density solution is extensively tested on a 4 kb 1T1R planar array for both memory and neuromorphic applications and the results shows that neuromorphic applications seems to be better suited for MLC programming because standard memory applications suffers from overlaps between programmed levels after the conductance relaxation effect.

SCIENTIFIC COLLABORATIONS: ¹Aix-Marseille Université, IM2NP, Marseille (FR), ²Université Paris-Saclay, CNRS, Palaiseau (FR), 3Stanford University, Stanford, CA (USA)

Context and Challenges

One of the main challenges for RRAM-based memory arrays is achieving high density of storage. For standard memory applications, high density is fundamental to place the RRAM technology among standard and scalable CMOS. Although, RRAM based memory circuits are also good for neuromorphic hardware thanks to the capability of RRAMs to perform a MAC operation naturally. Nevertheless, for neuromorphic applications, high density is also necessary in order to enhance performance of the system.

The bottleneck of the 1T1R structure remains the size of the access transistor that comes along with the RRAM device. The access transistor has to be big enough to drive the current necessary to program the RRAM and the 1T1R total surface is then appropriated by a transistor with a size that is hard to reduce. To overcome this scenario, it is possible to combine CEA-Leti latest advances on 3D stack integration and Multi-Level Cell (MLC) programming to achieve a high-density 3D monolithically integrated multiple 1T1R cell.

Our solution to improve RRAM density consists in combining a new 3D monolithically integrated multiple 1T1R (figure 1) developed at CEA-Leti with our own Multi-Level Cell (MLC programming strategy.

The 3D monolithically integrated multiple 1T1R might achieve 1.5X more density when compared to a standard planar 1T1R cell and features two HfO2 based RRAM fabricated on the BEOL with one of the RRAM connected to the bottom transistor and another connected to the top transistor. This 3D integrated 1T1R cell preserves the same behavior as a standard planar 1T1R cell.

The adopted MLC programming strategy was extensively studied for memory and neuromorphic applications using a 4 kb planar array. We show that it is possible to program up to nine conductance levels (equivalent to 3.17 bits) per RRAM device relying on the cycle-to-cycle variation of the RRAM devices while controlling the programming current which remains as low as possible to keep low power.

Standard memory applications suffers from the overlap between adjacent levels after programming due to the conductance relaxation effect. For memory applications, the MLC strategy is limited to four conductance levels (2 bits) in order to keep an acceptable BER. On other hand, we proposed a Neural Networks seems to be resilient to conductance relaxation, taking full advantage of the nine conductance levels. On this scenario, we improve by 4.75x the density of a RRAM 1T1R cell for Neural Network applications.

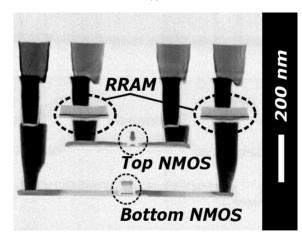


Figure 1: 3D structure with two CMOS and two RRAM.

Perspectives

Our research will continue to investigate MLC programming as a key feature of RRAM with the potential of leading us to further demonstrations of high performance and high-density neuromorphic hardware. Different design solutions might be proposed to handle the MLC programming strategy better while new CEA-Leti stack technologies will continuously be explored.

- [1] E. Esmanhotto et al., 2020 IEEE International Electron Devices Meeting (IEDM), 2020, https://doi.org/10.1109/IEDM13553.2020.9372019
 [2] C. Fenouillet-Beranger et al., 2020 IEEE Symposium on VLSI Technology, 2020, https://doi.org/10.1109/VLSITechnology18217.2020.9265092

3D RRAM with Gate-All-Around stacked nanosheet transistors for in-memory-computing

RESEARCH TOPIC:

Resistive RAM, HfO₂-based OxRAM, qate-all-around, nanosheet, junctionless, in-memory-computing

AUTHORS:

M. Ezzadeen, T. Dubreuil, N. Castellani, J.M. Hartmann, B. Previtali, J.M. Portal¹, G. Ghibaudo², F. Andrieu, and **S. Barraud**.

This work explores a novel 3D one transistor / one RRAM (1T1R) memory cube. The proposed architecture integrates HfO_2 -based OxRAM with select junctionless (JL) transistors based on Gate-All-Around stacked NanoSheet (NS) technology. Extensive characterization of JL transistors and OxRAMs is performed to show their ability to be co-integrated inside a same 1T1R memory cell. We show that a proper engineering of JL GAA transistors can result in compliance currents which are high enough to address OxRAM arrays whose memory window reaches HRS/LRS = 20 up to 10^4 cycles. This new architecture, which offers a high write and read parallelism, can be leveraged for in-memory-computing (IMC).

SCIENTIFIC COLLABORATIONS: ¹ University Aix Marseille, CNRS, IM2NP, Marseille, France, ² University Grenoble Alpes, IMEP-LAHC, 38000 Grenoble, France.

Context and Challenges

Today, storage-class memories like high-density 3D crossbar RRAM are promising for applications requiring a large amount of on-chip memory. RRAM is a leading candidate due to its high density, good scalability, low operating voltage, and easy integration with CMOS devices. Another attractive aspect of RRAM is their ability to perform primitive Boolean logic operations for in-memory and neuromorphic computing. However, if the 1T1R design is the most reliable architecture for IMC, the cell size remains limited by the conventional access transistor. This is why, in this work, our 1T1R architecture benefits from the high density of vertically stacked NS transistors which feature excellent scalability. This novel 1T1R 3D RRAM architecture is competitive from the crossbar density point of view, while getting rid of any sneak path current, enabling large-scale IMC.

Main Results

Our 3D 1T1R architecture is derived from our GAA CMOS structure and process flow; the main difference is that each horizontal GAA channel features an independent source connected to a BitLine (BL) and a drain directly connected to a pillar of RRAM memory cells (figure 1) [1]. First, we study the performance of GAA JL transistors used as selector. Preliminary TCAD simulations enabled us to find a good compromise between high performance and good electrostatic control. Then, we fabricated nMOS JL transistors with one level of NS. They exhibit an I_{ON} current of 120 μ A at $V_{DS} = 1.3 \text{ V}$, $V_{GS} = 1.5 \text{ V}$, $L_G = 60 \text{ nm}$ and W = 50 nm, which should be translated into a compliance current I_{CC} close to 150 μA at W = 80 nm (targeted width of our select GAA transistors). We also checked that the local variability is not strongly degraded with JL transistors and that they can be cycled up to $V_{\text{DD}} = 2 \text{ V}$ more than 107 times with negligible electrical characteristic modifications [2]. Similarly, we characterized 4kbits 1T1R RRAM arrays based on TiN bottom electrode / 5 nm $HfO_2/5$ nm $\operatorname{Ti}/\operatorname{TiN}$ top electrode integrated in the BEOL with select transistors based on 130nm CMOS technology. Electrical characterization of 4kbits OxRAM arrays shows a large memory window (HRS / LRS = 20) up to 10^4 cycles with a current compliance of $150\,\mu\text{A}$, compatible with the performances of our JL transistors. Finally, we experimentally demonstrate scouting logic operations capability with 2 operands, which should be extended to 4 operands thanks to an original two cells/bit "double coding" scheme assessed by SPICE simulations [3]. We evidenced that this computing scheme which is 2 times more energy efficient than a write-verify approach can be a good option to perform *in-situ* logic operations.

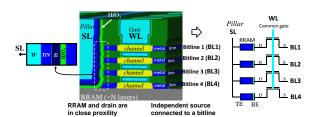


Figure 1: 1T1R OxRAM memory cell

Perspectives

Technological development of modules are still ongoing in order to build and explore this 1T1R 3D RRAM architecture. This work is also supported by SPICE simulation to investigate the interest of this novel architecture for IMC.

- [1] S. Barraud et al., 2020 IEEE International Electron Devices Meeting (IEDM), https://doi.org/10.1109/IEDM13553.2020.9371982
 [2] D. Bosch et al. 2020 IEEE Symposium on VLSI Technology, https://doi.org/10.1109/VLSITechnology18217.2020.9265036.
- [2] D. Bosch et al. 2020 IEEE Symposium on VLSI Technology, https://doi.org/10.1109/VLSITechnology18217.2020.9265036.
 [3] M. Ezzadeen et al. IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4626-4630, Nov. 2020, https://doi.org/10.1109/TED.2020.3020779.

Phase change memory: electro-thermal and phase field simulations to explore innovative PCM Architectures and **PCM Crystallization Mechanisms**

RESEARCH TOPIC:

PCM, Ge rich GST, Innovative PCM, Phase Change Mechanism, Electro-thermal and Phase Field simulations, Physical Characterization

AUTHORS:

O. Cueto, G. Navarro, E. Nolot, L. Prazakova, A.L. Serra, R. Bayle^{1,2,4}, M. Plapp², C. Vallee³, M.C. Cyrille

Phase-Change Memory (PCM) is one of the most promising innovative non-volatile memory technologies. We report on PCM TCAD simulation activity at the CEA-Leti that provides guidelines to technological development but also insight in complex physical crystallization mechanisms. The realizations we report on also illustrates the complementarity of TCAD simulation activity with electrical characterization and advanced physical characterization activities at CEA-Leti.

SCIENTIFIC COLLABORATIONS: 1 STMicroelectronics, 2 LPMC CNRS-Ecole Polytechnique, 3 CNRS-LTM, 4 CEA-Leti.

Context and Challenges

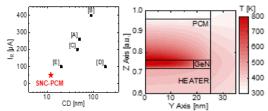
PCM entered the market addressing Storage Class Memory and it is in sampling within Microcontrollers for Automotive applications. PCM architecture optimization and crystallization dynamics understanding are still required.

Main Results

We demonstrated that a lithography independent Self-Nano-Confined PCM enables programming down to 50 □ A and endurance more than 108 cycles in a 4kb array (Figure 1a). 3D Electro-thermal simulations highlighted that such low current density is due to a better thermal confinement (Figure 1) [1]. With LPMC and STMicroelectronics, we developed a tool with the multiphase field method to simulate phase changes in Ge rich GST [2]. It captures both the emergence of a two-phase polycrystalline layer starting from an amorphous layer (Figure 2) and the melting and recrystallization during the SET and RESET operations in a "wall" type PCM [2]. Experimental results (XRD, FTIR and Raman) confirm the emergence of two distinct crystalline phases: Ge/GST[3].

Perspectives

A full coupling of the multiphase field model with the electrothermal solver will be implemented in collaboration with advanced physical characterization team and atomistic simulation team. Microstructure of the material modifies the current and the temperature through the PCM. In order to include such heterogeneities, the equations for electric and heat conduction need to be resolved with the same spatial resolution as the phase-field model, with phase dependent properties.



- [A] J.I. Lee et al, VLSI 2007
- [B] R. Anunziata et al. IEDM 2009
- [C] G. Servalli, IEDM 2009
- [D] S. Hanzawa et al, ISSCC 2007
- [E] Y. Choi et al, ISSCC 2012

Figure 1: Left) SNC vs other PCM Right) T SNC

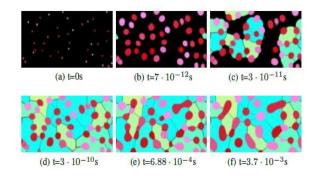


Figure 2: Crystallization (pink: Ge, green: GST)

- [1] A.L. Serra et al, Transactions on Electron Devices (2020), https://doi.org/10.1109/TED.2020.3044267
 [2] R. Bayle et al, Journal of Applied Physics (2020), https://doi.org/10.1063/5.0023692
- [3] L. Prazakova et al, Journal of Applied Physics (2020), https://doi.org/10.1063/5.0027734

Ovonic threshold switching and phase-change memory devices for storage class memory

RESEARCH TOPIC:

Ovonic Threshold Switching (OTS), Phase-Change Memory (PCM), Storage Class Memory (SCM)

AUTHORS:

C. Laguna, G. Lama, M. Bernard, N. Castellani, S. Abdelkader¹, G. Navarro

Back-End-of-Line (BEOL) resistive memory technologies demonstrated to be the right enabler for Storage Class Memory (SCM) applications required in modern and future memory-centric architectures. This was possible thanks to the combining of the unique selector features of Ovonic Threshold Switching (OTS) devices, with the reliability and maturity of Phase-Change Memory (PCM). In this framework, we developed and analyzed a new class of OTS devices called "OTS Multilayer" (OTS ML) enabling low electrical properties variability and studied key metrics and reliability analysis protocols in PCM targeting high endurance and high speed and preparing next generation of high density 3D multiple decks Crossbar arrays based on PCM and OTS.

SCIENTIFIC COLLABORATIONS: 1 INSA Lyon

Context and Challenges

Storage Class Memory (SCM) became a necessary level of the memory hierarchy with the goal to provide a low read latency, non-volatile and cost effective interface between the memory (DRAM) and the storage (NAND Flash). 3D Crossbar arrays, enabled by BEOL OTS and resistive memory technologies, represent the best candidates for SCM, but they require extremely high endurance and high programming speed.

Main Results

We demonstrated that through a new family of selector devices called "OTS Multi-Layer", we can target the material stability at 400°C and the tuning of the selector switching performances by properly engineering interfaces, thickness and individual layers' stoichiometry. We validated the high variability control of the electrical parameters and a high endurance up to more than 10° cycles (Figure 1) wrt to a standard bulk solution [1]. SCM suitability was investigated in GeTe and GeSbTe based PCM devices, studying and describing their main metrics evolution along cycling. Thanks to the subthreshold conductivity and retention analyses, we provide evidence why GeSbTe alloys can target an endurance of more than 109 cycles at low programming energy (Figure 2), fulfilling SCM requirements [2].

Perspectives

Co-integration of best OTS and PCM technologies available in Leti is ongoing, targeting the demonstration of the reliability of the Crossbar arrays and of the new devices architectures developed. This will enable new memory design paradigms and new applications.

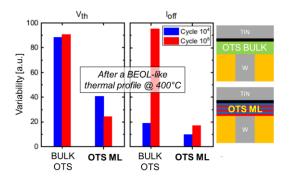


Figure 1: Threshold switching and leakage current spread

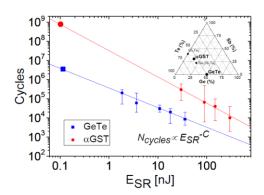


Figure 2: Endurance performances

- [1] C. Laguna et al, International Memory Workshop (IMW), 2020, https://doi.org/10.1109/IMW48823.2020.9108130 [2] G. Lama, Microelectronic Reliability, 2020, https://doi.org/10.1016/j.microrel.2020.113823

Co-integration of resistive memories with back-end selectors for future high energy efficient systems



RESEARCH TOPIC:

Resistive memories, RRAM, 1S1R, crossbar, crosspoint, programming, in memory computing

AUTHORS:

J.M. Lopez, P. Trotti, L. Grenouillet, N. Castellani, J. F. Nodin, G. Navarro, S. Oukassi, G. Pillonnet, C. Carabasse, G. Molas

We have developed low voltage operation 1S1R structures composed by resistive memories (RRAM) integrated with a back-end selector which can be adjusted based on the circuit requirements. We also propose an innovative low power charge based RRAM programming scheme. These solutions provide a powerful set for boosting energy efficiency and improving performances like endurance and variability.

SCIENTIFIC COLLABORATIONS: 1 IMEP-LAHC, 2 IM2NP Marseille, 3 INL-CNRS, INSA de Lyon

Context and Challenges

Resistive Memories (RRAM) is a promising hardware candidate implementing performant In Memory Computing architectures. Developing dense crosspoint arrays and efficient programming scheme are key enablers to boost the actual RRAM performances.

Main Results

We designed two RRAM based crosspoint structures showed forming free behavior, stable 2 decades for lon/loff during 107 cycles and moderate leakage current compatible with 100kB. Playing with the memory and selector stacks, we explore high density integration allowing >1MB crosspoint arrays with low voltage operation on a 28nm core process.

We also developed an innovative programming scheme consisting of discharging a programming capacitor over the memory cell, controlling the maximum energy provided to the The solution was experimentally validated demonstrating the potential to reduce the programming energy of a factor of 10 in comparison with standard writing scheme.

Perspectives

We are investigating the impact of scaling of RRAM based crosspoints. We are also implementing fully integrated charge based programming scheme on next test vehicles to demonstrate energy and variability gains for future in memory computing systems.

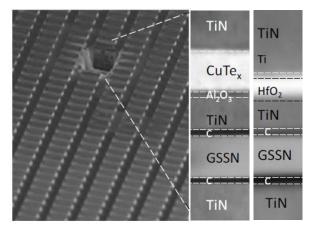


Figure 1: 1S1R and stacks for crosspoint arrays.

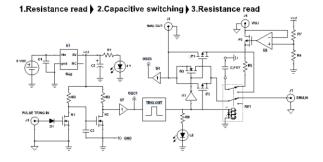


Figure 2: Charge based programming circuit board

- [1] G. Molas et al., IEEE International Memory Workshop (IMW), 2020, https://doi.org/10.1109/IMW48823.2020.9108143
 [2] J. M. Lopez et al., IEEE International Memory Workshop (IMW), 2020, https://doi.org/10.1109/IMW48823.2020.9108126
 [3] P. Trotti et al., IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS), 2020, https://doi.org/10.1109/ICMTS48187.2020.9107936

BEOL compatibility of Si:HfO₂ ferroelectric films and demonstration of nanosecond laser anneal to boost their remanent polarization

RESEARCH TOPIC:

Ferroelectric HfO_2 , Back End of Line integration, CMOS compatibility, Nanosecond Laser Anneal, Silicon doping

AUTHORS:

T. Francois, J. Coignus, S. Kerdilès, N. Vaxelaire, C. Carabasse, S. Slesazeck¹, U. Schroeder¹, T. Mikolajick¹, **L. Grenouillet**

Scaled ferroelectric Si-implanted HfO $_2$ capacitors of 0.28 μ m² were successfully co-integrated above 130 nm CMOS, demonstrating for the first time BEOL compatibility of this material. Area scaling is shown to improve endurance (10¹² cycles extrapolated at 3 V). Excellent distributions of coercive fields E_{C+}, E_{C-} and remanent polarization 2·P_R are reported at wafer scale, as well as excellent data retention at 85 °C. Nanosecond Laser Anneal (NLA) is demonstrated to be extremely powerful to "engineer" ferroelectric film crystallization. Ferroelectric undoped HfO $_2$ is obtained with this technique, and 2.P_R values > 20 μ C/cm² are reported for Si:HfO $_2$, while keeping BEOL compatibility.

SCIENTIFIC COLLABORATIONS: ¹NaMLab gGmbH, Dresden, Germany

Context and Challenges

Ferroelectric HfO₂-based thin films are changing the paradigm of ferroelectric memories, thanks to their CMOS compatibility and potential for scalability. In 2019, our group demonstrated for the first time that scaled Hf0.5Zr0.5O₂-based ferroelectric capacitors integrated above 130 nm CMOS are compatible with BEOL thermal budget [1,2]. In the following 10 nm Si-doped HfO₂ films, whose crystallization temperature is higher than Hf0.5Zr0.5O₂, were assessed.

Main Results

TiN/Si:HfO $_2$ /TiN capacitors with diameters of 600nm (0.28µm²) were integrated in 130nm BEOL CMOS between M4 and M5. Our approach consists in doping the 10 nm HfO $_2$ film by ion implantation, which facilitates intermixing compared to the conventional ALD doping technique. Ferroelectric behavior is reported with a maximum thermal budget of 450°C for crystallization (Figure 1). Capacitor area downscaling is demonstrated to be beneficial for high endurance (10 12 cycles extrapolated at 3 V).

In order to improve further film crystallization in the orthorhombic (ferroelectric) phase, Nanosecond Laser Anneal is demonstrated to be very promising to increase temperature above 1000 $^{\circ}\text{C}$ in the HfO₂-based film without compromising CMOS integrity (Figure 2).

Perspectives

These results pave the way to the demonstration of 1T-1C FeRAM memory arrays using ferroelectric HfO $_2$. In particular, the high endurance demonstrated for HfO $_2$ -based capacitors is promising to bridge the gap toward the 10^{15} cycling requirement.

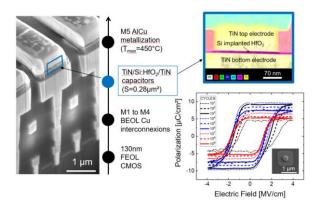


Figure 1: HfO₂-based BEOL ferroelectric capacitors

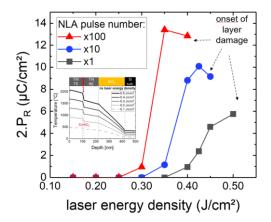
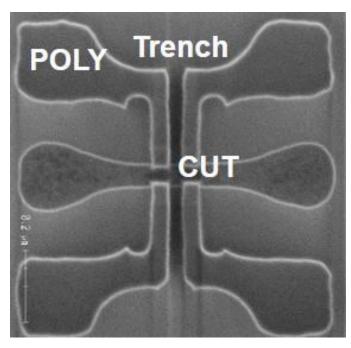
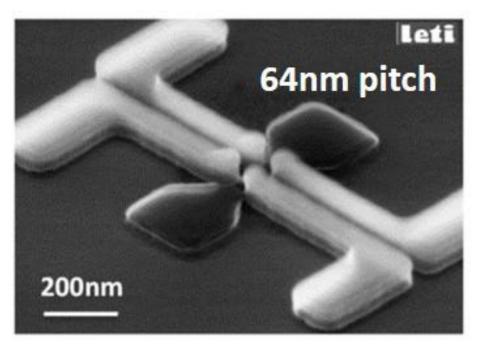


Figure 2: Laser Anneal boosts remanent polarization

- [1] T. François et al., IEEE International Electron Devices Meeting (IEDM), 2019, https://doi.org/10.1109/iedm19573.2019.8993485 [2] L. Grenouillet et al., IEEE Silicon Nanoelectronics Workshop (SNW), 2020, https://doi.org/10.1109/SNW50361.2020.9131648
- [3] L. Grenouillet et al., IEEE Symposium on VLSI Technology (VLSI), 2020, https://doi.org/10.1109/VLSITechnology18217.2020.9265061



Gate Patterning with (Litho-etch³) triple process Pitch down to 64 nm and OVL spec. <30nm



2D quantum-dot arrays

© CFA-I et

03

PATTERNING

- Immersion lithography on the edge
- Etching impact on the self-assembly and pattern transfer of block copolymers for new advanced patterning approach
- Sub-15 nm multilayer nanopillar patterning for hybrid SET/CMOS integration
- Development of non-conventional chemistries for advanced CMOS spacer patterning
- Hybrid E-beam lithography capabilities for a large field of nanodevices applications

Immersion lithography on the edge

RESEARCH TOPIC:

Immersion lithography, 193i, patterning, large field stitching, negative tone development (NTD)

AUTHORS:

M. Argoud, A. Le Pennec, R. Tiron, C. Comboroure, B. Minghetti¹, Pui Lam², C. Navarro³, M. May, G. Rademaker

Immersion 193 nm lithography is a mature technology that enables to address new challenges outside the conventional fields of application. For a polarization filter application, a full wafer has been seamlessly exposed with continuous high resolution line/space gratings. A second advanced use case was to implement a negative tone development (NTD) resist to enlarge patterning performance, required for the Directed Self-Assembly (DSA) of lamellar line/space block copolymers (BCP) with a nominal period L_0 of 31.5 nm.

SCIENTIFIC COLLABORATIONS: 1,2 ASML (FR, NL), 3 Arkema (FR)

Context and Challenges

Immersion lithography (IL) has been a workhorse semiconductor technology for over a decade. The reticle is usually limited by the field size of 26 mm x 33 mm. For a polarization filter application, the required effective field size was 20 cm by 20 cm consisting of a continuous grating with a CD of 50 nm and a period of 100 nm. This required an unusual field-to-field positioning measurement and control within the same layer, which can be extended to large chips for other applications [1]. A second advanced use case is overcoming the resolution limits of the immersion scanner by means of pitch multiplication by DSA of lamellar BCPs. In order to prevent assembly defects, these polymers need high-quality guides [2].

Main Results

For the polarizer stitching application, a diffraction based overlay (µDBO) target has been developed to measure the stitching alignment between the different exposed fields. The field-to-field stitching performance was measured and corrected by a novel 13-term polynomial model developed by ASML, until a stitching of 1.5 nm (μ+3σ) misalignment was attained. This result was applied to the polarizer case (without µDBO marks) and combined with an aerial image simulation to address stitching artefacts such as line pinching and bulging and to determine the best conditions for continuity. This resulted in a full 300 mm wafer seamlessly exposed with 50 nm CD, 100 nm period line/space gratings [1].

The ACE process for DSA, unique at CEA-Leti is based on the use of spacer double patterning to create the guides for the DSA of 31.5 nm period line/space patterns. Given their sensitivity to the quality of the guiding pattern, IL combined with a negative tone development (NTD) resist has been put in place [2]. The use of a mask with large-scale features has been a key enabling factor to decrease alignment defects of block copolymers by three orders of magnitude to 10⁴ cm⁻².



Figure 1: Seamless stitching of 4 fields (CD = 50 nm

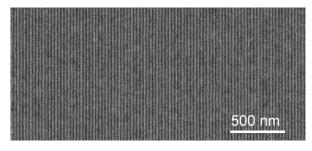


Figure 2: Alignment of block copolymers (CD = 16 nm

Perspectives

The seamless stitching approach developed can be used for imagers with high-resolution features, ultra-large die electronics and becomes necessary for high-NA (0.55) EUV lithography. NTD resists will be pursued for the most demanding of patterning applications sensitive to patterning variations, such as silicon quantum computing and low-loss photonic applications.

- [1] M. May et al. Proc. SPIE 11325 (2020), https://doi.org/10.1117/12.2552012 [2] G.J. Rademaker et al, Proc. SPIE 11326 (2020), http://doi.org/10.1117/12.2552003

Etching impact on the self-assembly and pattern transfer of block copolymers for new advanced patterning approach

RESEARCH TOPIC:

Etching for Directed Self-Assembly (DSA) application

AUTHORS:

M. G. Gusmão Cacho, K. Benotmane, P. Pimenta-Barros, C. Navarro¹, K. Sakavuyi², N. Possémé

Directed Self-Assembly (DSA) of block copolymers is an advanced patterning technique being investigated to target small and dense patterns for the future technological nodes. The most important aspect of this technique is to obtain guided patterns with long-range order and then remove one of the phases to achieve a mask for pattern transfer of the features. The etching impact on the ACE (Arkema-CEA) chemo-epitaxy flow has been studied and the etching steps have been optimized to eliminate self-assembly defects. In order to transfer the line patterns obtained through the block copolymer into the hard mask, we have developed a mixed wet and dry etching approach for a modified PS-b-PMMA high chi block copolymer presenting a pitch of 18 nm.

SCIENTIFIC COLLABORATIONS: ARKEMA (FR), Brewer Science Inc.(USA)

Context and Challenges

For the sub-10 nm nodes, pattern scaling has slowed down due to conventional lithography limitations in terms of resolution, defectivity and cost. Our research proposes to introduce the Directed Self-Assembly (DSA) of block copolymers (BCPs) as a low-cost solution to obtain high-resolved and dense patterns. This approach is based on the self-assembly property of BCPs, which are capable of microphase separation, forming a dense array of ordered nanostructures with dimensions from 50 nm down to 5 nm.

Main Results

We evaluated the impact of the etching steps involved in the ACE (Arkema-CEA) chemoepitaxy flow, namely regarding the adherence of the neutral layer. Following the flow optimization, we successfully demonstrated the chemoepitaxy of a PS-b-PMMA with 32 nm pitch without alignment defects on a 100 μm² surface (Figure 1) [1].

We then developed a mixed wet and dry etching approach to selectively remove the PMMA from a high-χ modified PS-b-PMMA with 18 nm pitch. With this approach, the pattern transfer of the PS lines into the SiO2 and silicon layers was validated (Figure 2). The results show that, for small and dense pitches, the main dry etching key challenges come from the trade-off between achieving high selectivity and avoiding bridge formation [2].

Perspectives

Now that we have optimized the ACE flow and demonstrated an etching approach for the high- χ PS-b-PMMA on free surface, the next step will focus on adapting the flow to guide the 18-nm pitch high-x BCP into straight lines.

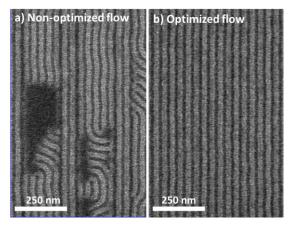


Figure 1: ACE flow applied to PS-b-PMMA.

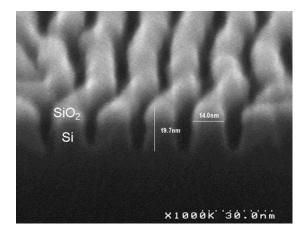


Figure 2: Pattern transfer of PS lines

RELATED PUBLICATIONS:

[1] M. G. Gusmão Cacho et al., Journal of Vacuum Science and Technology A, (39), 033004 (2021), https://doi.org/10.1116/6.0000850

[2] M. G. Gusmão Cacho et al., Microelectronic Engineering, (230) 111369 (2020), https://doi.org/10.1016/j.mee.2020.111369

Sub-15 nm multilayer nanopillar patterning for hybrid SET/CMOS integration

RESEARCH TOPIC:

Single-electron-transistor, nanopillars patterning, E-beam lithography, multilayer RIE, low-temperature plasma oxidation

AUTHORS:

P. Brianceau, A. Gharbi, F. Laulagnet, G. Rademaker, J. V. Borany¹, H.-J. Engelmann¹, M. Rommel², E. Amat³, M.-L. Pourteau

The Internet of Things (IoT) is a strongly growing market, with 20 billion connected devices expected in 2020. A critical constraint for those devices is to offer low power consumption. In this context, single-electron-transistors (SETs), consisting of a Si quantum dot lying between two tunnel junctions to neighboring drain and source Si regions, are gathering growing interest. For future industrialization, it is crucial to show a 200 mm CMOS-compatible fabrication of SETs working at room temperature. This is the goal of the IONS4SET European project in which LETI was involved in the last 4 years.

SCIENTIFIC COLLABORATIONS: 1 HZDR, Dresden (DE), 2 Fraunhofer-IISB, Erlangen (DE), 3 IMB-CNM, Bellaterra (ES)

Context and Challenges

The SET physics is based on tunneling effect through a quantum dot between the source and drain of a gate-all-around nanopillar (NP) transistor, and typical Coulomb-blockade oscillations are observed on I-V plots. Those devices are functional at room temperatures and low voltages if the dimension of NP and quantum dot are in the nanometer range. From device simulations of various pillar geometries, we targeted the challenging patterning of NP of ~70 nm height and sub-15 nm diameter, with an embedded thin SiO₂ gate layer.

Main Results

By combining electron-beam lithography with dry reactive ion etching, we have structured such NPs with a diameter down to 19 nm [1]. A resist trimming step enables to reduce the diameter, while the SOC/SiARC/resist tri-layer stack enhances etch selectivity. The CD uniformity is 2.5 nm, and NPs profile are straight. A sacrificial oxidation which consumes a fraction of the pillars surface Si, followed by HF removal of the oxide, further reduces the diameter. Low-temperature (<400°C) plasma oxidation using Hyperion® equipment from HQ-Dielectrics ensures the stability of the Si quantum dot in the oxide. NPs down to 10 nm diameter (Figure 1) have been reliably fabricated and contacted for further electrical testing (Figure 2) [2].

Perspectives

A key future achievement is to integrate SETs in hybrid SET/FET devices.

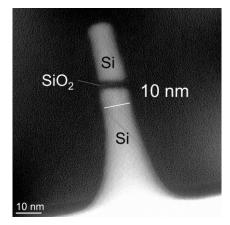


Figure 1: TEM image of a NP after plasma oxidation

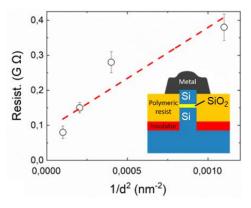


Figure 2: Resistance of contacted NP vs. diameter

- [1] M.-L.Pourteau et al., Micro and Nano Engineering, (9) 100074 (2020), https://doi.org/10.1016/j.mne.2020.100074, [2] E. Amat et al., Nanomaterials, 10(4), 716 (2020), https://doi.org/10.3390/nano10040716

Development of non-conventional chemistries for advanced CMOS spacer patterning



RESEARCH TOPIC:

Dry and wet etch patterning of advanced logic devices

AUTHORS:

O. Pollet, V. Ah-Leung, V. Bacquié, A. Tavernier, F. Boulard, N. Possémé

Silicon Nitride (SiN) spacer etching in 3D CMOS technologies has become a very challenging step to be able to complete the etching while preserving channel materials. The formation of parasitic spacers along fin sidewalls requires a lengthy overetch compared to conventional planar integrations. Thanks to SiCl₄ addition, we develop a cyclic strategy alternating selective passivation and nonselective etching. On nanowire-type patterned structures, it shows the full removal of the parasitic spacer while providing a silicon loss of less than 2 nm.

Context and Challenges

The $\mathrm{Si_3N_4}$ spacer forms the mask for source/drain implantation and protects the gate sidewalls for advanced CMOS transistor integration. Its etching is a critical step which requires selective etch stop and low damage on silicon. Moreover, in 3D CMOS technologies, gate stack and spacer materials must be etched away during patterning not only from horizontal planes like channel top or STI but also from channel sidewalls.

Main Results

Thanks to the addition of $SiCl_4$ to conventional CH_3F based chemistry, we show a selective etch stop and low damage on silicon by the formation of a SiO_xF_y passivation layer, which limits the transfer of the reactive layer into the silicon film. Application on the pattern revealed that this approach offers non-facetted Si_3N_4 spacer, no foot formation, and 1 nm SiGe consumption [1]. For 3D CMOS integration, where parasitic spacer on fin sidewall should be removed, a cyclic sequence alternating $SiCl_4$ steps with nonselective CHF_3 steps is developed and validated. When applied to nanowire patterned structures, this process demonstrates to induce less than 2 nm of silicon loss despite the long overetch used to thoroughly eliminate parasitic spacers on fin sidewalls [2].

Perspectives

Further developments are ongoing to enhance SiCl₄-containing process performances on patterned structures and make them fulfill specifications for spacer etching in 3D CMOS integration.

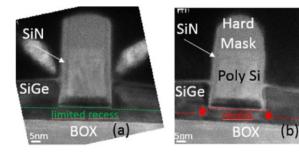


Figure 1: Etching with (a) or without (b) SiCl₄ addition

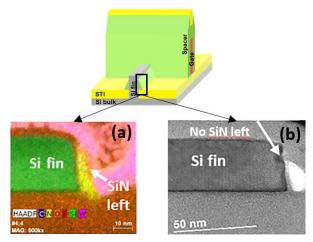


Figure 2: Continuous (a) vs. cyclic (b) approach

- [1] N. Posseme, et al., J. Vac. Sci. Technol. A 38, 033004 (2020) https://doi.org/10.1116/1.5145158
- [2] O. Pollet, et al., J. Vac. Sci. Technol. A 38, 063007 (2020) https://doi.org/10.1116/6.0000584

Hybrid E-beam lithography capabilities for a large field of nanodevice applications

RESEARCH TOPIC:

hybrid lithography, E-beam, DUV, resists, shape-beam tool, advanced devices

AUTHORS:

F. Laulagnet, M. Cannac, A. Gharbi, J.A. Dallery¹, C. Charpin-Nicolle, Marceline Bonvalot², S. Landis, P. Sixt, I. Servin

Maskless lithography is versatile and a cost-effective patterning approach, well suited for demonstrators of nanodevice fabrication and covering a large field of applications (Photonic, Displays/LED, Memories, FDSOI, quantum computing, MEMS or RF). The hybrid lithography concept allows to reduce significantly writing time by coupling high-resolution of Electron Beam Direct Write (EBDW) lithography and high-throughput of a mask-based DUV lithography. This approach involves two consecutive exposures using a unique resist, unlike complex "mixand-match" multiple patterning strategies.

CEA-Leti demonstrate high-resolution capability down to 30 nm, while matching the whole process to two consecutive exposures and preserving alignment performances.

SCIENTIFIC COLLABORATIONS: 1Vistec Electron Beam GmbH, Jena (DE), 2CNRS-LTM, Grenoble (FR)

Context and Challenges

The hybrid lithography approach involves two consecutive exposures using a unique resist, which is an elegant process without additional etch step. The high-resolved patterns are reserved to E-beam writing whereas non-critical patterns are exposed on DUV optical scanner. The main advantages are writing time gain, design layout flexibility and high resolution but it requires a compatible resist for both exposures and manage delay time constraint and alignment matching between the two lithography tools [1].

Main Results

Hybrid lithography approach is illustrated by the example of memory cells for OXRAM devices [2]. The patterned cells of 30 nm are printed with E-beam and the less aggressive patterns (> 300nm) are exposed on a DUV scanner using a unique negative chemically amplified resist (CAR) with thickness of 70 nm. The CD uniformity and alignment (OVL) are within specifications

The interest of hybrid lithography was fully demonstrated in terms of gain in throughput, high-resolution by matching the single resist process to both E-beam & DUV lithography. To extend hybrid flow to novel resist platforms with DUV 193 nm, alternative solutions to conventional CAR resists show promising results in terms of sensitivity, resolution, LWR and stacking compatibility.

Perspectives

This new process capability will also strengthen our ability to quickly evaluate new high-resolution designs developed for quantum computing and IA, before moving to immersion 193 nm optical lithography platform which would require a complex and expensive mask set.

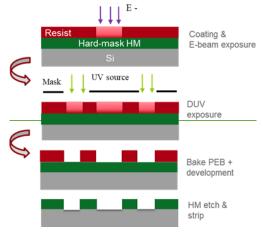


Figure 1: Hybrid lithography concept

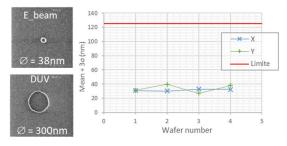
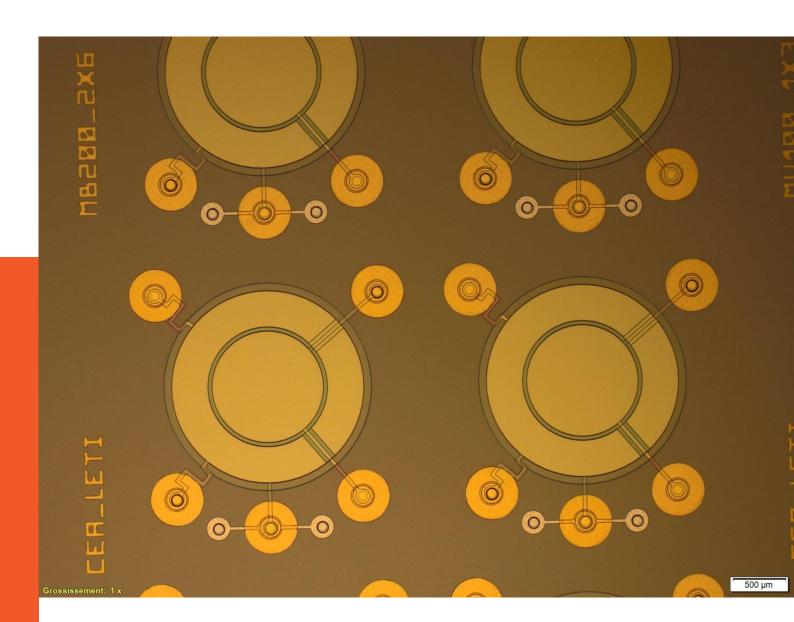


Figure 2: CD-SEM patterns and OVL Mean + 3σ between E-beam and DUV level

- [1] I. Servin et al., Proc. SPIE 11518, Photomask Technology, (2020), https://doi.org/10.1117/12.2572868
 [2] C. Charpin-Nicolle et al., Microelectronic Engineering, (221), 111194, (2020), https://dx.doi.org/10.1016/j.mee.2019.111194



Piezoelectric Membrane Ultrasonic Transducer

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04

MEMS, NEMS & RF COMPONENTS

- AIN-based bimorph piezoelectric micromachined ultrasound transducers for air-borne applications
- Potentialities of single-crystal LiNbO₃ and LiTaO₃ film bulk acoustic resonators for high-frequency filters
- Optomechanical mass sensing
- Magnetically actuated nanostructures for biotechnologies: examples of cancer cells destruction and inhibition of bacterial biofilms formation

AlN-based bimorph piezoelectric micromachined ultrasound transducers for air-borne applications

RESEARCH TOPIC:

Piezoelectric MEMS, Micromachined Ultrasonic Transducer, Time-of-Flight measurement

AUTHORS:

J.C. Bastien, J. Jung, F. Blard, F. Gardien, K. Benedetto, **B. Fain**

In the last years, piezoelectric micromachined ultrasound transducers (pMUT) have raised a great interest for various applications such as obstacle localization, gesture recognition, fingerprint sensing and advanced biomedical applications. Compared to conventional bulk transducer, pMUT are much easier to miniaturize and co-integrate with electronics, what offers important possibilities. CEA-Leti has developed bimorph AIN-based pMUTs, a particular structure that presents good properties for both emission and reception, and are particularly relevant for air-borne pulse-echo measurements.

Context and Challenges

pMUT transducers are both sensors and actuators. Depending on the application, piezoelectric material may be chosen to optimize emission or reception properties. A challenge is to overcome the emission / reception trade-off using a specific bimorph pMUT architecture.

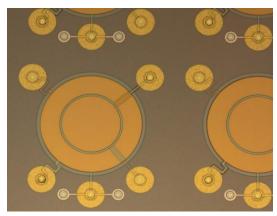
Main Results

We developed an AIN-based bimorph pMUT architecture for air-borne pulse-echo measurements around 100 kHz. As presented in [1], this structure includes four electrode pairs that may be combined to enhance the drive sensitivity. The low dielectric permittivity of AIN and the four channels should also ensure good receive sensitivity and low noise at the electronics stage.

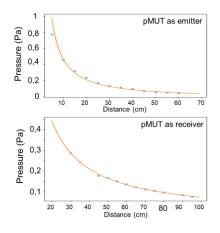
The acoustic characterization of pMUTs confirms the potential of such structure for emission and reception. The figure below presents the pressure emitted by a single membrane excited by a 1V sinusoidal electric actuation at 103 kHz, which is of 70 dB at 50 cm. For reception, the pMUT membrane is used to measure the pressure of a commercial emitter calibrated beforehand. A single membrane may measure a pressure as low as a few mPa, thanks to a dedicated discrete electronics

Perspectives

Pulse-echo measurements may be achieved to benefit from the good properties of the bimorph pMUT. Advanced signal processing, including a matched filter to optimize the data filtering, could also be used to enhance the detection range that could reach several meters for a single membrane.



Top view of AIN bimorph pMUTs



Pressure emitted and received by a pMUT membrane

RELATED PUBLICATIONS:

[1] J. Jung et al., Eng. Res. Express 2 045013 (2020), https://doi.org/10.1088/2631-8695/abc140

Potentialities of single-crystal LiNbO₃ and LiTaO₃ film bulk acoustic resonators for high-frequency filters



RESEARCH TOPIC:

Lithium niobate (LiNbO₃), Lithium tantalate (LiTaO₃), Film Bulk Acoustic Resonator, 5th Generation of mobile applications (5G)

AUTHORS:

M. Bousquet, P. Perreau, C. Maeder-Pachurka, A. Joulie, F. Delaguillaumie, J. Delprato, G. Enyedi, G. Castellan, **A. Reinhardt**

Y+163°-cut LiNbO $_3$ and X-cut LiTaO $_3$ Film Bulk Acoustic Resonators (FBAR) with patterned bottom electrodes and a sacrificial layer cavity have been fabricated using a layer transfer process. FBAR based on 250 nm-thick Y+163°-cut LiNbO $_3$ films displays a single resonance located at 4.78 GHz, with an electromechanical coupling factor (k_1^2) of 17.6%. The quality factor at antiresonance (Q_a) is around 200, leading to a Qxf product close to 9 ×10¹¹, which is slightly higher than previous realizations at 2.5 GHz. The 2 GHz X-cut LiTaO $_3$ FBAR possess a reasonable temperature stability: the temperature coefficients of the resonance and antiresonance frequency were found to be +16 and -42 ppm/K. These TCF values are lower than those reported for LiNbO $_3$ FBARs.

Context and Challenges

With the deployment of the 5^{th} generation of mobile communications standards (5G), RF band pass filters need to cope with an increase in frequency and fractional bandwidth, and a decrease in temperature coefficient of frequency (TCF) and insertion loss. Such wide bandwidths filters require the introduction of passive elements such as inductors in the filter topology, or resonators based on piezoelectric materials with larger electromechanical coupling factors than those of conventional AIN or its derivatives ($k_t^2 = 6.5 - 9$ %). This has motivated works on the development of resonators and filters based on single crystal LiNbO₃ and LiTaO₃ which offer promising perspectives to reach high fractional bandwidth ($k_t^2 = 5 - 45\%$ depending on the bulk waves).

Main Results

We report here the implementation of Film Bulk Acoustic Resonators based on Y+163°-cut LiNbO $_3$ and X-cut LiTaO $_3$ films fabricated using a layer transfer process (4-inch) including patterned bottom electrodes and a sacrificial layer cavity.

Figure 1 shows the electric response of a FBAR based on 250 nm-thick Y+163°-cut LiNbO₃ films. As previously reported, this orientation provides a single resonance, whose frequency is here pushed up to 4.78 GHz due to the reduced piezoelectric film thickness. The effective electromechanical coupling factor is close to 17.6%. The quality factor at antiresonance is around 200, leading to a Qxf product close to 9×10¹¹, which is slightly higher than previous realizations at 2.5 GHz [1].

FBAR based on 740 nm-thick X-cut LiTaO₃ resonator displays resonance and antiresonance frequencies of respectively 1.58 and 1.70 GHz, leading to an electromechanical coupling coefficient of 17.4 % [2]. The quality factor at resonance and antiresonance are calculated to be 400 and 200, respectively. Moreover, the X-cut LiTaO₃ FBAR displays lower TCF values than those previously reported for LiNbO₃ FBAR [1], with measured temperature coefficients of the resonance and

antiresonance frequency of +16 and -42 ppm/K, respectively.

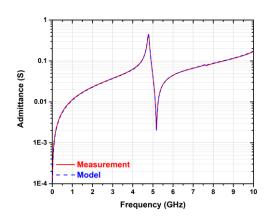


Figure 1: Typical response of a 4.8 GHz Y+163°-cut LiNbO₃ FBAR

Perspectives

These results demonstrate a first step towards introducing single crystals LiNbO_3 and LiTaO_3 films as an alternative to AIN for next generation of wideband RF filters. Future works will be devoted to further improve performances, especially quality factors and TCF values.

RELATED PUBLICATIONS:

[1] M. Bousquet et al., IEEE International Ultrasonics Symposium (2020), https://doi.org/10.1109/IUS46767.2020.9251654 [2] M. Bousquet et al., IEEE International Ultrasonics Symposium (2020), https://doi.org/10.1109/IUS46767.2020.9251463

Optomechanical mass sensing

RESEARCH TOPIC:

MEMS/NEMS, mass sensors, resonators, optomechanics

AUTHORS:

M. Sansa, A. Brenac¹, M. Gely, C. Masselon¹, I. Favero², H.E. Dawale, L. Sibeud, F. Badets, G. Jourdan, S. Hentz

Nanomechanical mass spectrometry is well suited for the analysis of high mass species such as viruses. Beams or cantilevers used so far force a trade-off between analysis time (related to capture area) and mass resolution (related to device mass). Such devices also require complex readout schemes and hinder the analysis of a large variety of species. We have demonstrated mass spectrometry with nano-optomechanical resonators fabricated with a Very Large Scale Integration process. Our device is impervious to particle position, stiffness or aspect ratio, allowing the analysis of objects such as viruses with a tail or fibrils. Compared to electrical read-out, we show a three-fold improvement in capture area with no resolution degradation.

SCIENTIFIC COLLABORATIONS: ¹ CEA IRIG, ² Université de Paris, laboratoire Matériaux et Phénomènes Quantiques

Context and Challenges

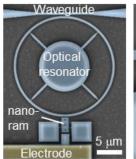
Nanomechanical mass spectrometry relies on one-dimensional devices, which forces a trade-off between analysis time and mass resolution, and requires complex readout in particular when stiffness or shape come into play. These issues restrict nanomechanical MS to the analysis of species with specific properties.

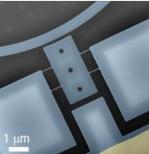
Main Results

We performed mass spectrometry with a resonator that is by design insensitive to landing position, stiffness, size, or shape. It embeds a platform that vibrates in-plane, providing large capture area. Obtaining excellent mass resolution is extremely difficult with electrical transductions for such thin devices and we used here on-chip cavity-based optomechanical resonators. They were fabricated with the first Very Large Scale Integration fabrication process for optomechanics, on 200 mm wafers and designed with a compact analytical model implemented in Verilog A. We have performed analysis of tantalum nanoclusters ranging from 2.8 to 7.7 MDa in less than 5 minutes.

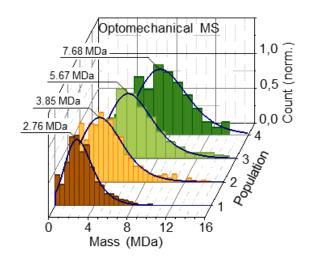
Perspectives

Our demonstration paves the way to high-throughput MS analysis of nanoparticles with any possible geometry. Devices with orders of magnitude better resolution are in reach of optomechanical read-out. Such devices would open new applications in structural biology and nano-characterization such as the analysis of amyloid fibrils involved in neurodegenerative diseases, or tailed viruses used for phagotherapy, promising alternative standard to antibiotherapy.





Our nano-optomechanical mass sensor



Tantalum nanoparticle mass spectra

- [1] M. Sansa et al., Nature Communications, 2020, http://doi.org/10.1038/s41467-020-17592-9
 [2] H.E. Dawale et al., IEEE Transactions on Electron Devices, 2020, http://doi.org/10.1109/TED.2020.3024477
- [3] H.E. Dawale et al., IEEE 33rd International Conference on Micro Electro Mechanical Systems, 2020, http://doi.org/10.1109/MEMS46641.2020.9056258

Magnetically actuated nanostructures for biotechnologies: examples of cancer cells destruction and inhibition of bacterial biofilms formation



RESEARCH TOPIC:

magnetic nanoparticles, nanofabrication, magnetic actuation, biomechanics

AUTHORS:

B Dieny¹, R Morel¹, S Sabon¹, C Naud¹, M Carrière², Y Hou², F Berger³, S Leulmi-Pichot⁴, R Cowburn⁴, LM Cursaru⁵, **H Joisten**

Magnetic anisotropic particles offer a unique way to exert local forces and torques on biological species (e.g. living cells), and study their reaction to the induced stress. A particularly interesting application studied at SPINTEC is the destruction of cancer cells and tumors thanks to the low-frequency vibration of magnetic particles under oscillating applied magnetic field [1]. In-vitro and in-vivo experiments demonstrated the potential of this method towards cancer treatment. Besides, arrays of magnetic micronic cantilevers have been studied as cilia for magnetic field mapping. Recently, in collaboration with Cambridge Univ., we demonstrated that vibrating arrays of such cilia could be used to prevent biofilms formation in microfluidic channels [2].

SCIENTIFIC COLLABORATIONS: ¹SPINTEC, CEA, CNRS, UGA, ²IRIG-SyMMES, CEA, CNRS, UGA, ³BrainTech Lab-INSERM, UGA, ⁴Cambridge University (UK), ⁵NCDMNR-IMNR (Romania).

Context and Challenges

Magnetic nanoparticles are widely used in biotechnology, for their ability to be remotely excited by external magnetic field and to interact with targeted entities, for applications such as cancer cells destruction, cells stimulation, bacteria or viruses screening. While superparamagnetic particles have been used for decades [3], the emergence of new types of magnetic anisotropic particles led to new magnetomechanical approaches for biotechnologies and potential therapies [1-2].

Main Results

Particularly remarkable is the triggering of cancer cells death (apoptosis) through the mechanical vibrations of magnetic particles (ex.NiFe disks) at low frequency (~20Hz), preserving neighboring healthy cells. The vibrations are remotely induced by an oscillating external magnetic field (a few mT) without heat production. Our recent review [1] analyses the in-vitro and invivo studies conducted in this field, in particular the physical and biological aspects of cells/particles interactions (figure 1). Furthermore, mechanical vibration of remotely actuated magnetic cantilevers arrays - dynamic surfaces - can reduce by up to 70% bacterial biofilms formation (Coll. Cambridge Univ [2], figure 2).

Perspectives

The physiological reactions of living cells to mechanical stress largely remains to be explored and understood. This is particularly true for stem cells and cancer cells. Magnetically actuated particles are particularly suited for experimental studies in this field.

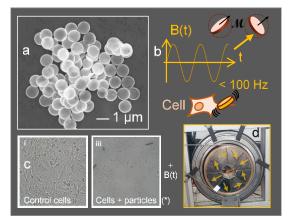


Figure 1: Magnetic disks on cancer cells

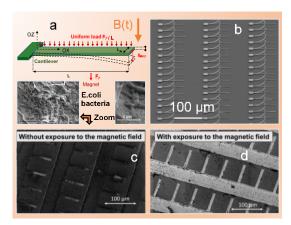
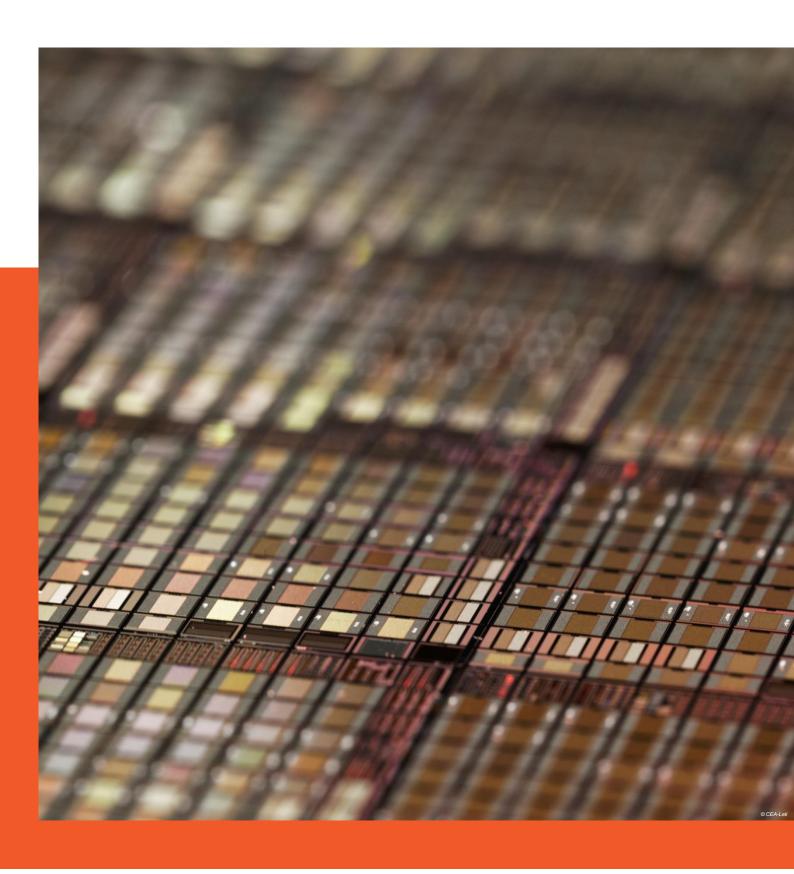


Figure 2: Magnetic cantilevers actuation on E. Coli biofilm

- [1] C. Naud et al., Nanoscale Advances, 2020, 2, 3632, https://doi.org/10.1039/d0na00187b
- [3] S. Leulmi-Pichot et al., Scientific Reports, 2020,10:15470, https://doi.org/10.1038/s41598-020-72406-8 [2] LM Cursaru et al., Nanomaterials 2020,10(8), 1500, https://doi.org/10.3390/nano10081500



05

POWER & ENERGY

- Advances in electrical characterization of gate oxide interface quality and threshold voltage instabilities in GaNon-Si E-mode MOSc-HEMTs
- Simulation and compact modeling of AlGaN/GaN heterostructure device for IC applications optomechanical mass sensing
- Recent progress on diamond thin film transfer by Smart Cut[™]
- Solid-state ionic capacitors for on-chip power storage
- Electrically tuned power extraction strategies for efficient and robust vibration energy harvesting systems

Advances in electrical characterization of gate oxide interface quality and threshold voltage instabilities in GaN-on-Si E-mode MOSc-HEMTs

RESEARCH TOPIC:

GaN-on-Si, MOSc HEMT, MOS channel HEMT, BTI, Vth instabilities, Dit extraction, Interface quality

AUTHORS:

W. Vandendaele, A.G. Viey, M.-A. Jaud, S. Martin, R. Modica¹, F. lucolano¹, G. Ghibaudo², G. Meneghesso³, R. Gwoziecki

CEA-Leti and ST Microelectronics are cooperating on GaN-on-Si technology development targeting the industrialization of Power HEMTs and Diodes for high efficiency power conversion. The E-mode MOSc-HEMT architecture is developed as a Normally-Off device addressing both the reduction of gate leakage and the increase of transistor lifetime. Being based on a MOS stack, it is mandatory to assess the intrinsic quality of the Oxide/GaN interface as well as to understand the Vth instabilities under positive gate bias (pBTI). This year recent breakthrough enabled the accurate Al₂O₃/GaN interface trap density (Dit) measurement. In addition, we evidenced a multi-factorial pBTI degradation mechanism combining epitaxial C_N acceptor traps ionization and electrons trapping in Al₂O₃.

SCIENTIFIC COLLABORATIONS: 1 ST Microelectronics, Catania, Italy; 2 IMEP-LAHC Minatec, Grenoble, France; 3 University of Padova, Padova, Italy

Context and Challenges

GaN-on-Silicon HEMT technologies drag significant attention for low-cost medium power applications (< 2kW) due to GaN high breakdown electric field and excellent AlGaN/GaN 2DEG transport properties. To ensure user safety normally-off devices (Vth > 0V) are required for power switching applications. CEA-Leti targets this feature developing MOSc-HEMT architecture. The MOS configuration brings outstanding insulation properties as well as excellent electrostatic behavior. However, recent BTI studies suggest significant Vth instabilities, which would severely affect the dynamic performances of the device. Deep assessment of the Al₂O₃/GaN interface quality and advanced characterization of the interface traps density of MOS are then mandatory.

Main Results

Through standard temperature dependent measurements (Capacitance-Conductance-Voltage) performed at Al₂O₃/UID-GaN interface, we proved that the 2D elements of the gate (sidewalls, corners and bottom), combined with high resistivity of the UID-GaN layer, induce a delay in the ac signal propagation towards the middle of the gate. This delay artificially increases the conductance peak leading to overestimation of the extracted Dit. Using planar structures, an accurate Dit extraction was developed (Figure 1) [1] opening the way to process optimization. Interface quality apart, the gate oxide (Al₂O₃) is the core of the MOSc-HEMT technology and we have pointed out this year that pBTI is a combination of C_N acceptors in the GaN:C buried layer (G1) and of Al₂O₃ defects (G2) (Figure 2) [2, 3].

Perspectives

Our interface trap density (Dit) extraction procedure has now to be validated on n-GaN recessed gate 2D structures and the particular impact of sidewalls and corners of the gate has also to be investigated. Al₂O₃ defects causing the major part of the Vth instabilities, the pBTI studies will be completed by physical and chemical characterization.

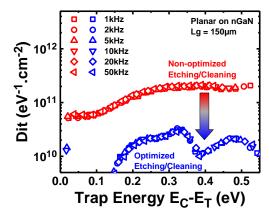


Figure 1: Extracted Dit=f(E_C-E_T) on planar n-GaN capacitors for two etching/cleaning processes.

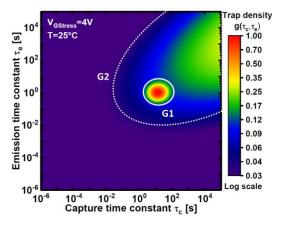


Figure 2: CET Map illustrating 2 trap populations

- [1] W. Vandendaele et al., IEEE International Electron Devices Meeting (IEDM), 2020, https://doi.org/10.1109/IEDM13553.2020.9371965
 [2] A.G. Viey et al., IEEE International Electron Devices Meeting (IEDM), 2020, https://doi.org/10.1109/IEDM13553.2020.9371938
 [3] A.G. Viey et al., IEEE Transaction on Electron Devices, 2021, https://doi.org/10.1109/IED.2021.3050127

Simulation and compact modeling of AlGaN/GaN heterostructure device for IC applications

RESEARCH TOPIC:

Power device, GaN-on-Si, HEMT, Hybrid anode diodes, TCAD, compact model, SPICE

AUTHORS:

S. Martinie, M.-A. Jaud, A. Vaysset, G. Atmaca, F. Triozon, J. Buckley

For several years, CEA-Leti has been actively working on the development and industrialization of an advanced GaN-on-Silicon technology including diodes and transistors for medium power applications (650V and below). In this context, the simulation of the AlGaN/GaN heterostructure in various configurations is one of the main challenge for devices optimization but also to provide the compact models for circuits design. In a collaboration with STMicroelectronics and thanks to TCAD simulations, CEA-Leti has investigated a lateral diode concept to demonstrate surge current capability. Moreover, in collaboration with Silvaco a Verilog-A compact model of heterojunction transistor based on the surface potential approach was developed.

SCIENTIFIC COLLABORATIONS: STMicroelectronics, Silvaco

Context and Challenges

AlGaN/GaN based High-Electron-Mobility Transistor (HEMT) transistors and diodes are a promising candidate for high frequency and high power applications. Modeling and simulation of these devices are consequently of great interest to optimize the device performances and to design circuit.

Main Results

In an Hybrid Anode Diode (HAD) concept (Figure 1a), TCAD simulations evidence that hole injection can occur at pGaN metallic anode and results in an increase of the hole density pGaN/AlGaN interface. To preserve electrostatic equilibrium, additional electrons are thus accumulated in the GaN channel and leads to surge current [1]. This surge current is more likely to occur in the case of an ohmic pGaN anode contact and a highly doped pGaN layer (Figure 1b). Concerning development of compact models for circuit design, an approach similar to MOS models to describe HEMT AlGaN/GaN heterojunction is proposed [2]. First, the Poisson equation is solved classically, using Boltzmann statistics. Then, quantum confinement is added as an effective bandgap widening (triangular-well approximation). The resulting surface potential equation is validated by comparison with Poisson-Schrödinger solver (Figure 2) and is similar to the one used in MOS compact models (such as the standard model PSP or L-UTSOI, supported by CEA-Leti for the CMC). Therefore, current, charge and other features can be readily implemented with proven methods.

Perspectives

Concerning HAD, because Ohmic contact on p-GaN have been recently demonstrated to be possible in literature, our work can pave the way to the use of conductivity modulation to obtain surge current capability in lateral power diodes.

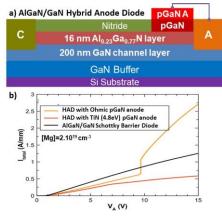


Figure 1: a) HAD structure b) Current curves

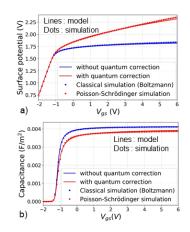


Figure 2: a) Surface potential b) Capacitance

RELATED PUBLICATIONS:

[1] G. Atmaca et al., International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2020, https://doi.org/10.23919/SISPAD49475.2020.9241673 [2] A. Vaysset et al., International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2020, https://doi.org/10.23919/SISPAD49475.2020.9241679

Recent progress on diamond thin film transfer by Smart CutTM

RESEARCH TOPIC:

Diamond, Smart Cut^{TM} , Power electronics, Wide band gap semiconductors

AUTHORS:

C. Masante, J. De Vecchy, J. Widiez, F. Milesi, F. Mazen, F. Servant, L. Le Van-Jodin

The main constraint for using diamond substrate to make power devices is the monocrystalline substrate size limited to 1 cm². Transfer of diamond thin films by the Smart Cut™ technology is studied as an innovative solution to realize wafer scaled diamond substrates, by paving a wafer with diamond thin films. To this end, the succession of two hydrogen implantations and annealing is demonstrated to produce significant surface blistering, a major step toward the first diamond transfer.

SCIENTIFIC COLLABORATIONS: Institut Néel (CNRS), DiamFab, SOITEC

Context and Challenges

Diamond is an up-and-coming semiconductor for next generation power devices due to its wide gap and its excellent conductivity. However. electronic monocrystalline diamond substrates are only available in small size, in the order of a few mm2 to 1 cm2. One solution to achieve larger substrates is to pave a wafer-scale substrate with thin diamond films sliced from small diamond substrates. One of the most efficient method to achieve such process is the Smart Cut™, relying mostly on implantation, bonding and thermal splitting to transfer thin films. Controlling the implantation, bonding and annealing conditions leading to splitting is key for the transfer. This work presents successful splitting conditions, observed as surface blistering in the absence of a receiving substrate, the first main step to develop a Smart Cut™ process.

Main Results

 $H^{\scriptscriptstyle +}$ ions were implanted in a 4x4x0.5 mm $^{\scriptscriptstyle 3}$ IIa diamond plates then annealed at 1000°C during 1 hour in high vacuum. No surface blistering was observed at this point due to the extremely slow diffusion coefficient of hydrogen in diamond. However a damaged amorphous layer in the implanted region is clearly evidenced by EELS and HR-STEM [1]. A second H+ implantation at a higher dose, followed by a second annealing led this time to significant blistering of the surface [2]. STEM images clearly show the presence of nanometric bubbles in the implanted damaged layer [2], that eventually led to the macroscopic blistering observed when they coalesce. The transition between the amorphous and crystalline layers is sharp, around 20 nm thick. This suggests that the annealing successfully healed the implantation induced damage, below a defect density threshold yet to be determined. This strongly suggests that the implanted hydrogen can only diffuse in a preamorphized diamond layer, in this case obtained with the first implantation and annealing.

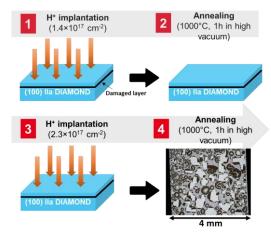


Figure 1: Implantation and annealing conditions

Perspectives

This 4 steps implantation and annealing process leads to the successful splitting of a thin diamond layer. The next step toward the diamond SmartCut™ demonstration is to achieve diamond wafer bonding. An adequate receiving substrate must be found, compatible with the high temperature splitting annealing. Additionally, the control of the surface roughness and flatness is key to enhance the bonding interface strength, which is challenging on small square-shaped plates.

- [1] J.C. Piñero et al., Applied Surface Science, (2020), https://doi.org/10.1016/j.apsusc.2020.146998
- [2] J. De Vecchy. Micro et nanotechnologies/Microelectronique. Université Grenoble Alpes, 2020. Français. (NNT: 2020GRALT022).

Solid-state ionic capacitors for on-chip power storage



RESEARCH TOPIC:

Thin film, ionic capacitors, on-chip power storage, solid state

AUTHORS:

V. Sallaz^{1,2}, F. Voiron¹, S. Poulet², M. Bedjaoui², Raphaël Salot², Sami Oukassi²

CEA-Leti's work on miniaturized power-storage involves optimization of numerous elements in order to improve performance. Last year we developed a high power density solid ionic capacitor integrating 15nm inorganic LiPON electrolyte. We demonstrate an areal capacitance density of 100 µF cm⁻² at scan rates below 100 V s⁻¹ among the highest reported so far for such devices. Further 3D extrapolations highlight the strong potential of solid ion capacitors to be used as on-chip integrated power storage units.

SCIENTIFIC COLLABORATIONS: 1 Murata Integrated Passive Solutions, 2 CEA-Leti

Context and Challenges

The continued miniaturization of electronics has asserted the need for highly integrated energy storage devices. On-chip energy storage can reduce dissipation from power loss and I/O switching noise. Micro-supercapacitors (MSC) are one of the main solutions to address this need, especially known for their high power densities and excellent cycling stability. However the most common solution relies on polymer electrolytes leading to low operating voltage (about 1V) and poor cycle life.

Main Results

Metal-Ion conductor-Metal structures using blocking electrodes have been used to investigate the areal capacity variation with LiPON ionic conductivity, electrochemical kinetics, and the potential window. The fabricated devices exhibit typical capacitance values as high as 100 µF cm⁻² at scan rates below 100 V s⁻¹ over 10⁵ cycles and a high nominal voltage of 3 V. The voltammetry results indicate that the storage mechanism consists in Li-ion accumulation at the electrode/electrolyte interfaces, as expected from typical double layer capacitors. These results highlight the potential of an integrated LiPON for micro-supercapacitors. The Li:P ratio around 3 in LiPON chemical composition allows for the electrolyte to have a good balance between its mobile charge carriers concentration and ionic mobility, and consequently leading to higher energy and power densities, respectively.

Perspectives

For further developments, the use of ALD thin layers would permit to consider MSC structures with large aspect ratio for enhanced electrical performance. A projection considering an amplification factor of x250 (Figure 1) would bring exceptionally high energy and power densities of 17 $\mu\text{Wh.cm}^{-2}$ and 1.7 W cm⁻² respectively. This projection is based on a threedimensional structuring of the device architecture on the one hand, and an improvement in the quality of the electrode/ion conductor/electrode stack (conformality, intrinsic properties of ionic / electronic conduction) on the other hand. The process compatibility with silicon and the choice of low-cost metal electrodes would make it particularly viable for an industrial large-scale production.

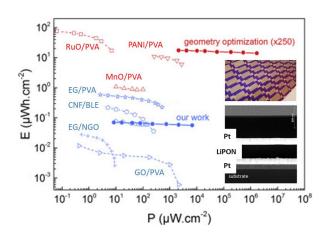


Figure 1: MSC areal energy density vs areal power density (filled symbols) in comparison with all-solid-state thin film MSCs (open symbols) considering planar (blue) and 3D architectures (red). Inset: MSC optical image (top) and SEM cross-section (bottom)

- [1] V. Sallaz et al., ECS Meeting Abstracts, 2019, https://doi.org/10.1149/ma2019-02/3/161. [2] V. Sallaz et al., J. Power Sources, vol. 451, 2020, https://doi.org/10.1016/j.jpowsour.2020.227786

Electrically tuned power extraction strategies for efficient and robust vibration energy harvesting systems

RESEARCH TOPIC:

Vibration, energy harvesting, piezoelectric resonators, electromagnetic harvesters, integrated circuits, electrically tuned power extraction.

AUTHORS:

A. Morel, A. Quelen, D. Gibus, C. Berlitz, P. Gasnier, S. Boisseau, A. Badel¹, G. Pillonnet

We have explored alternative electrical harvesting strategies to maximize the energy extraction capability of vibrating electromechanical energy harvesters. First, using the inverse piezoelectric effect, we have proposed an emerging technique able to enlarge the narrow bandwidth piezoelectric harvesters by +/- 10 %. From analytical derivations, we have demonstrated the ability of this electrical strategy to dynamically adjust the quality factor and resonance frequency of electromechanical generators. The proposed approach was implemented in a self-powered and self-adjusted integrated circuit. Using the one-cycle sense and react technique a 10x improvement of the energy extracted was demonstrated for an electromagnetic generator subjected to shocks.

SCIENTIFIC COLLABORATIONS: 1 SYMME, Université Savoie-Mont Blanc, Annecy (FR)

Context and Challenges

Ambient vibrations energy harvesting systems suffer from low robustness with respect to electromechanical transducers shifts (aging, temperature, process) or to slight variations of the vibrations frequency, limiting the widespread deployment of vibration energy scavenging systems. To overcome their inherent low robustness, we explore different techniques to improve the robustness of resonance-based harvesters considering piezoelectric and electromagnetic couplings.

Main Results

Piezoelectric harvesters

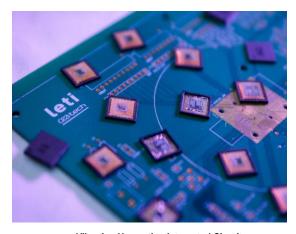
We have explored the dynamical tuning of the damping and stiffness induced by the electrical interface through the electromechanical piezoelectric coupling. Controlling the energy-harvesting phase, the electrical interface impacts the mechanical resonator and its resonance frequency. We have analytically derived the influences of electrical interface by introducing and tuning new harvesting phases based on the SECE technique [3]. Thereafter, we have evaluated a selfpowered and self-adjusted integrated circuit embedding various tunable-SECE approaches [4]. The presented IC is based on a 7-bits self-adjusted Phase-shifted Synchronous Electrical Charge Extraction (PSECE) strategy, including a real-time harvested power measurement to continuously track the maximum harvested power point (MPPT). With this implementation we have demonstrated a self-adjusted 3dBbandwidth around the resonance frequency (56 Hz+/-5Hz) leading to 454% bandwidth extension, with up to 94% conversion-efficiency at low acceleration levels (0.08 g) [1].

• Electromagnetic harvesters

To enhance the power extraction from electromagnetic generators (EMH), the harvesting ICs (HIC) suffer from costly bill of materials (BoM) compared to a low-efficiency, but still low-cost, widely adopted passive harvesting technique. Against this background, we proposed an HIC which exploits the inductive nature of the EHM and which implement sharing use strategy of storage element to drastically reduce the BoM. Moreover, to exploit the entire EMH's mechanical-to-electrical transduction capability, and to reduce the EMH size and weight, we demonstrated the ability of our HIC to ensure MPPT in the µs-range by dynamically measuring the input impedance and adjusting to the EMH conditions leading to high end-to-end efficiencies at sub-g acceleration. The presented HIC has the highest tracking frequency reported and was demonstrated to be highly adaptable to the environmental vibrations variations or oscillations decay after shocks without adding any additional external sensors nor needing to average the sensing over few periods, nor disconnecting the harvester [2].

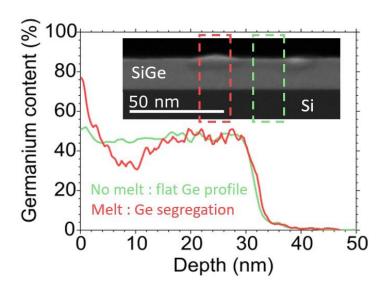
Perspectives

The next step is to translate the piezo-based tuning harvesting strategies to other electromechanical transductions. Other applications could benefit from the tunable frequency approach e.g. wireless energy transfer or M/NEMS-based resonant sensors.

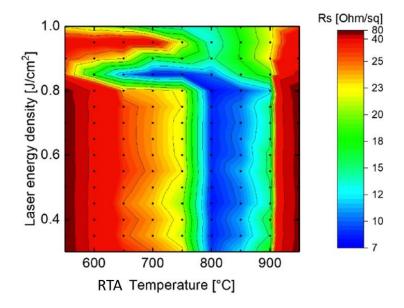


Vibration Harvesting Integrated Circuit

- [1] A. Morel et al., IEEE International Solid-State Circuits Conference (ISSCC), 2020, https://doi.org/10.1109/ISSCC19947.2020.9062972
- [2] A. Quelen et al., IEEE International Solid-State Circuits Conference (ISSCC), 2020, https://doi.org/10.1109/ISSCC19947.2020.9063023
- [3] D. Gibus et al., Applied Energy, 2020, https://doi.org/10.1016/j.apenergy.2020.115518
 [4] A. Morel et al., IEEE European Solid-State Circuits Conference (ESSIRC), 2020, https://doi.org/10.1109/LSSC.2020.3012340



Molten islands on the surface of a $Si_{0.6}Ge_{0.4}$ film after Nanosecond Laser Annealing



Sheet resistance of Si/Ti/TiN samples after Nanosecond Laser Annealing then Rapid Thermal Annealing

06

EMERGING PROCESSES AND DEVICES

- From direct bonding mechanism to applications
- Advanced chalcogenide materials for memory applications
- Advanced chalcogenide materials for optics and photonics
- Low temperature epitaxial growth and in-situ doping of group-IV semiconductors for photonics
- Advanced contacts on GeSn and III-V materials for photonics
- Advanced nanosecond laser annealing for nanoelectronics
- Advanced SiGe process modules for nanoelectronics

From direct bonding mechanisms to applications

RESEARCH TOPIC:

Direct bonding, anhydrous bonding energy, DEAE, Silicon, Silicon dioxide, ultra-thin silicon film, 3D applications, Smart Cut.

AUTHORS:

T. Tabata, L.G. Michaud, W. Schwarzenbach¹, V. Larrey and F. Fournel

Recently, a new surface preparation for direct bonding has been discovered. The addition of diethylethanolamine (DEAE) prior to bonding drastically increased the direct bonding energy in the low temperature, post bonding annealing domain (e.g. less than 500°C). DEAE seemed to enhance the silicon dioxide hydrolysis at the bonding interface by the trapped water. At the same time, a detrimental water behavior for the direct bonding energy was evidenced in another fundamental study. Those results highlight the complexity of direct bonding. Knowing it accurately enables to identify novel applications. Ultra-thin silicon films on flexible substrates or front-end devices could then be obtained for innovative 3D applications.

SCIENTIFIC COLLABORATIONS: SOITEC, Parc Technologique des Fontaines - F-38190 Bernin - France

Context and Challenges

Fundamental and applicative direct bonding studies were performed simultaneously in order to increase our understanding and fabricate innovative structures for 3D applications, for instance. Recently, two studies related to the direct bonding energy enabled us to increase our knowledge on direct bonding mechanisms. Two ultra-thin (<200 nm) silicon films were obtained and transferred on different substrates.

Main Results

Despite the fact that organic surface contamination has to be avoided for direct bonding, the addition of diethylethanolamine (DEAE) prior to bonding drastically increased the direct bonding energy in the low temperature, post bonding annealing domain (e.g. less than 500°C) (cf. Figure 1) [1]. DEAE seemed to enhance the silicon dioxide hydrolysis at the bonding interface by trapped water. At the same time, the direct bonding energy was reduced by water after the post bonding annealing. Indeed, for a low annealing temperature (200°C), water can penetrate at the bonding interface and corrode the silicon oxide bridges between the bonded surfaces [2]. Those results highlight the complexity of direct bonding but help to accurately control it. This enabled us to fabricate ultra-thin (<200 nm) silicon films on flexible substrates (cf. Figure 2) [3] or CMOS devices for 3D applications [4].

Perspectives

DEAE exciting results will result in a wide evaluation of organic molecules and their impact on direct bonding.

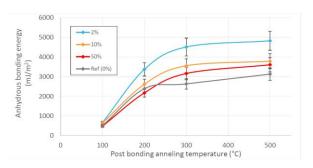


Figure 1: Anhydrous direct bonding evolution with different DEAE



Figure 2: 200 nm ultra-thin silicon film transfer to a flexible substrate [3].

- [1] F. Fournel et al., ECS Transactions 98 (4), 3 (2020); https://doi.org/10.1149/09804.0003ecst.
 [2] T. Tabata et al., Microelectronics Reliability 107, 113589 (2020); https://doi.org/10.1016/j.microrel.2020.113589.
 [3] L.G. Michaud, et al., Nanotechnology 31, 145302 (2020); https://doi.org/10.1088/1361-6528/ab647a.
 [4] W. Schwarzenbach et al., ECS Transactions 97 (5), 129 (2020); https://doi.org/10.1149/09705.0129ecst

Advanced chalcogenide materials for memory applications



RESEARCH TOPIC:

Chalcogenides, van der Waals, metavalent bonding, superlattice, phase-change memories, automotive applications

AUTHORS:

M. Tomelleri, D. Térébénec, V. Sever, N. Bernier, T. Farjot, C. Sabbione, F. d'Acapito¹, F. Hippert², J.-Y. Raty and **P. Noé**

Chalcogenide phase-change materials (PCMs) recently enabled a breakthrough in the field of memories, with a 3D cross-point architecture. The physics behind this success is related to "metavalent bonds" (MVBs) appearing in their crystalline phase. We showed that introducing a few MVBs within a covalent chalcogenide glass permits to obtain a new type of PCM extremely promising for memory devices requiring a very high data retention for automotive and embedded applications. Besides, the van der Waals growth of GeTe/Sb₂Te₃ super-lattices is key to further improve PCM memory performances. In 2020, we unveiled their local atomic structure and demonstrated how to master their growth on various substrates, further extending their application fields.

SCIENTIFIC COLLABORATIONS: ¹IOM-OGG, CNR, LISA beamline c/o ESRF, Grenoble. ²LMGP, Grenoble-Alpes Univ. *FRS-FNRS, Liège Univ., Belgium/CEA-Leti.

Context and Challenges

Despite their recent commercialization, PCM memories still face technological limitations. GeTe/Sb2Te3 super-lattices (SLs) were shown to exhibit improved performances compared to standard Ge-Sb-Te polycrystalline PCM thin films used in commercial memory devices. For embedded applications, the integrity of the code must be guaranteed at high temperature (10 years at 150°C and a few minutes at 260°C). Integrity is directly related to the thermal stability of the amorphous phase of PCMs against unwanted crystallization. Until now, no PCM based on a single compound was able to meet this challenge.

Main Results

The origin of the improved performance of SLs devices is still unknown. This is mainly due to a lack of structural description at the atomic scale. We evidenced their atomic structure by means of X-ray Absorption Spectroscopy coupled with modern ab initio molecular dynamic simulations [1]. These SLs rely on the van der Waals growth of Sb₂Te₃ pseudo-2D layers. We investigated the growth mechanism of Sb₂Te₃ layers (**Figure 1**) and demonstrated that SLs can be successfully grown on various types of substrates [2]. Finally, we showed that some specific GeSe1-xTex alloys can meet the requirements of embedded memories, with a stability reaching ~270°C for 10 years (**Figure 2**) [3].

Perspectives

Merging our unique knowledge and know-how on chalcogenide materials will enable on-demand design of new PCMs with tailored properties for future applications.

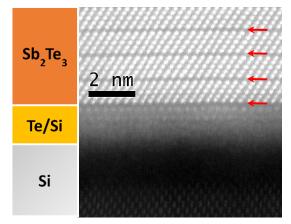


Figure 1: HRTEM image of 2D Sb_2Te_3 on Si. Red arrows show Te-Te vdW gaps

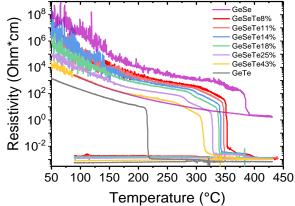


Figure 2: Novel GeSe $_{1-x}$ Te $_x$ PCM thin films with a high T $_{cryst}$ reaching ~350°C and an unprecedented resistance contrast

RELATED PUBLICATIONS:

[1] F. d'Acapito, P. Kowalczyk, J.-Y. Raty, C. Sabbione, F. Hippert and P. Noé, J. Phys. D: Appl. Phys. 53, 404002 (2020). https://doi.org/10.1088/1361-6463/ab98c1 [2] F. Hippert, P. Kowalczyk, N. Bernier, C. Sabbione, X. Zucchi, D. Térébénec, C. Mocuta and P. Noé, J. Phys. D: Appl. Phys. 53, 154003 (2020). https://doi.org/10.1088/1361-6463/ab6b98

https://doi.org/10.1088/1361-6463/ab6b9a
[3] M. Tomelleri, F. Hippert, T. Farjot, C. Licitra, N. Vaxelaire, J.-B. Dory, D. Benoit, V. Giordano and P. Noé, Physica Status Solidi (RRL) – Rapid Research Letters 2000451 (2020). https://doi.org/10.1002/pssr.202000451

Advanced chalcogenide materials for optics and photonics

RESEARCH TOPIC:

Chalcogenide, Mid-Infra-Red, photonics, optical nonlinearity, glass, metavalent bonding, fingerprinting

AUTHORS:

J.-B. Dory, P. Martinez, A. Verdy, M. Tessaire, M. Bernard, J.-B. Jager¹, J. Gaudin², J.-Y. Raty^{*}, B. Cluzel³ and **P. Noé**

Owing to a unique properties portfolio, chalcogenides offer tremendous applications ranging from memory to thermoelectric, optical and modern photonic devices. Improving further their properties is still possible thanks to ongoing progress in the understanding of their physical properties. We showed that the right tailoring of the amorphous structure of Ge-Sb-S-Se-Te-based glassy thin films expanded the application domain of on-chip nonlinear Mid-IR devices. Through a basic study of ultrafast physical mechanism upon laser pulses-matter interaction, we otherwise demonstrated a straightforward way to generate PUF (Physical Unclonable Functions) tags on the surface of an amorphous GeTe film, the latter being well adapted for anti-counterfeiting applications.

SCIENTIFIC COLLABORATIONS: 1CEA, IRIG, Grenoble. 2CELIA, Univ. Bordeaux, Talence. FRS-FNRS, Liège Univ., Belgium/CEA-Leti. ³ICB, Univ. de Bourgogne-Franche-Comté, Dijon.

Context and Challenges

Some chalcogenides are suitable for use in photonics or optical sensors operating in the near- and mid-Infra-Red. Combining the wide IR transparency of S-based glasses as well as the huge optical nonlinearities of Te-based ones is a challenge, however. The high sensitivity at ultrashort timescale of chalcogenides to high electrical field enables phase-change and ovonic threshold switching (OTS) applications. Hence, studying their response to ultrashort laser pulses application is key to explore the physical mechanisms at play.

Main Results

Through the right tailoring of the local atomic order of GeSbwSxSeyTez glassy films, an unprecedented trade-off between a good transparency in the MIR, a strong nonlinearity (Figure 1) and a good thermal stability was found, which is promising for innovative nonlinear photonic devices [1]. Moreover, we demonstrated a versatile method to generate random patterns on the surface of amorphous Ge-Sb-Te-based films using laser/matter interaction [2-3]. The periodicity of these surface wrinkles patterns are suited for use as PUF-tags (Figure 2). This paves the way to straightforward nondeterministic PUF-tag generation dedicated to small sensitive parts such as, for example, electronic devices/components, jewelry or watchmaking.

Perspectives

Modeling of amorphous chalcogenides as well as ps-timescale light-matter interaction by means of AIMD/DFT simulations should yield a better understanding of their outstanding properties

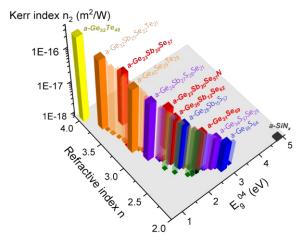


Figure 1: Nonlinear (Kerr) vs linear refractive index and optical bandgap of Te-, Se- and S-based amorphous chalcogenides

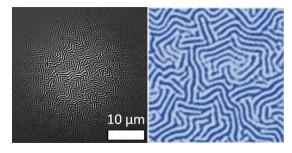


Figure 2: Optical images of PUF-tag made of a random wrinkle pattern obtained after laser pulse irradiation of a GeTe film capped with ultrathin SiN layer

- [1] J.-B. Dory et al., Scientific Reports 10, 11894 (2020). https://doi.org/10.1038/s41598-020-67377-9 [2] N. Fedorov, Review of Scientific Instruments 91, 105104 (2020). https://aip.scitation.org/doi/10.1063/5.0012485

Low temperature epitaxial growth and in-situ doping of group-IV semiconductors for photonics



RESEARCH TOPIC:

Very low temperature epitaxy, in-situ doping, GeSi and GeSn, Mid Infra-Red Photo-Detectors and Light Emitting Diodes

AUTHORS:

M. Frauenrath, J. Richy, E. Nolot, M. Veillerot and J.-M. Hartmann

We have explored (i) the 300°C − 350°C epitaxy of GeSn with GeH₄ or Ge₂H₆ as the Ge precursor and SnCl₄ as the Sn precursor, (ii) the in-situ doping, at 350°C, of pure Ge with B and of GeSn with B or P and (iii) the feasibility of growing, at those temperatures, GeSi alloys for use as barriers in GeSn / GeSi heterostructures. Thanks to those studies, we should be able to grow, on top on Ge Strain-Relaxed Buffers, pin stacks with in-situ doped Ge or low Sn content GeSn as p-type or n-type doped contacts and high Sn content GeSi / GeSn multi quantum-wells as the optically active parts of the heterostructures. Our aim is to fabricate, in the near future, mid infra-red photodetectors, light emitting diodes and, ultimately, lasers.

Context and Challenges

We would like to grow, on top on Ge Strain-Relaxed Buffers, pin stacks with (i) in-situ doped Ge or GeSn as contacts and (ii) high Sn content GeSi / GeSn multi quantum-wells as the optically active parts of the heterostructures. Our aim is to fabricate mid infra-red photo-detectors, light emitting diodes and, ultimately, lasers. This is however far from being easy, as the solid solubility of Sn in Ge is low (1%), while we are interested in Sn contents 8% and more, to have direct bandgap materials. Growth temperatures should then be ultra-low, in the 300°C – 350°C range, to avoid Sn precipitation / segregation.

Main Results

We have first of all explored the 300°C - 350°C epitaxy of GeSn with GeH4 or Ge2H6 as the Ge precursor and SnCl4 as the Sn precursor (see Figure 1). GeH4 yielded similar GeSn growth rates but lower Sn contents than Ge₂H₆ and the thickness uniformity was worse [1]. We have also studied the 350°C in-situ doping of pure Ge [2] and low Sn content GeSn [3] with Ge_2H_6 , $SnCl_4$ and B_2H_6 or PH_3 . We succeeded in having B and P concentrations in the few 10¹⁹ cm⁻³ - 10²⁰ cm⁻³ range for both. Finally, we have investigated the impact of temperature on the properties of GeSi layers grown with Ge₂H₆ and SiH₂Cl₂ [4]. Meaningful Si contents (around 7.5%) and acceptable growth rates were obtained in the 325°C - 375°C range, but layers were islanded.

Perspectives

We will shortly use this know-how to fabricate pin structures for mid-IR optical purposes.

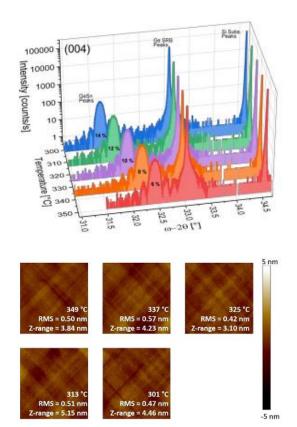


Figure 1: XRD profiles and AFM pictures for tens of nm thick GeSn layers grown at 301°C to 349°C on Ge Strain-Relaxed-Buffers.

- [1] J.M. Hartmann et al., ECS Transactions 98 (5), 225 (2020); https://iopscience.iop.org/article/10.1149/09805.0225ecst, J.M. Hartmann et al., ECS Transactions 98 (5), 203 (2020); https://iopscience.iop.org/article/10.1149/09805.0225ecst, M. Frauenrath et al., ECS Transactions 98 (5), 325 (2020); https://iopscience.iop.org/article/10.1149/09805.0325ecst.
- [4] J.M. Hartmann, Journal of Crystal Growth 546, 125789 (2020); https://doi.org/10.1016/j.jcrysgro.2020.125789

Advanced contacts on GeSn and III-V materials for photonics

RESEARCH TOPIC:

Contacts on GeSn, InP and InGaAs semiconductors for optoelectronics applications

AUTHORS:

A. Quintero, F. Boyer, P. Gergaud, J.M. Hartmann, V. Reboud, C. Jany, M. Grégoire¹, Q. Rafhay², E. Cassan³, **Ph. Rodriguez**

Performant contacts on GeSn and III-V semiconductors is of prime importance in optoelectronic devices. CEA-Leti has thus developed technological modules which are fully compatible with a Si fabrication line for the metallization of GeSn, InP and InGaAs. First of all, we have quantified the impact and behavior of Sn during the solid-state reaction of Ni thin films with GeSn, a low and potentially direct bandgap group-IV semiconductor. We have then developed CMOS-compatible ohmic contacts on n-type InP and p-type InGaAs III-V semiconductors in 200 and

SCIENTIFIC COLLABORATIONS: 1 STMicroelectronics, Crolles (FR) / 2 IMEP-LAHC, Grenoble (FR) / 3 C2N CNRS Université Paris-Saclay, Paris (FR)

Context and Challenges

Dedicated contact technologies on GeSn and III-V semiconductors are mandatory to fabricate optoelectronics devices in 200 and 300 mm Si fabrication lines. The physicochemical and electrical properties of systems such as Ni/GeSn and Ni or Ti on InP and InGaAs have then to be assessed to identify the best process conditions and trade-

Main Results

The role of Sn during the Ni/GeSn solid-state reaction (SSR) was investigated [1]. Results showed that Sn incorporated into the intermetallics during the Ni/GeSn SSR. Sn atoms accumulated around grain boundaries, reducing paths for Ni diffusion and delaying the monostanogermanide phase growth (Figure 1). When the temperature increased and the film agglomerated, Sn atoms migrated towards the top surface. The addition of alloying elements to the intermetallics was shown to delay agglomeration and Sn segregation [2]. This could be a solution for contacts on high Sn content GeSn

A CMOS-compatible contact technology was otherwise developed on n-InP and p-InGaAs for Si photonics [3]. Results obtained covered a wide scope: from surface preparation, solid-state reaction and metallization (Figure 2) to electrical properties and integration schemes. The use of Ti-based contacts resulted in contact resistivity and performance reliability in line with device requirements and long-term thermal stress constraints [4].

Perspectives

These material developments will be implemented on photonic devices.

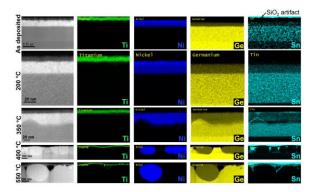


Figure 1: Cross-sectional TEM images of Ni/GeSn samples after various Rapid Thermal Anneals

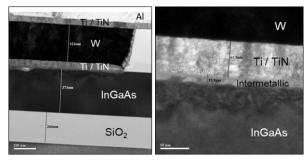


Figure 2: Cross-sectional TEM pictures ofthe Ti metallization of InGaAs in a device.

- [1] A. Quintero et al., Journal of Applied Crystallography **53**, 605 (2020), https://doi.org/10.1107/S1600576720003064
 [2] A. Quintero et al., Material Science in Semiconductor Processing **108**, 104890 (2020), https://doi.org/10.1016/j.mssp.2019.104890
 [3] Ph. Rodriguez et al., Japanese Journal of Applied Physics **59**, SL0801 (2020), https://doi.org/10.35848/1347-4065/ab7f1e
 [4] F. Boyer et al., IEEE Transactions on Electron Devices **67**, 2495 (2020), https://doi.org/10.1109/TED.2020.2985766

Advanced nanosecond laser annealing for nanoelectronics

RESEARCH TOPIC:

Nanosecond laser anneal, SiGe, surface melt, strain, segregation, contacts, C40-TiSi₂ formation into C54-TiSi₂

AUTHORS:

L. Dagault, L. Esposito, A.-S. Royer, P. Acosta-Alba, M. Grégoire¹, D. Mangelinck², F. Cristiano³ and S. Kerdilès

We investigated the structural modifications of SiGe epilayers and of Si/Ti/TiN stacks upon Nanosecond Laser Annealing (NLA) in a SCREEN LT-3100 platform. For each system, we carefully studied the influence of the laser energy density and the number of laser shots. For SiGe samples, test vehicles for the formation of ultra-shallow junctions, we focused on the surface morphology, the strain evolution and the Ge redistribution. For the Ti-based structures that emulated contacts for imagers, we explored the phase sequence when combining NLA and a rapid thermal annealing (RTA).

SCIENTIFIC COLLABORATIONS: ¹ STMicroelectronics, Crolles (FR), ² IM2NP, Marseille (FR), ³ LAAS, Toulouse (FR)

Context and Challenges

Nanosecond laser annealing is a technique which is particularly suitable for the fabrication of structures with thermal budget limitations, such as in 3D integration or advanced imagers. It should, for instance, enable the formation of innovative contacts and give access to ultra-high active dopant concentrations. Before any attempts at process integration, we have first to understand the various phenomena encountered when submitting doped semiconductors or contacts to NLA.

Main Results

We carefully investigated, on thin SiGe layers, the various regimes encountered when varying the laser energy density [1]. We evidenced the formation of isolated molten islands at the onset of fusion (Figure 1), the roughness of the melting front and the resulting strain relaxation when at least part of the SiGe layer remained solid during laser annealing. Optimal annealing conditions were those corresponding to the exact melt of the whole SiGe film, with a strong Ge redistribution well reproduced by numerical simulations [2].

Concerning the formation of Ti-based contacts [3], we demonstrated that NLA with the right process conditions used on a Si/Ti/TiN stack resulted in the formation of a C-40 TiSi₂ phase. A subsequent RTA yielded the low resistance C54-TiSi2 phase at a temperature as low as 650°C, instead of 800°C for a single RTA (Figure 2).

Perspectives

Strengthened by these findings, we will continue the work towards the integration of NLA into device fabrication flows.

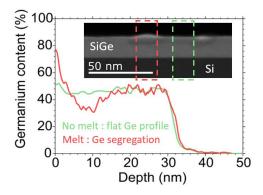


Figure 1: Molten islands at the surface of a Si_{0.6}Ge_{0.4} film after NLA (fusion onset)

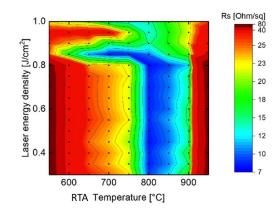


Figure 2: Sheet resistance of Si/Ti/TiN samples after NLA then RTA

RFI ATED PUBLICATIONS:

- [1] L. Dagault et al., Appl. Surf. Sci. 527, 146752 (2020), https://doi.org/10.1016/j.apsusc.2020.146752. [2] A.-S. Royet et al., 2020 Intern. Conf. on Simulation of Semiconductor Processes and Devices (SISPAD), Kobe, Japan, 2020, pp. 89-92, https://doi.org/10.23919/SISPAD49475.2020.9241664.
- [3] L. Esposito et al., J. Appl. Phys. 128, 085305 (2020); https://doi.org/10.1063/5.0016091

Advanced SiGe process modules for nanoelectronics

RESEARCH TOPIC:

Si and SiGe, selective etching, surface preparation, CMOS sub-10 nm, Gate-All-Around Architectures.

AUTHORS:

P.-E. Raynal, S. Rachidi, A. Campo, N. Posseme, J.-M. Hartmann and Virginie Loup

Integrating SiGe layers in advanced transistors is challenging as new cleaning and etching processes have to be developed. The removal efficiency of surface contaminants (such as C, F, O) on SiGe epitaxial layers has thus been assessed prior to the Selective Epitaxial Growth of SiGe:B in Sources/Drains (S/Ds). An original surface preparation based on i) a wet chemical oxide formation followed by ii) a standard NH₃/NF₃ remote plasma Siconi® process was shown to yield the best results. We have also explored the SiGe etching using (i) an isotropic plasma, ii) a wet alkaline solution and (iii) a HCI+GeH4 mixture in an epitaxy tool. Thanks to it, we should be able to selectively remove SiGe in SiGe/Si Gate-All-Around stacks and recess at low temperature SiGe S/Ds.

Context and Challenges

Hole mobility in compressively-strained SiGe channels is several times higher and the bandgap lower than in unstrained Si, making them attractive for use in advanced devices. SiGe surface preparation (prior to selective epitaxy in Sources/Drains regions) and the release of SiGe wires in Gate-All-Around devices are challenging, however. The high reactivity of Ge towards oxidation will then be key to passivate a SiGe surface and obtain highly Si versus SiGe selective etching.

Main Results

A new surface preparation strategy based on i) a wet chemical oxide formation followed by ii) a standard NH_3/NF_3 remote plasma Siconi® process was tested prior to the epitaxial regrowth of $Si_{0.60}Ge_{0.40}$ on $Si_{0.60}Ge_{0.40}$ [1]. Drastically reduced interfacial contaminations, very smooth surfaces and high-quality films after epitaxial re-growth were obtained (Figure 1). A wet alkaline-based process was shown to be too anisotropic for lateral Si wire selective etching [2]. The best results were obtained with an oxidant dry treatment followed by a CF₄/N₂/O₂ downstream plasma step: 20 nm wide SiGe wires were then released (Figure 2) [3]. Finally, we succeeded, with a HCl+GeH4 gaseous mixture, in etching at temperatures 550°C and less Si(:P) and SiGe(:B) in an epitaxy tool [4].

Perspectives

We will shortly test the selective Si versus SiGe dry etching know-how to fabricate stacked SiGe nanowires and HCl+GeH₄ to etch recesses in Si and SiGe prior to re-epitaxy.

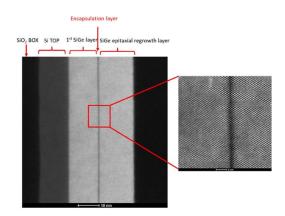


Figure 1: Cross-sectional TEM image after the epitaxial growth of Si_{0.60}Ge_{0.40} on to Si_{0.60}Ge_{0.40} after a "HF/HCI-SC1-Siconi®" surface preparation and some growth parameter tunina.

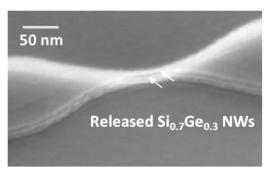
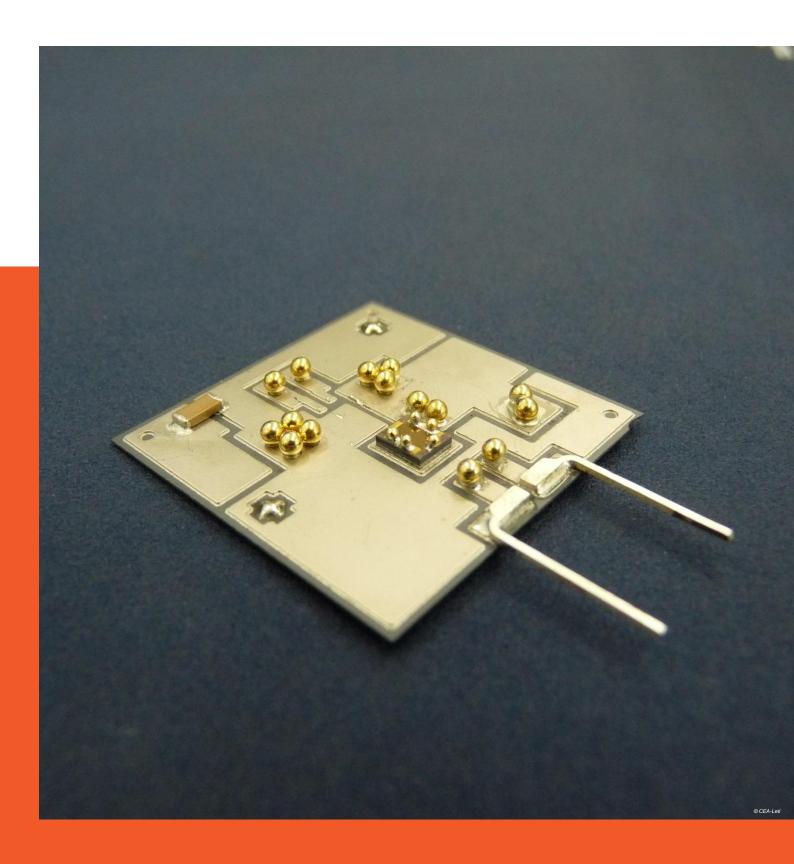


Figure 2: 3D SEM image of two released SiGe nanowires 20 nm wide and 8 nm thick.

- [1] P.E. Raynal et al., Materials Science and Engineering B 262, 11469 (2020); https://doi.org/10.1016/j.mseb.2020.114696.
 [2] S. Rachidi et al., ECS Journal of Solid State Science and Technology 10, 014007 (2021); https://doi.org/10.1149/2162-8777/abddd8.

- [3] S. Rachidi et al., Journal of Vaccum Science & Technology A 38, 033002 (2020); https://doi.org/10.1116/1.5143118, [4] J.M. Hartmann and M. Veillerot, Semiconductor Science and Technology 35, 015015 (2020); https://doi.org/10.1116/1.5143118,



07

3D INTEGRATION & PACKAGING

- Direct hybrid bonding technology towards multiwafer stacking and 5 μM pitch interconnects with Die-to-Wafer stacking
- Chiplets integration on active interposer for heterogeneous multichip-modules and scalable advanced compute nodes towards exascale-level performance Mammography
- Co-integration of TSV mid process and optical devices for Silicon photonics interposers
- Advanced packaging for power applications

Direct hybrid bonding technology towards multiwafer stacking and 5 µm pitch interconnects with Die-to-Wafer stacking

RESEARCH TOPIC:

Hybrid Bonding, 3D Integration, Die-To-Wafer, Heterogenous integration

AUTHORS:

N. Bresson, C. Dubarry, C. Karam, P. Stewart, A. Bond, L. Sanchez, C. Castan, N. Nadi, F. Fournel, C. Euvrard, G. Mauguen, E. Bourjot, ¹Pascal Metzger, **L. Arnaud**

Direct hybrid bonding process, using copper/oxide mix interfaces, is foreseen as essential for the success of 3D heterogeneous integration for both W2W and DTW assemblies. The main direct hybrid bonding benefit is the capability to reach easily interconnection pitches between 1µm to 10µm. The use of this technology is relatively accessible on condition of mastering specific BEOL levels DRM and using tools adapted to fine alignment with ultraclean environment. Two ways of exploring x, y and z axis of 3D structures are presented here. 3 Layer stack explores the Z directions by stacking multiple wafers with fine pitch Interconnections, while die-to-wafer explores x and y directions to fulfill the requirement of 3D heterogeneous integration.

SCIENTIFIC COLLABORATIONS: 1SET Corporation.

Context and Challenges

Recent applications require vertical chip stacking to increase the performance of many devices without the need of advanced nodes. In this perspective, the combination of direct hybrid bonding technology with Through-Silicon-Via will allow associating different functions fabricated on separate wafers. Indeed, Die-To-Wafer (DTW) hybrid bonding process is essential for 3D heterogeneous integration. Process challenges are the control of low nanotopography levels and alignment capability.

Main Results

Wafer to wafer hybrid bonding was achieved with multi-pitch design from 1 to 4µm of single levels of Cu damascene. Defect-free bonding, was demonstrated on a stack with three wafers. Middle wafers thinning was done to a thinning as low as 3µm. Alignment performance was characterized for two superposed hybrid bonding interfaces (Figure 1). In this set of wafers, modelling the alignment enables us to optimize the residuals down to 100nm. For DTW, a specific work reached a final alignment <1µm (Figure 2). Our bonder ensured alignment performance while keeping the surface safe from particle contamination. Dies with interconnection pitches of 5µm were successfully assembled on the same target wafer.

Perspectives

An electrical test vehicle can be reliably fabricated associating multi-wafers stacking with hybrid bonding process and high density thin TSV. Hybrid bonding DTW scaling will be evaluated with electrical and reliability readouts of multi-pitch structures.

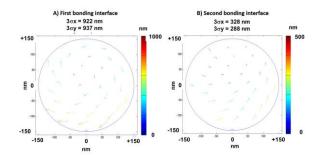


Figure 1: Wafer-to-wafer alignment

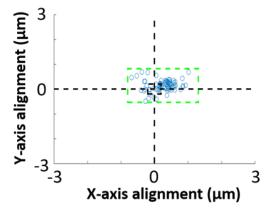


Figure 2: Alignment performances for DTW

- [1] E. Bourjot et al., « Known good dies strategies compatible with Direct Hybrid Bonding », 3DC-TEST Workshop, 2020.
- [2] L. Arnaud et al, MRS Communication 2020, https://doi.org/10.1557/mrc.2020.77

Chiplets integration on active interposer for heterogeneous multi-chip-modules and scalable advanced compute nodes towards exascale-level performance

RESEARCH TOPIC:

Active silicon interposer, chiplet partitionning, 3D integration, high performance computing (HPC), heterogeneous integration

AUTHORS:

P. Coudrain, A. Garnier, P. Vivet, D. Dutoit, P.Y. Martinez, Y. Beilliard^{1,2}, D. Danovitch^{1,2}, D. Drouin^{1,2}, J. Charbonnier

Supercomputers will soon achieve exascale computing performance, for which energy efficiency and computing density are essential. In this perspective, architectural evolutions will be necessary, in particular the introduction of innovative hardware technologies around the processors. The close integration of chips, active interposer and programmable gate arrays (FPGAs) opens the way to dense, efficient and modular computing nodes.

SCIENTIFIC COLLABORATIONS: 1 Institut Interdisciplinaire d'Innovation Technologique (3IT), Université de Sherbrooke, Sherbrooke (CA), ² Laboratoire Nanotechnologies Nanosystèmes (LN2), Sherbrooke (CA)

Context and Challenges

Changes brought by high performance computing are based on exponential increase in performance over last decades. Behind apparent continuity lie architectural revolutions, recently stimulated by 3D integrations. These technologies have enabled heterogeneity and increased bandwidth, now decisive for hardware innovations towards exascale levels. Two Integrations of chiplets on active interposer were demonstrated.

Main Results

Intact integrates 96 cores in 6 chiplets (28nm FDSOI), stacked on a 200 mm² active interposer (65nm CMOS) with 20 µm-pitch micro-bumps. The Interposer embeds on-chip power management, scalable cache coherence, energy-efficient 3Dplugs, memory-IO controller and socket communication, and 40 µm pitch through silicon via [1].

ExaNoDe is the first multi-chip-module combining two dice and a stack of chiplets on active interposer. ExaNoDe support a bandwidth density of 375 GB/s/mm². Measurements and architecture extrapolation indicate that this scheme covers ultrawide workloads range for next generation scalable, highperformance compute nodes [2].

Perspectives

To further improve bandwidth, latency and energy, disruptive photonic interposers will interconnect computing and electricaloptical conversion chiplets. More-than-Moore technologies will enable non classical computing architectures, combining tight logic/memory coupling with 3D technologies such as Coolcube $^{\rm TM}$, nonvolatile memories, and scalable in-memory computing architectures.

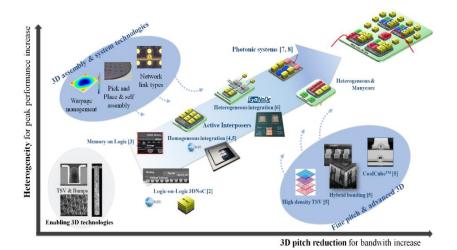


Figure 1: 3D integration roadmap for high performance computing [3

- [1] P. Vivet et al., IEEE International Solid- State Circuits Conference (ISSCC), 2020, https://doi.org/10.1109/ISSCC19947.2020.9062927 [2] P.-Y. Martinez et al., IEEE Symposium on VLSI Technology, 2020, https://doi.org/10.1109/VLSITechnology18217.2020.9265100
- [3] D. Dutoit et al., IEEE International Electron Devices Meeting (IEDM, 2020, https://doi.org/10.1109/IEDM13553.2020.9372037

Co-integration of TSV mid process and optical devices for silicon photonics interposers

RESEARCH TOPIC:

Photonics, Interposer, silicon ring modulator, TSV Mid, Optical Network on Chip (NoC)

AUTHORS:

¹P. Tissier, Y. Thonnart, S. Bernabé, D. Saint-Patrice, S. Malhouitre, M. Assous, R. Vélard, ¹F. Bœuf, J. Charbonnier

Silicon photonics technology is now gaining maturity with increasing levels of design complexity from devices to large photonic integrated circuits. Close integration of control electronics with 3D assembly of photonics and CMOS open the way to high-performance computing architectures partitioned in chiplets connected by optical NoC on silicon photonic interposers. The research team has first introduced a new optical NoC topology and architecture "POPSTAR" (Processors On Photonic Silicon interposer Terascale Architecture) with system analysis concerning process, thermal, device and packaging constraints [1]. Focusing on silicon photonics interposer, TSV Mid integration impact on sensitive photonic structures such as ring modulators has been then extensively studied [2].

SCIENTIFIC COLLABORATIONS: 1ST Microelectronics.

Context and Challenges

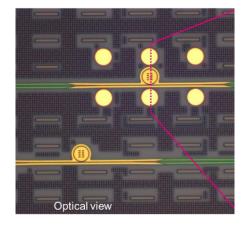
The influence of TSV integration on CMOS device performances has been widely reported but such studies are rare in photonics. This investigation aims to answer whether the added processing steps, thinning and TSV implementation affect photonic performances, and presents guidelines for the design of photonics interposers.

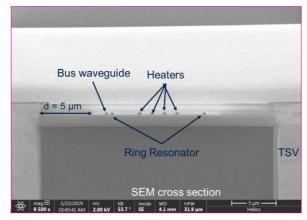
Main Results

The co-integration of TSV mid process 10 µm in diameter and 100 µm in height and photonic devices has been successfully achieved with a detailed impact study of 3D-integration process. The thinning of the wafer, necessary for interconnecting the front and back sides of the interposer, does not impact the photonic performance down to 100 µm in thickness. Sensitive photonic components such as ring resonators reveal no modifications of their optical characteristics with TSV presence at even 1 µm distance. This means that, in terms of design, large wire-bonding pads needed for thermal tuning and modulation of ring resonators could be replaced by a dense TSV matrix. In the framework of Datacenter electrooptical transceivers, this will allow a compact module of ring resonators connected by TSVs with an optimal footprint.

Perspectives

These results of full compatibility of TSV with photonic structures pave the way for new possible architectures in HPC, Datacom or any application requiring large and complex Photonic circuits (switches, neuromorphic, networks,...).





Co-integration of TSV and ring resonator

- [1] Y. Thonnart et al., Automation & Test in Europe Conference & Exhibition (DATE), 2020, https://doi.org/10.23919/DATE48585.2020.9116214 [2] P. Tissier et al., IEEE Electronics System-Integration Technology Conference (ESTC), 2020, https://doi.org/10.1109/ESTC48849.2020.92298

Advanced packaging for power applications



RESEARCH TOPIC:

Power packaging, embedded die, low inductance, double side cooling, heterogeneous integration, SiP

AUTHORS:

J. Delaine, D. Bergogne, V. Rat, F. Rothan, P. Périchon, C. Lanneluc, A. Izoulet, M. Porlan, R. Escoffier, J. Favre¹, **C. Laurant**

Advanced power modules are intended to unleash the full potential of wide-band gap semiconductor like GaN or SiC devices. They are designed to reduce and/or balance parasitic elements, improve heat transfer, while optimizing both cost and reliability. This is achieved through size reduction, 3D integration, new joint materials and double side cooling. First, a new system in package was introduced; it embeds both active and passive devices between two ceramic substrates by silver sintering for automotive application [1]. An alternative to the ceramic substrates is embedding die technology using organic compounds. The team aimed at optimizing the working conditions of a phase leg based on GaN transistors using the industrial DRM of an industrial partner [2].

SCIENTIFIC COLLABORATIONS: 1aPSI 3D

Context and Challenges

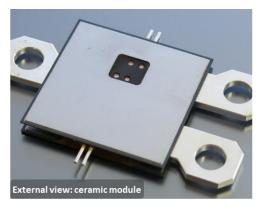
Wide band gap (WBG) devices are pushing the power packaging toward new solutions. As switching operations are faster, the parasitic elements must be reduced and the thermal management improved. The automotive industry is seeking modules allowing a good thermal management either with a low thermal resistance or a high working temperature. This investigation aims at pushing forward packaging topologies so they are no more the critical path for the performances of WBG power converters.

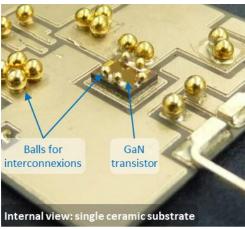
Main Results

The 650V double-side cooling module using ceramic substrates is compatible with high operating temperature. The parasitic inductance is as low as 3 nH at 100 MHz thanks to the ceramic capacitors embedded into the module. Embedded die packaging was studied as an alternative to monolithic Integration. The study showed that it is possible to package together active and passive devices together with very low parasitic elements and a low thermal resistance. By embedding a decoupling capacitor within the package with a half bridge, the parasitic inductance can be as low as 0,7nH.

Perspectives

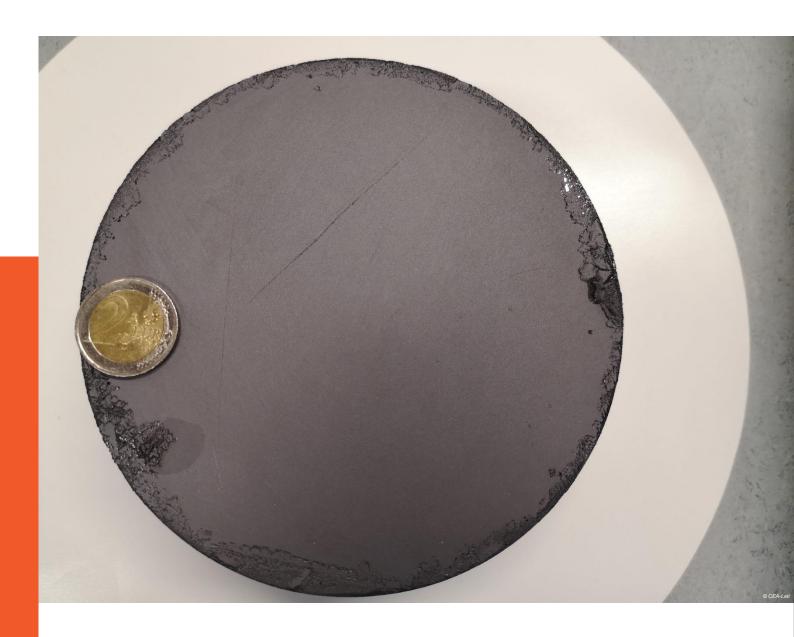
Double side cooling was a first step to improve thermal management and to go further, high working temperature must be investigated along with parallelization of WBG transistors. Organic substrates demonstrated a good potential to take up the challenges of GaN transistors implementation. This first study open the door for higher power applications and/or larger system Integration.





Double side cooling power module using ceramic substrates

- [1] C. Laurant et al., IEEE 70th Electronic Components and Technology Conference (ECTC), 2020, https://doi.org/10.1109/ECTC32862.2020.00222
- [2] J. Delaine et al., PCIM Europe digital days, 2020; https://ieeexplore.ieee.org/document/9178111



Φ=148 mm Cd1-yZnyTe crystal (crystal growth performed at CEA-Leti).

08

MATERIALS & TECHNOLOGY FOR PHOTONICS

- Insights into industrial MOVPE growth of III-nitride structures for high performance devices
- From 5-inch CdZnTe ingots to high quality (111) CdZnTe substrates for SWIR 2K2 15 μm pitch infrared focal plane arrays
- Bragg Diffraction Imaging of CdZnTe Single Crystals
- Mixed van der Waals heterostructures: study of the WSe₂-graphene (2D-2D) and InGaN-graphene(3D-2D) heterojunctions

Insights into industrial MOVPE growth of III-nitride structures for high performance devices

RESEARCH TOPIC:

Analytical models of metalorganic vapor-phase epitaxy (MOVPE) growth of gallium nitride based semi-conductor compounds

AUTHORS:

M. Mrad, J. Kanyandekwe, M. Lafossas, C. Licitra, A. Dussaigne, V. Yon, J. Richy, G. Feuillet, **M. Charles**

The understanding of metalorganic vapor-phase epitaxy (MOVPE) for the growth of III-nitride semiconductor materials is instrumental in speeding up CEA-Leti research and development of LEDs and power electronics for electric vehicles and other emerging applications. In this research, we developed new analytical tools for improving the understanding of III-nitride growth for both LEDs and AlGaN HEMTs

Context and Challenges

The properties and performance of III-nitride devices depend heavily on the epitaxial layers grown. However, MOVPE growth is complex, and modelling of all the thermodynamic and kinetic effects difficult. We developed new analytical tools to improve understanding of III-nitride growth for both LEDs and AlGaN high electron mobility transistors (HEMTs).

Main Results

We examined the impact of growth hardware on In-containing layers. We demonstrated that, due to residual metallic Ga on the showerhead gas delivery system, the In precursor can be converted into a Ga precursor, leading to modifications of layer thickness and composition, as shown in Figure 1 [1]. This issue was previously shown in InAIN layers, and this year we showed that it also applied to InGaN layers used in LEDs. We also created a simplified model of AlGaN growth for HEMTs that considered simplified gas-phase pre-reactions and surface desorption to predict AlGaN layer composition and growth rates. The predictions for HEMT devices were excellent, and the model could also be adapted for use predicting layer growth in UV LEDs, as shown in Figure 2 [2].

Perspectives

We will continue to work on MOVPE models to gain a better understanding of the epitaxial growth of III-nitride materials. Devices from visible and UV LEDs to power electronics for electric vehicles and renewable energy transmission will benefit from this new understanding.

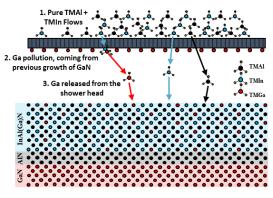


Figure 1: Showerhead interactions model [1]

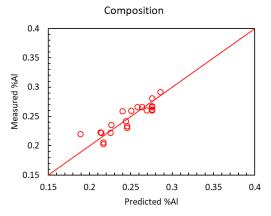


Figure 2: Predicted vs measured AIGaN composition [2]

- [1] Mrad Mrad et al., Journal of Crystal Growth, 536, 125596 (2020), https://doi.org/10.1016/j.jcrysgro.2020.125596 [2] Matthew Charles et al., Phys. Status Solidi B, 257, 1900576 (2020), https://doi.org/10.1002/pssb.201900576
- 2] Watthew Chanes et al., 1 Hys. Status Solidi B, 251, 1900510 (2020), https://doi.org/10.1002/pssb.201900514

From 5-inch CdZnTe ingots to high quality (111) CdZnTe substrates for SWIR 2K² 15 µm pitch infrared focal plane arrays



RESEARCH TOPIC:

Infrared detection circuits with large collection area and mega pixels chips for astrophysical research

AUTHORS:

E. Gout, T. Journot, M. Parent, A. Pagot, J. Merlin, R. Obrecht, D. Giotta, S. Petit, V. Destefanis¹, Y. Fourreau¹, Y. Loreau¹, JL. Santailler

A Cd_{1-y}Zn_yTe single crystal is currently a choice substrate for the growth of lattice-matched Hg_{1-x}Cd_xTe epilayers with cutoff wavelength in the SWIR range (from 2 μm (x=0.54) to 2.9 μm (x=0.4)). Large diameter Cd_{1-y}Zn_yTe ingots are required for the manufacturing of large 2K2 infrared focal plane arrays with 15 µm pitches. We demonstrated in early 2020, the crystal growth of high quality single crystal ingots close to 5-inch in diameter with a Vertical Gradient Freeze-like technique. Thanks to that, we were then able to fabricate for the first time large-dimension infrared (SWIR) 2K², 15 µm pitch, focal plane arrays (FPA). Those results are part of the H2020 Asteroid project.

SCIENTIFIC COLLABORATIONS: 1 LYNRED 364 Avenue de Valence, Actipole CS 1002138113 Veurey-Voroize, France

Context and Challenges

Mega pixels infrared detection circuits are in high demand by the European astrophysical community. The H2020 Asteroid project aims to develop large dimension focal plane arrays (FPA) in the SWIR band with 2K2, 15 µm pitch pixels. The device area is 32 mm², then, and the fabrication of at least 4 devices per wafer is mandatory for economic reasons. Largedimension substrates and an upscaling of all technological steps are necessary, then.

Main Results

The crystal growth of high quality II-VI compounds is a big challenge [1]. After decades of developments, we succeed in delivering to Lynred, which is focusing on 4-inch wafers, CdZnTe ingots 115 mm in diameter. In early 2020, we demonstrated the growth of larger CdZnTe ingots close to 5inch in diameter in an upscale furnace [2]. Wafers were manufactured (crystal orientation, cutting, polishing and surface preparation (Figure 1), epilayer growth of lattice matched HgCdTe layer) and technological processes implemented in Leti's II-VI platform. Then, a set of 2K2, 15 µm pitch, detection circuits were hybridized at Lynred (Figure 2). Processing capabilities on large diameter substrates were thus demonstrated.

Perspectives

Substrate availability was required for production on higher diameter wafers at Lynred. Further optimizations are underway, on those wafers, to obtain the same performances and yields than on smaller diameter substrates.



Figure 1: Φ=148 mm Cd_{1-y}Zn_yTe (lapped) crystal

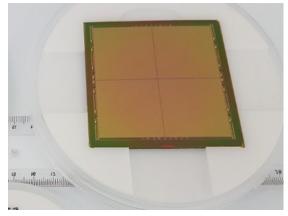


Figure 2: 4 SWIR 2K2, 15 µm pitch, FPA

- [1] D. Breiller et al., Journal of Electronic Materials, 43, N°8, 2901, (2014), https://doi.org/10.1007/s11664-014-3146-x
 [2] J.L. Santailler et al., Proc. SPIE 11407, Infrared Technology and Applications XLVI, 114070G (2020), https://doi.org/10.1007/s11664-014-3146-x

Bragg diffraction imaging of CdZnTe single crystals

RESEARCH TOPIC:

Imaging and characterization of extended defects in CdZnTe bulk crystals used for cooled infrared detectors

AUTHORS:

C. Yildirim, A. Pagot, E. Gout, T.N. Tran Thi1, J. Baruchel1, D. Brellier and P. Ballet

A high-quality CdZnTe single crystal has been imaged with micrometer resolution using monochromatic X-ray Bragg diffraction at the bending magnet (BM)-05 beamline of the European Synchrotron Radiation Facility. Imaging crystal defects is crucial to visualize their arrangement within the bulk. Large field-of-view rocking curve projection maps can be acquired in transmission geometry using samples as thick as 0.5 mm thanks to the Borrmann effect. Section topography can be applied to provide information on the depth of the observed defects allowing for a complete 3D localization of lattice distortions.

SCIENTIFIC COLLABORATIONS: 1 European Synchrotron Radiation Facility (ESRF), Grenoble (FR)

Context and Challenges

Imaging defects in crystals used as templates for infrared detecting HgCdTe layers is crucial to understand both the relationship to detector final performances and the growth mechanisms of CdZnTe.

Main Results

Rocking Curve Imaging (RCI) experiments were conducted at ESRF using the parallel and monochromatic (20 keV) X-Ray beam of the BM-05 beamline. CdZnTe substrates, 0.5 mmthick, cut at the beginning, middle and end of a pulled (111)oriented CdZnTe crystal ingot were put in Bragg conditions for the (220) planes. Imaging over a 2Kx2K, 0.75 µm pitch, pixelized detector resulted in 1.5 mmx1.5 mm frames (Figure 1). Reconstructed images in intensity, peak position or full width at half maximum (FWHM) contain diffraction contrast corresponding to local deformation induced by extended defects such as dislocations. Figure 2 shows FWHM images revealing the different defect density and localization of dislocations for the three substrates imaged. Low FWHM regions (in blue) are defect-free while large FWHM (yellowred lines) corresponds to dislocations which are mostly found to pack in "walls" delimiting cells of high quality materials. The material at the bottom of CdZnTe ingot contains a much higher defect density resulting in thicker, denser walls and thus smaller average cell size.

Perspectives

These RCI experiments provide unique information about crystal defects. RCI will thus be used to follow material optimization during future detector developments.

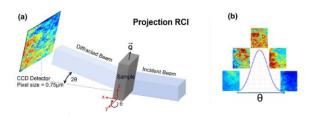


Figure 1: Rocking Curve Imaging (RCI) experiment

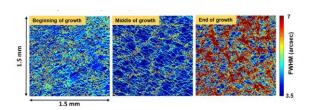


Figure 2: RCI maps of three substrates taken at the beginning. middle and bottom of a pulled CdZnTe ingot.

- [1] C. Yildirim et al., Journal of Electronic Materials, 49, 4550-4556, (2020), https://doi.org/10.1007/s11664-020-08219-2. [2] C. Yildirim et al, Journal of Synchrotron Radiation, 28, 1, 301-308, (2021), https://doi.org/10.1107/S1600577520014149.

Mixed van der Waals heterostructures: study of the WSe₂-graphene (2D-2D) and InGaN-graphene(3D-2D) heterojunctions



RESEARCH TOPIC:

2D materials and heterostructures

AUTHORS:

C. Paillet, Y. J. Dappe, Y. Almadori, M. T. Dau, C. Vergnaud, M. Jamet, P. Pochet, S. Vézian¹, A. Michon¹, B. Damilano¹, B. Grévin, B. Hyot

The identification of a growing number of two-dimensional (2D) materials has inspired worldwide efforts to integrate 2D materials into van der Waals (vdW) heterostructures. Given that any passivated, dangling bond-free surface will interact with another via vdW forces, the vdW heterostructure concept can be extended to include the integration of 2D materials with non-2D materials. Such combinations of materials would yield vdW heterostructures with a variety of structural and electronic properties opening up new avenues for innovative device designs. We present here the study of a 2D-2D WSe₂-graphene heterojunction by Kelvin probe force microscopy and the epitaxial growth study of a 3D-2D InGaN on graphene heterojunction.

SCIENTIFIC COLLABORATIONS: 1 Université Côte d'Azur, CNRS-CRHEA, Valbonne (FR)

Context and Challenges

The emergence of van der Waals-bonded heterostructures has opened fantastic perspectives for the design of innovative devices.

Main Results

We demonstrated in [1] the nucleation and growth of InGaN on graphene by molecular beam epitaxy. As shown in Figure 1, the nucleation of InGaN occurs through the formation of dendrite-like islands weakly bonded with the fully preserved graphene layer. Further growth of the InGaN nuclei leads to the formation of a non-fully coalesced film in partial epitaxy with the SiC substrate underlying the graphene layer. In opposition to conventional epitaxially grown heterostructures, a very weak binding energy between the substrate and the III-N semiconductor was evidenced.

In the work reported in [2], we investigated the electronic properties of WSe₂ layers deposited on graphene (itself grown on SiC substrates) by Kelvin probe force microscopy (Figure 2). Experimental data reveal the existence of an interface dipole, which is shown by DFT to originate from the neutralization of graphene n-doping by an electron transfer towards the WSe2 layers. These interfaces can be described in a 2D version of the Schottky-Mott model by taking into account this interface dipole.

Perspectives

In vdW heterostructures, electrostatics fields and charge transfers at interfaces play a significant role. It is of particular importance to understand these effects to take advantage of those specific surface properties in innovative devices.

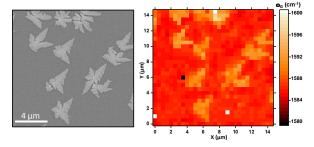


Figure 1: SEM image and ω_G Raman map of InGaN on graphene

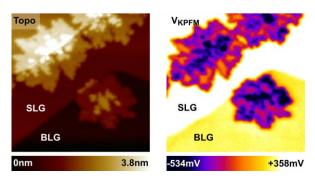
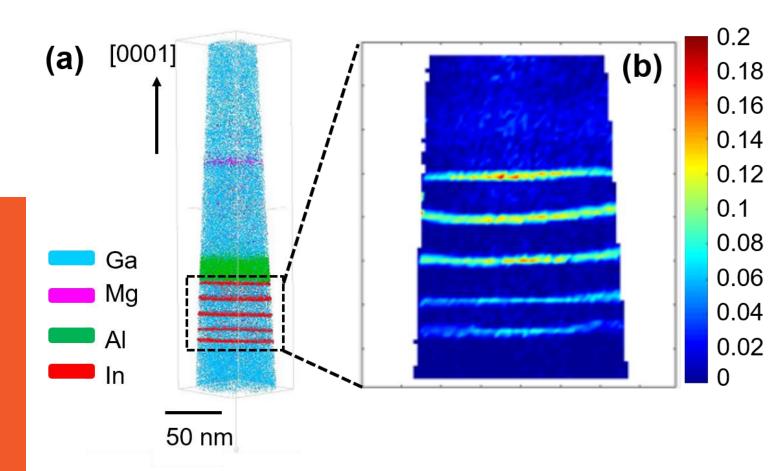


Figure 2: AFM and KPFM images of WSe2 on graphene

- [1] C. Paillet et al., Nanotechnology, 31, 40, (2020), https://doi.org/10.1088/1361-6528/ab98bd [2] Y. J. Dappe et al., Nanotechnology, 31, 25, (2020), https://doi.org/10.1088/1361-6528/ab8083



3D APT reconstruction of hybrid tunnel junction LED structure (a) and calculated In-site fraction of the MQWs (b)



CHARACTERIZATION

- 3D atomic-scale correlative microscopy of GaN-based materials for optoelectronic devices
- Measurement of magnetic fields with nm-scale resolution by off-axis electron holography
- Hybrid nano-characterization of complex materials and objects
- Development of fast and nondestructive in-line metrology for the elemental depth-profiling of thin inorganic materials
- Accurate metrology of composition and mass deposition for the development of chalcogenide materials
- Phase change memory materials structural characterization & metrology

3D atomic-scale correlative microscopy of GaN-based materials for optoelectronic devices

RESEARCH TOPIC:

Optical spectroscopy, atomic-scale microscopy, physicalchemical correlation

AUTHORS:

I.Dimkou, E. Di Russo, D. Cooper, E. Monroy, L. Rigutti¹, N. Rochat, A. Grenier

The continuous development of new LEDs based on III-N nitrides semiconductors from disinfection in UV to microdisplays in the visible range requires optimized efficiency and low energy-consumption as these devices cover numerous applications. An original approach combining multi-spectroscopic and microscopic (CL, SIMS TEM, APT) characterizations to electronic band structure simulations of the device has been developed. The gain of knowledge from the correlation of the physical, structural and chemical signatures on both blue and UV LED span from device design to technological Integration.

SCIENTIFIC COLLABORATIONS: 1UNIROUEN, CNRS, Groupe de Physique des Matériaux (FR)

Context and Challenges

Optimizing the efficiency of III-N based materials is a global challenge since such devices are used in a large field of applications: lighting, telecommunication, disinfection, power... Many factors may cause a drop in performance such as alloy fluctuations, interface roughness, inter-diffusion, dislocations or strain. Consequently, understanding the efficiency of GaN based devices with regard to their structural and chemical properties is a way to better understand their behavior.

Main Results

We showed how multi-spectroscopic and microscopic characterization (CL-TEM-SIMS-AFM-APT) combined with 3D simulations of electronic band structure of the nano-objects using Nextnano3 software, which has been adapted for IIInitride calculations. We demonstrated that the structural and chemical information extracted from these techniques allow the precise modeling of the electronic band structure of these nanostructures; obtaining excellent agreement with optical and electrical measurement. The comparison between simulated and measured device behavior such as emission energy [1] or depletion length [2] lead to a better understanding of device performance.

Perspectives

The correlative approach could easily evolve to find application in the characterization of nanoscale transistors, quantum sensors, and actuators. We will continue to develop this approach at CEA-Leti to address complex sample architectures such as nano and micro-wire for lighting applications in the frame of ANR-ASCESE 3D (2021-2025).

Structural and chemical signature of InGaN/GaN QDs

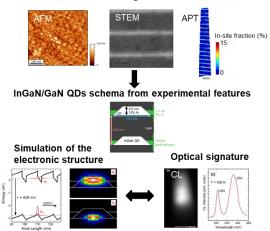


Figure 1: InGaN/GaN QDs investigation: from structural and chemical investigations to simulation of the electronic band profile and electron-hole distribution. Comparison between experimental and measured emission energy provides deep understanding of the structure's behavior.

- [1] I. Dimkou et al., ACS Appl. Nano Mater. (2020), doi.org/10.1021/acsanm.0c02106 [2] Di Russo et al., Nanotechnology (2020), https://doi.org/10.1088/1361-6528/ab996d

Measurement of magnetic fields with nm-scale resolution by off-axis electron holography

RESEARCH TOPIC:

Transmission Electron Microscopy, Electron Holography, Magnetic Devices, Spintronics

AUTHORS:

V. Boureau, T. Almeida, B. Dieny¹, L. Prejbeanu¹, **D. Cooper**

Off-axis electron holography is a transmission electron microscopy based technique that can be used to measure magnetic, electrostatic and strain fields with nm-scale resolution. In order to meet the demands of spintronic devices, off-axis electron holography has been developed for the measurement of magnetic fields. To test the quantitative nature of this technique some simple NiFe nanowires (NW) have been examined. Methods has been developed to simultaneously optimize the signal-to-noise and achieve a spatial resolution of 1 nm. Then magnetic memory devices have been examined at room temperature and at elevated temperature to assess their thermal stability.

SCIENTIFIC COLLABORATIONS: ¹Univ. Grenoble Alpes, CNRS, CEA, Spintec (FR)

Context and Challenges

Magnetic random access memory (MRAM) devices are excellent candidates for information storage. They exhibit excellent scalability with fast switching speeds. However, as they are reduced in size, they become less stable with temperature increase. In this work, some different MRAM devices have been examined to assess the effect of the use of perpendicular shape anisotropy (PSA) to improve stability for small device dimensions.

Main Results

Experimental methods have been developed to perform electron holography with unprecedented signal-to-noise and simultaneous nm-scale spatial resolution [1]. These techniques are now used on a daily basis to measure the fields in classical semiconductor and spintronic devices. Here, MRAM devices were examined as a function of temperature in-situ in a TEM. Large devices with a diameter of 100 nm and 1 nm thick magnetic storage layers were found to be unstable at temperatures above 150°C [2]. Subsequent devices with 20 nm diameters and 50 nm thick storage layers were found to be stable at temperatures up to 250°C confirming that the use of PSA is a viable approach for the implementation of MRAM devices for reliable data storage solutions.

Perspectives

Spintronic devices are expected to become an important part of the microelectronic industry. By putting in place a quantitative magnetic field mapping technique with the appropriate spatial resolution and sensitivity, CEA-Leti has the capability to support this activity.

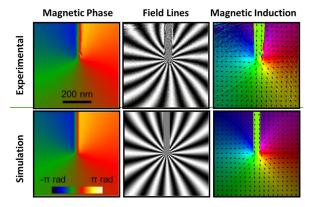


Figure 1: Quantification using magnetic NiFe NW

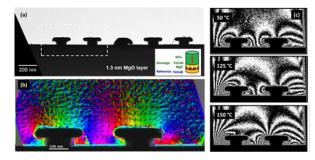


Figure 2: MRAM device examined at high temperature

- [2] V. Boureau *et al.*, J. Phys. D: Appl. Phys. (2020), <u>doi.org/10.1088/1361-6463/abc77d</u> [2] V. Boureau *et al.*, Nanoscale (2020), <u>doi.org/10.1039/D0NR03353G</u>

Hybrid nano-characterization of complex materials and objects

RESEARCH TOPIC:

Surface analysis, micron scale, atomic-scale microscopy, hybrid characterization

AUTHORS:

A. Gomes de Carvalho, A. Priebe¹, T. E. J. Edwards¹, O. Renault, J.-P. Barnes

The developments of innovative materials for specific, demanding applications, as well as the need for understanding complex objects and materials assembly such as biological systems studied at the frontiers between physics, biology and technology, calls for increasingly sophisticated analytical methods. A new field is, for instance, rapidly evolving where different techniques are combined into hybrid approaches, enabling materials analysis at complementary scales and information levels. Here, two examples illustrate this trend in materials analysis: the hybrid nano-characterization of a brain tissue section and of diluted nanoparticles

SCIENTIFIC COLLABORATIONS: ¹Empa, Swiss Federal Laboratories for Materials Science and Technology (CH)

Context and Challenges

Materials complexity increases due to more demanding applications and diversified needs. Materials analysis now requires hybrid characterization involving complementary techniques implemented at different scales and levels of sophistication for providing answers towards deeper understanding and reliable qualification of the systems studied.

Main Results

We showed for the first time the combined use of time of flight secondary ion mass (TOF-SIMS) and X-ray photoemission spectroscopy (XPS) and microscopy to successfully image at the micron scale chemical heterogeneities in brain tissues after neural device implantation [1]. The key advantage of this approach is the chemical identification and quantification of relevant regions scanning transmission electron microscopy combined with energy-dispersive X-ray spectroscopy (STEM/EDX) was used to image Al nanoparticles (NPs) in an amorphous ZrCuAg metal alloy matrix. To successfully image the NPs, both instruments had to be pushed to their limits (Figure 2), vibration reduced to a minimum and secondary ion yield maximized (oxygen flooding).

Perspectives

Getting beyond combined analysis in hybrid characterization will require meaningful correlations from similar areas at the mesoscopic scale. This will open up new possibilities for the analysis of complex systems in cutting-edges-technologies such as nano- and optoelectronics and biotechnologies.

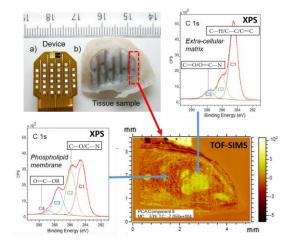


Figure 1: XPS/TOF-SIMS combination on brain tissue

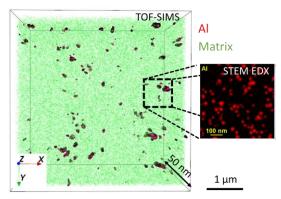


Figure 2: STEM-EDX/TOF-SIMS of AI nanoparticles.

- [1] A. Gomes de Carvalho et al., Biointerphases (2020), doi.org/10.1116/6.0000110
- [2] A. Priebe et al., Anal. Chem. (2020), doi.org/10.1021/acs.analchem.0c02361

Development of fast and non-destructive in-line metrology for the elemental depth-profiling of thin inorganic materials



RESEARCH TOPIC:

Characterization, metrology, grazing-incidence X-ray fluorescence, plasma-profiling time-of-flight mass spectrometry

AUTHORS:

Y. Mazel, S. Torrengo, M-C Lépy¹, D. Eichert², A. Tempez³, E. Nolot

In-line metrology of the elemental depth-profiles in thin inorganic layers is crucial to monitor process-induced elemental distribution and to reveal unexpected buried contamination. We firstly demonstrated the performances of combined grazing-incidence X-ray fluorescence and X-ray reflectivity for the non-destructive analysis of thin layers films from 1 to 200 nm with sub-nm resolution. Improved surface sensitivity can be obtained by the use of multilayered substrates, as investigated in collaboration with CEA-List and Elettra synchrotron. Sub-nm resolution was also achieved by plasma profiling time-of-flight mass spectrometry (PP-TOFMS), enabling destructive but very fast reference-free analysis of films up to few µm, as demonstrated in the frame of collaboration with Horiba.

SCIENTIFIC COLLABORATIONS: 1 CEA, LIST, (LNE-LNHB), (FR), 2 ELETTRA, Sincrotrone Trieste, (IT), 3 HORIBA (FR)

Context and Challenges

Thin layered inorganic materials often feature in-depth elemental distribution, which may be designed to improve the device performance, induced by process steps, or resulting from unexpected buried contamination. In-line metrology strategies are developed to access elemental depth-profiles with sub-nm resolution.

Main Results

We have established that the combination of grazingincidence X-ray fluorescence and X-ray reflectivity was a tool of choice for sub-nm resolution non-destructive elemental depth-profiling in materials with thickness ranging from 1 to 200 nm [1]. The surface sensitivity of such analysis may be improved by the adjustment of the X-ray standing wave field according to multi-layered substrates (SML) (Figure 1) [2]. PP-TOFMS is a destructive technique which provides very fast depth-profile information for thickness ranging from a few nm up to a few μm . In addition, as all elements feature similar relative sensitivity factors, it allows reference-free analysis of the elemental distribution (Figure 2.). We have demonstrated these performances, first on thick layers with buried contamination, then on thin phase-change materials at different process steps [3].

Perspectives

The improvement of the performances of PP-TOFMS will be conducted in collaboration with Horiba. It will include the establishment of a database of relative sensitivity factors as a long term action, and innovative strategy to improve the measurement of light elements.

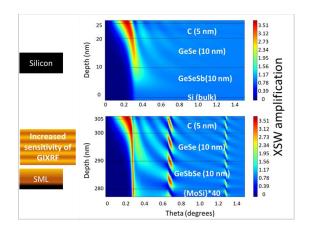


Figure 1: Amplification of XRF signal with SML

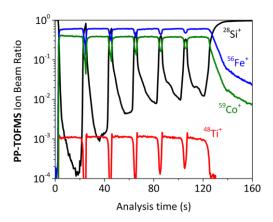


Figure 2: PPTOFMS analysis of buried contamination

- [1] S. Torrengo et al, Spectrochimica Acta Part B,(2020), https://doi.org/10.1016/j.sab.2020.105926 [2] E. Nolot et al, Spectrochimica Acta Part B (2020), https://doi.org/10.1016/j.sab.2020.105864
- [3] E. Nolot et al, Surf Interface Anal. (2020), https://doi.org/10.1002/sia.6823

Accurate metrology of composition and mass deposition for the development of chalcogenide materials

RESEARCH TOPIC:

Characterization, metrology, mass deposition, composition, chalcogenide, phase-change memory, 2D materials

AUTHORS:

C. Sabbione, S. Cadot, C. Jeynes¹, B. Beckhoff², E. Nolot

We have developed strong collaborations with the University of Surrey and the Physikalisch-Technische Bundesanstalt to improve the accuracy of in-line metrology of the composition and the mass deposition of thin chalcogenides materials with composition-driven performances. We specifically investigated challenging metrology characterizations around ultrathin transition metal dichalogenides and nitrogen-doped phase-change telluriumbased materials.

SCIENTIFIC COLLABORATIONS: 1 University of Surrey (UK), 2 Physikalisch-Technische Bundesanstalt (PTB) (DE)

Context and Challenges

The properties of chalcogenide materials are highly driven by composition, which results in challenging metrology for ultrathin transition metal dichalogenides and for phase-change telluriumbased materials doped with light elements such as nitrogen.

Main Results

The in-line metrology scheme for transition dichalogenides includes X-ray photoelectron spectroscopy for measurement and high-resolution fluorescence (XRF) to access the mass deposition. The importance of an accurate calibration strategy was specifically demonstrated on MoS₂ films by comparison with reference-free experiment conducted by the PTB-Berlin at Bessy synchrotron [1]. Similarly, the accuracy of XRF analysis for the composition of nitrogen-doped GeSbTe alloy phase-change materials strongly depends on reference values measured by ion beam techniques (IBA) (Figure 1). We first highlighted the significant discrepancy of these values upon IBA Then, we collaborated with the University of Surrey to develop IBA strategy with controlled uncertainty and based on elastic backscattering spectrometry, resulting in in-line XRF analysis aligned with process accuracy requirements (Figure 2) [2].

Perspectives

Improved fundamental parameters of sulfur will be investigated in the frame of the international Fundamental Parameters Initiative. The influence of high-energy photoelectrons in XRFbased quantification of light elements will be evaluated.

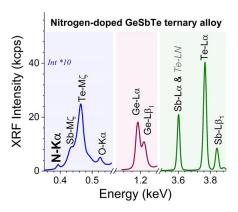


Figure 1: High-resolution XRF spectra of GSTN film

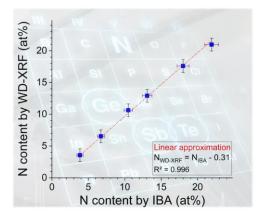


Figure 2: Accuracy of XRF calibrated against RBS

- [1] E. Nolot et al, Spectrochimica Acta Part B 166 (2020) 105788, https://doi.org/10.1016/j.sab.2020.105788 [2] C. Jeynes, E. Nolot et al, J. Anal. At. Spectrom., (2020), 35, 701–712, https://doi.org/10.1039/C9JA00382

Phase change memory materials structural characterization & metrology

RESEARCH TOPIC:

PCRAM, chalcogenides, phase change, X-ray diffraction, stress, strain, crystallization, demixing

AUTHORS:

L. Prazakova, E. Nolot, F. Fillot

The thermal crystallization of Ge₂Sb₂Te₅ (GST) and Ge-rich GST thin films has been investigated by in-situ X-ray diffraction (XRD). Firstly, the use of different X-ray diffraction techniques allows to investigate the mechanical behaviour by plotting the strain versus stress evolution upon crystallization. Therefore, nanoscale strain, macroscale stress and nucleation / crystallization are then fully described. Secondly, the isothermal XRD analysis of Ge-rich GST enables to consider the structural evolution and the crystallization mechanism of the material. It demonstrates the progressive structural rearrangement at higher temperatures, resulting in complete demixing of Ge and GST crystalline phases

Context and Challenges

The concept of PCRAM (Phase Change Random Access Memory) features a simple device structure and excellent performances and appears to be suited for the next generation of non-volatile memories. Today, Germanium Antimony Telluride alloys (GST and Ge-rich GST) are considered as the best candidates.

Main Results

The correlation of XRD techniques (in-plane XRD, out of plane XRD, high resolution XRD on substrate and 2D high energy XRD) allows the characterization of the mechanical behaviour of GST upon thermal crystallization. The GST nanomechanics is then characterized by a new method at the nanoscale and at the macroscale. Plotting the stress vs. strain allows to calculate Young moduli between 9 GPa to 37 GPa for amorphous and crystalline matrix. Intermediate states with amorphous / crystalline ratio can be also deduced (Figure 1).

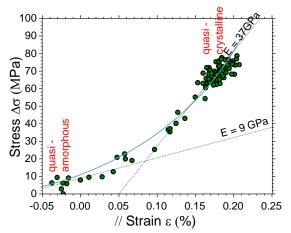


Figure 1: Elastic curve of GST at 125°C

The isothermal XRD has been performed on Ge-rich GST alloys to investigate its crystallization mechanism. The results highlight the formation of a transient GST phase (G+GST) and thus the progressive rearrangement of the material structure (Fig. 2). The G+GST phase (higher Ge content with respect to GST) is driven by crystallization phenomena, leading to the gradual expulsion of Ge. Therefore, the Ge-rich GST system moves toward the complete separation of Ge and GST stable phases.

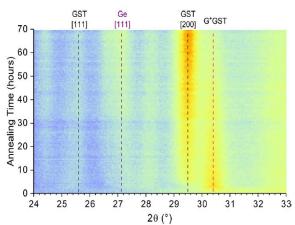


Figure 2: XRD at 300°C on Ge-rich GST alloys

Structural analysis of thermally crystallised PCM is still under investigation by x-ray scattering. In particular, XRD line profile of PCM deserves a full and deep analysis.

- [1] F. Fillot et al., J. Appl. Phys, (2020), https://doi.org/10.1063/5.0023653
 [2] L. Prazakova et al., J. Appl. Phys, (2020), https://doi.org/10.1063/5.0027734



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PHD DEGREES AWARDED IN 2020

- Adrien HUGO
- Matthias FRACCAROLI
- Konstantinos TRIANTOPOULOS
- Anthonin VERDY
- Denys LY
- Jon DE VECCHY
- Raphaël BAYLE
- Mrad MRAD
- Pierre JANIOUD
- Diego ALFARO ROBAYO
- Julien SOREL
- Andrea QUINTERO
- Louise BANNIARD
- Daphnée BOSCH
- Thomas DALGATY
- Rebecca CHAHINE
- Flore BOYER
- Edouard VILLEPREUX
- Ousmane Magatte KANE
- Baptiste NEFF
- Mostafa BARIK El

ADRIEN HUGO

GRAPHENE-BASED LIQUID-GATED TRANSISTORS FOR BIOSENSING

University Grenoble Alpes - February 27th, 2020



With the rise of cancers, infectious and cardiovascular diseases, the early and/or real-time robust detection of the associated biomarkers is particularly crucial for establishing a diagnosis and an efficient treatment. Considering a worldwide ageing population and the growing need for an improved healthcare in emerging countries such as India or China, the demand for point-of-care diagnostics represents a field of applications biosensors. Graphene-based solution-gated field-effect-transistors (SGFET) represent a highly promising generation of biosensors, in line with the superior sensitivity of biosensors benefiting from the exceptional properties of nanowires and carbon nanotubes. Transforming a SGFET device into a biosensor requires to immobilize bioreceptors at the graphene surface. The non-covalent functionalization is the most efficient technique, since it can preserve both graphene structural integrity and electrical properties. In this perspective, PBASE is widely used, since this molecule can adsorb onto graphene by pi-pi interactions, while exposing a reactive moiety serving as an anchor for grafting biological receptors. However, it is not systematically demonstrated that bioreceptors remains functional when grafted to PBASE, since this molecule lacks the ability to prevent bioreceptors from stacking onto graphene and consequently being denaturated. The "tripod" is a molecule binding multivalently to graphene thanks to three pyrene feet, effectively projecting any active functionality away from the surface, and forming a predictable and robust biorecognition layer on graphene. In this context, this thesis work aimed at developing a tripod functionalized graphene-based SGFET for highly robust, and sensitive biosensing applications. Different methods were explored in order to establish a stable and reproducible fabrication process. particular, this process was characterized through a set of AFM, XPS and Raman measurements. The performance of the asfabricated devices was assessed before non-covalent functionalization, through electrical measurements in air and in liquid environments, and a first proof of concept of streptavidin detection was presented.



MATTHIAS FRACCAROLI

TRANSPARENT AND CONDUCTIVE VANADIUM SULFIDE FILM SYNTHESIZED BY CVD/ALD ON LARGE AREAS

University Grenoble Alpes – March 11th, 2020

In the context of functional diversification ("More than Moore"), transition sulfides are currently being actively studied for original optical devices production. Some materials in this family have a lamellar structure, similar to graphene like vanadium sulfides. The synthesis of these lamellar films remains actively dominated by high-temperature CVD processes (> 550 ° C). However, in order to hope the development of a reliable synthesis method, it is important to reduce the deposition temperature that leads to a poor uniformity and a poor conformity. In this work, we have studied the potential of a chemical vapor deposition approach at low temperature (200 °C). This method allow

us to obtain an amorphous vanadium sulfide film on a 300 mm wafer and point out their ability to self-reorganize in order to obtain a lamellar film of V₇S₈ after thermal annealing. A 5.2 nm film has interesting optical and electrical properties; this film is conductive with a carrier density of 1.1.10²³ cm⁻³, the holes are the main charges carriers (type p), a mobility of 0.2 cm².(Vs)⁻¹, a conductivity of 1063 S.cm⁻¹, an output work of 4.8 eV while preserving good transparency (transmittance of 75% for a wavelength of 550 nm).



KONSTANTINOS TRIANTOPOULOS THERMAL EFFECTS IN ADVANCED SI-MOSFETS

University Grenoble Alpes - March 27th, 2020

CMOS technology has now reached the size of about 10 nm and below. Researchers and manufacturers are now trying to push the physical limits imposed by scaling down, by acting on different technology levers to improve device performance without further reduce dimensions. New transistor architectures have been introduced, such as planar thin film transistors (FDSOI) or the multi-gate transistors (Trigate, FinFETs, ...). The integration of new semiconductor materials (III-V materials ... 2D) is also being considered for advanced technology nodes (≲7nm) to maintain electrical performance. An alternative to this scheme, however, is possible with sequential 3D integration (called CoolCube™ see figure) [1]. This integration is to sequentially produce two levels of transistors, the levels being connected at the same time that the process of the transistors. This integration provides a high density of transistors through the use of the third dimension (vertical). However, this technology requires the development of low-temperature manufacturing processes for the upper stage of the transistors in order to maintain the performance of the transistors of the lower floor. The proposed thesis is in this context, focusing on the study of electrical properties of these 3D devices (upper and lower floor, mutual influence of the two levels of transistors) to optimize the operation thereof. Objectives of the thesis: the main objective is the study of electrical of MOS transistors manufactured CoolCube Leti, with a special focus on transport in the channel and reliability associated with the performance.

The job is largely experimental, based on electrical measurements of transistors. From these measures, we will seek, in addition to assessing the overall performance of these transistors, to study the carrier mobility of the channel in the top transistors (low thermal budget) and down (additional thermal budget), the effect of self-heating (related to thin films and the reduced volume of the channel) on each floor and that induced by the operation of a stage on the other. It will also focus on assessing the reliability of each stage transistors, linked with other electrical characteristics and technological processes used. The thesis will be carried out in the laboratory of electrical characterization (LCTE) Silicon Components department Leti, in close collaboration with the laboratory 'integration-die' (LiCI).



ANTHONIN VERDY

STUDY OF AMORPHOUS CHALCOGENIDE MATERIALS AND OF THEIR ELECTRICAL THRESHOLD PROPERTIES TARGETING THE DEVELOPMENT OF SELECTOR DEVICES FOR RESISTIVE MEMORIES

University Grenoble Alpes - June 5th, 2020

A performance gap between the CPU and the memory is growing more and more: the CPU is waiting the information. The development of new technologies of memories is becoming a necessity to support the evolution of microelectronics. Among them, resistive memories represent the best candidates for the development of new systems capable of boosting the performances of a computer. However, such memories have to be integrated in series with a Back-End selector device in order to achieve their full performances. The aim of this thesis is to studied the electrical ovonic threshold switching (OTS) in amorphous chalcogenides targeting the development of selector devices. An experimental work evaluate different materials based on the Ge₃₀Se₇₀ and As₂Te₃ compounds. For each material, the structural, optical and electrical

properties are characterized. The benchmark and the correlation between the materials highlight the impact of the different elements of the composition on the OTS mechanism. Finally, trade-off, guidelines and methodology are given in order to drive the development of OTS selector according to the specifications to achieve.

DENYS LY

RESISTIVE MEMORIES AND 3D MONOLITHIC TECHNOLOGIES FOR RECONFIGURABLE SPIKING NEUROMORPHIC PROCESSORS

University Grenoble Alpes – June 19th, 2020

The human brain is a complex, energy-efficient computational system that excels at cognitive tasks thanks to its natural capability to perform inference. By contrast, conventional computing systems based on the classic Von Neumann architecture require large power budget to execute such assignments. Herein comes the idea to build brain-inspired electronic systems, computing the so-called neuromorphic approach. In this thesis, we explore the use of novel technologies, namely Resistive Memories (RRAMs) and threedimensional (3D) monolithic technologies, to enable the hardware implementation of compact, low-power reconfigurable Spiking Neural Network (SNN) processors. We first provide a comprehensive study of the impact of RRAM electrical properties on SNNs with RRAM synapses and trained with unsupervised learning (Spike-Timing-Dependent Plasticity (STDP)). In particular, we clarify the role of synaptic variability originating from RRAM resistance variability. Second, we investigate the use of RRAM-based Ternary Content-

Addressable Memory (TCAM) arrays as synaptic routing tables in SNN processors to enable on-the-fly reconfigurability of network topology. For this purpose, we present indepth electrical characterisations of two RRAM-based TCAM circuits: (i) the most common two-transistors/two-RRAMs (2T2R) RRAM-based TCAM, and (ii) a novel onetransistor/two-RRAMs/one-transistor (1T2R1T) RRAM-based TCAM, both featuring the smallest silicon area up-to-date. We compare both structures in terms of performance, reliability, and endurance. Finally, we explore the potential of 3D monolithic technologies to improve area-efficiency. In addition to the conventional monolithic integration of RRAMs in the back-end-of-line of CMOS technology, we examine the vertical stacking of CMOS over CMOS transistors. To this end, we demonstrate the full 3D monolithic integration of two tiers of CMOS transistors with one tier of RRAM devices, and present electrical characterisations performed on the fabricated devices



JON DE VECCHY

REALIZATION OF INNOVATIVE SUBSTRATES BASED ON DIAMOND

University Grenoble Alpes – July 2nd, 2020

Within a global aim of reducing energy consumption, microelectronics components must be more efficient and less energyconsuming. Power electronics, which converts electric power, is particularly concerned because its component must operate at high intensity, voltage and temperature. Silicon, the base material of these components, is reaching its limits and the conception of components made with other materials is currently being studied. Among the candidate materials, diamond and its outstanding properties is of great interest. Its excellent thermal conductivity (2200 W/m/K) combined with high breakdown field (10 MV/cm) and high hole mobility (2000 cm²/V/s) are attractive for making smaller and more efficient components. However, monocrystalline diamond synthesis methods are limiting substrate size to about 15 x 15 mm², thus preventing its industrialization. The approach developed in this thesis is the diamond layer transfer to another substrate by adapting the Smart Cut™ process. This process is based on a combination of ion implantation and bonding of the implanted substrate to a receiving substrate. Annealing then causes the fracture of the implanted substrate and the detachment of a film

(with controlled thickness) which is transferred to the receiving substrate. This approach would make it possible to reduce component cost by decreasing diamond consumption and to open the way to industrialization thanks to successive transfers on a large substrate. Smart CutTM must be fully adapted to the diamond case, studies of each step will thus be presented. Blistering observation on the implanted substrate surface after annealing is the very first step of ion implantation parameters adaptation. A blistering process using combinations of hydrogen ion implantation and annealing will be presented. Diamond transformations occurring during the process will be characterized. Full layer transfer studies using substrate bonding will then be presented. Finally, prospects optimization and realization will be given.



RAPHAËL BAYLE MODELLING OF PHASE CHANGE MECHANISMS IN PCM MEMORIES USING THE MULTI-PHASE-FIELD METHOD

Institut Polytechnique de Paris – July 7th, 2020

Phase change memories (PCM) exploit the variation of resistance of a small volume of phase change material: the binary information is coded through the amorphous or crystalline phase of the material. The phase change is induced by an electrical current, which heats the material by the Joule effect. Because of its fast and congruent crystallization, the Ge₂Sb₂Te₅ alloy is widely used for PCM. Nevertheless, to get a better reliability at high temperatures, which is required for automotive applications, STMicroelectronics uses a Ge-rich GeSbTe alloy. In this alloy, chemical segregation and appearance of a new phase crystalline occur during crystallization. The distribution of phases and alloy components are critical for the proper functioning of the memory cell; thus, predictive simulations

would be extremely useful. Phase field models are used for tracking interfaces between areas occupied by different phases. In this work, a multi-phase field model allowing simulating distribution of phases and species in Ge-rich GeSbTe has been developed. The parameters of the model have been determined using available data on this alloy. Two types of simulations have been carried out, firstly to describe crystallization during annealing of initially amorphous deposited thin layer; secondly to follow the evolution of phase distribution during memory operation using temperature fields that are typical for those operations. Comparisons between simulations and experiments show that they both exhibit the same features.



PIERRE JANIOUD
THERMAL PIEZORESISTIVE BACK ACTION IN SUSPENDED SILICON NANOWIRES BASED MEMS

The development of new technologies, either in consumer electronic domain (smartphones, internet of things...) or in automotive domain (autonomous vehicles), largely boosted the increasing demand of miniaturized and highly performant sensors. Piezoresitive transduction by means of silicon nanowire is particularly interesting to improve detection capability of current sensors. Various benefits of this transduction have been identified for NEMS and MEMS applications, and in particular, high sensitivity and excellent compactness. Moreover, power consumption remains a major issue for miniaturized sensors. Optimized use of nanowires could eventually lead to significant improvement of this transduction mechanism for low power and high performances sensors. Thermal Piezoresistive Back Action (TPBA), highlighted in DC-biased nanowires, allows to finely control electromechanical response

University Grenoble Alpes – July 10th, 2020

and optimize the transduction mechanism of MEMS. Based on a thermal, electrical and mechanical coupling, this phenomenon particularly allows to reach a self-sustained oscillation regime that could be used to monitor the resonance frequency of a resonator. The objective of this thesis is to study this back action mechanism in nanowires used for M&NEMS components developed at CEA-Leti. A complete study of silicon nanowires properties, whose typical dimensions are 250 nm x 250 nm x 5 µm, allows to evaluate their interest to implement this mechanism. Based on analytical models and finite element modeling, a model of this phenomenon is proposed. Then, it is confronted with experimental results achieved on existing components and others fabricated during this thesis. Finally, a discussion on the perspectives of this study evaluates the gain brought by this mechanism and its potential applications.



MRAD MRAD
EPITAXY OF QUATERNARY INGAALN LAYERS FOR HIGH
PERFORMANCE TRANSISTORS
University Grenoble Alpes – July 7th, 2020

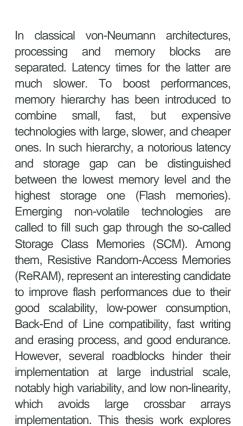
Currently, the CEA-Leti develops GaN based HEMTs on Si wafers using AlGaN barriers. Yet, the growth of InAlN barriers on GaN buffers demonstrated the possibility to surpass the AlGaN on GaN performance. However, the MOCVD growth of high quality, pure and well controlled InAIN barriers in Close Coupled Showerhead (CCS) reactor is difficult. This is due to the serious problem of the nonintentional incorporation of Ga into InAIN barriers, arising from the growth of thick GaN buffers grown beforehand. In this work, we firstly focus on understanding and quantifying the Ga pollution problem in a CCS tool during the MOCVD growth of InAIN barrier layers. We show reduced indium incorporation and increased Ga non-intentional incorporation in the barrier layers along with an increased thickness of these layers as the Ga pollution increases. We propose a for quantitative model observations suggesting that the TMIn precursor reacts with the metallic Ga on the showerhead shield surface to TMGa. which is release incorporated as Ga into the layers. Incidentally, we have also proved that Ga pollution is also occurring during the MOCVD of InGaN layers for the same reason, which is also an important asset for the control of the emissive material in light emitting devices. In the second part of this work and after knowing the origin of the Ga pollution, we discuss the possibility of overcoming it. The Ga pollution was overcome by resorting to: growth interruption before the growth of

InAIN barrier layers, in situ chlorine chamber cleaning and different surface etching processes for the GaN buffer. Although this method was very efficient to avoid the Ga pollution effect on the growth of InAIN barriers, the growth interruption process would however be difficult to implement in an industrial environment where one growth run is preferred. Hence, we had to develop alternative ways to solve the issue. Since the presence of Ga within the shield originates from the condensation of Ga desorbed from the surface of the growing GaN, we have implemented different tests to avoid the condensation from happening. Later we have found that increasing the shield temperature during the growth of the thick GAN buffers would avoid Ga condensation on the shield and so avoid its effect on the growth of InAIN. As a result from this work, we managed to grow well controlled and Ga free InAIN barriers heterostructures with a very low Rsheet value of around 185 Ohm/□. In conclusion, this work constitutes strong steps toward the replacements of conventional AlGaN/GaN barriers, with well controlled, pure and higher performance InAIN/GaN barriers for power and RF applications.

DIEGO ALFARO ROBAYO

INVESTIGATION OF RESISTIVE MEMORIES FOR STORAGE CLASS MEMORY APPLICATIONS

University Grenoble Alpes – September 22nd, 2020



such aspects to increase attractiveness of ReRAM technologies for SCM applications. For the former, endurance variability is addressed at the array level through various measurements over diverse stacks configurations. Results allow to study the impact of programming conditions on failure mechanisms dispersions, leading to the development of a stochastic model based on defects generation inside the resistive layer. As for the non-linearity issue, successful cointegration between best-in-class HfO2 and GeSeSbN Ovonic Threshold Selector (OTS) in 1S1R structures, is demonstrated. Hence, leakage currents compatible with 100Mb-1Gb bank size are obtained. For the first time, to our knowledge, key parameters of OTS+ReRAM systems for high-density crossbar arrays are identified and studied at the statistical level, allowing proposition of further optimizations and opening the way to a whole field of studies which include new materials and circuits to improve 1S1R performances.



JULIEN SOREL

ANALYTICAL ELECTRON TOMOGRAPHY: DATA TREATMENT AUTOMATION AND APPLICATION TO 3D MICROELECTRONICS NANODEVICES. Université Grenoble Alpes – October 2nd, 2020

The development of new technologies, either in consumer electronic domain (smartphones, internet of things...) or in automotive domain (autonomous vehicles), largely boosted the increasing demand of miniaturized and highly performant sensors. Piezoresitive transduction by means of silicon nanowire is particularly interesting to improve detection capability of current sensors. Various benefits of this transduction have been identified for NEMS and MEMS applications, and in particular, high sensitivity and excellent compactness. Moreover, power consumption remains a major issue for miniaturized sensors. Optimized use of nanowires could eventually lead to significant improvement of this transduction mechanism for low power and high performances sensors. Thermal Piezoresistive Back Action (TPBA), highlighted in DC-biased nanowires, allows to finely control electromechanical response and optimize

the transduction mechanism of MEMS. Based on a thermal, electrical and mechanical coupling, this phenomenon particularly allows to reach a self-sustained oscillation regime that could be used to monitor the resonance frequency of a resonator. The objective of this thesis is to study this back action mechanism in nanowires used for M&NEMS components developed at CEA-Leti. A complete study of silicon nanowires properties, whose typical dimensions are 250 nm x 250 nm x 5 µm, allows to evaluate their interest to implement this mechanism. Based on analytical models and finite element modeling, a model of this phenomenon is proposed. Then, it is confronted with experimental results achieved on existing components and others fabricated during this thesis. Finally, a discussion on the perspectives of this study evaluates the gain brought by this mechanism and its potential applications.



ANDREA QUINTERO

DEVELOPMENT AND ELECTRICAL CHARACTERIZATION OF OHMIC CONTACTS ON GESN ALLOYS

Université Paris-Saclay – October 16th, 2020

Efforts on the semiconductor industry are constantly made to improve different parameters like the devices performance or the speed of data transference. To reach these advances, innovative alternatives can be considered: changing the production processes steps, the device architecture or the materials that will constitute the devices. Germanium-Tin (GeSn), group-IV alloy, corresponds to an interesting material to integrate in electronic or optoelectronic devices. GeSn material can be used as source and drain stressor in Ge MOSFETs (metal-oxide-semiconductor field-effect transistors), and as high mobility channels in both pMOSFETs and pTFETs (thin field-effect transistors). On the other hand, the addition of a sufficient amount of Sn in the Ge lattice structure (about 10 at.%) offers the potential to get a direct band-gap structure. This material could be then used to achieve a monolithically integrated group-IV laser that is compatible with Si-CMOS technology (complementary metal-oxide-semiconductor). No matter the application. low-resistive. stable and reliable metallic or intermetallic contacts are key components to inject electric current in the devices. Ni /GeSn intermetallics have been considered as suited contact material for these kinds of applications. This PhD thesis was

therefore dedicated to the systematic and comprehensive development and characterization of Ni / GeSn intermetallics to contact GeSn-based devices. The Ni / GeSn properties analyzed in terms of: phase sequence, morphological and electrical evolution during the solid-state reaction is presented first. As Ni / GeSn intermetallics exhibit a poor thermal stability, different alternatives such as the use of preamorphization by implantation (PAI), the addition of alloying elements (Co, Pt) and the use of laser annealing are also studied to enhance the contact thermal stability. Ultimately, another alternative concerning Ti metallization is also mentioned. Thanks to these studies, a comprehensive and systematic analysis of the Ni / GeSn system was realized. In addition, the identification of different alternatives to modify the process conditions that can enhance the Ni / GeSn system thermal stability was achieved. The results obtained represent a good starting point to elaborate high quality, stable and reliable GeSn-based contacts that can be fully integrated in electronic or opto-electronic devices.

LOUISE BANNIARD

INERTIAL SENSORS WITH OPTOMECHANICAL TRANSDUCTION

University Grenoble Alpes – November 27th, 2020



High performance accelerometers are required in many different domains as sophisticated navigation control systems, research or consumer electronics. A variety of transduction mechanisms has been used to sense the acceleration: capacitive, piezoresistive, thermal... Optomechanical transduction is a promising avenue to realize accelerometers with extremely sensitive readout of mechanical motion with high bandwidth. This also has the advantage of being immune electromagnetic interferences contrary to the traditional transduction methods. In this work, an optomechanical accelerometer is presented which employs Whispering Gallery Modes disk or ring resonator as displacement sensor. The motion of an inertial mass detunes the resonant cavity and thus modulates the optical power at the output of the sensor. The designs and

technological developments of three optomechanical accelerometers are described. We present also the optical and mechanical sensor characterisations. The aim of the thesis is to evaluate the potential of an optomechanical approach for high performance accelerometers.

DAPHNÉE BOSCH

SIMULATION, FABRICATION AND ELECTRICAL CHARACTERIZATION OF ADVANCED SILICON MOS TRANSISTORS FOR 3D-MONOLITHIC INTEGRATION

University Grenoble Alpes - December 17th, 2020

Nowadays, Microelectronics industry must handle a real "data deluge" and a growing demand of added functionalities due to the new market sector of Internet Of Things, 5G but also Artificial Intelligence... At the same time, energy becomes a major issue and new computation paradigms emerge to break the traditional Von-Neumann architecture. In this context, this PhD manuscript explores both 3D monolithic integration and nano-electronic devices for In-Memory Computing. First, 3D monolithic integration is not seen only as an alternative to Moore's law historic scaling but also to leverage circuit diversification. The advantages of this integration are analysed in depth and in particular an original top-tier Static Random Access Memories (SRAM) assist is proposed, improving significantly

SRAM stability and performances without area overhead. In a second time, an original transistor architecture, called junctionless, suitable for 3D-monolithic integration is studied in detail. Devices are simulated, fabricated and electrically characterised for mixed digital/analog applications. In particular, the impact of channel doping density on mismatch is tackled. Also, low temperature (<500°C) junctionless bricks are developed and device optimization trade-off are discussed. In a third time, an innovative 3D structure combining state of the art devices: junctionless stacked Silicon nanowires and Resistive Random Access Memories (RRAM) is envisioned. This technology is proved to enable In-Memory Boolean operations through a so-called "scouting logic" approach.



THOMAS DALGATY BAYESIAN NEUROMORPHIC COMPUTING BASED ON RESISTIVE MEMORY University Grenoble Alpes – November 27th, 2020

Artificial intelligence is a field that, historically, has benefited from the combination of ideas from across interdisciplinary boundaries which have improved models of AI and the algorithms that operate on them. Biological nervous systems in particular have inspired various model topologies and algorithms that have led to leaps in performance. In contrast, as computing power and memory availability have increased relentlessly since the 50's, models of Al have largely failed to recognize the constraints imposed by, or incorporate the opportunities offered by, the underlying computing hardware. Actually the mismatch between model, algorithm and hardware is the limiting factor that currently curtails the efficient application of locally-adaptive AI systems at the edge. In this thesis, the interdisciplinary boundary between machine learning, emerging technologies and biological nervous systems is explored with the objective of proposing a new, hardware-focussed, approach for the application of energy efficient and locally-adaptive edge neuromorphic computing systems. Resistive memories are a leading candidate as an enabling technology for AI to reduce its energy requirements. This is largely owed to the efficient and parallelised implementation of the dot-product operation that pervades machine learning as well as material-level compatibility ranced CMOS. However, advanced application of RRAM has been confined to implementations of gradient-based machine learning algorithms to train RRAM-based multi-layer perceptron models. This thesis recognises that, in contrast, the intrinsic properties of this technology can be harnessed through

Bayesian approaches to machine learning where model parameters are described as random variables. RRAM-based implementations of Markov Chain Monte Carlo sampling algorithms are implemented and applied to the training of RRAM-based models. An RRAM-based computing hardware is also proposed. Inspired by the organisational principles of animal nervous systems, this thesis proposes analogue circuit solutions for biological models of neurons and synapses and for a systemlevel architecture to interconnect such elements. These bio-inspired circuits colocalise memory and computation by incorporating resistive memory devices directly into the circuits, determining model parameters and the interconnectivity between these elements locally. Based on recent neurophysiological studies, models inspired by the cricket cercal system and the fruit fly motion detection system are proposed. It is also discussed how the 'small-worldness' of networks of neurons found in animal nervous systems can provide a solution to the spatial connectivity constraints inherent to the proposed RRAM-based computing.



REBECCA CHAHINE

NANO-ENGINEERING OF CHALCOGENIDE PHASE-CHANGE MATERIALS FOR ULTIMATE PHASE-CHANGE MEMORIES

University Grenoble Alpes - December 1st, 2020

In terms of performance, cost and functional speed, phase-change memories are playing a key role in data storage technologies. Leveraging the properties of some chalcogenide materials, phasechange materials (PCMs) present unique features, mainly: fast and reversible switching between amorphous and crystalline states with significant optical and electrical contrasts between the both However, for an improved elevated power performance. the consumption due to the high programming current must be reduced, and the crystallization temperature also has to be increased. In this context, we have developed new multilayer systems of $[GeTe/C]_n$ and $[Ge_2Sb_2Te_5/C]_n$. The aim is to obtain, in a controlled and reproducible manner, a thin laver of nanostructured PCM with dimensions less than 10 nm. The multilayers were produced by the magnetron sputtering deposition technique in a 200 mm industrial equipment with a multi-cathode chamber. The multilayers are amorphous after deposition. Ion beam techniques permitted to check periodicity and composition of the multilayers. The sheet resistance and reflectivity as a function of temperature were measured in situ. The crystallization temperature of PCM in the multilayer structure increases and is dependent on the thickness of the PCM layer and that of the carbon films. The kinetics and magnitude of the amorphous-crystal transition of PCM in

the multilayers are also significantly affected. The impact of the multilayer structure on the crystallization of GeTe versus Ge₂Sb₂Te₅ is then compared and discussed with respect to their crystallization mechanism. We show that the initially amorphous multilayer structure is retained even after PCM crystallization during an annealing that is identical to the one used for the manufacture of memory devices (300 °C for 15 min). Thus, it is possible to obtain nanocrystalline grains of PCM in amorphous C on the order of 4 nm vertically and 20-30 nm in the layer plane. These results are compared with the microstructure of C-doped GeTe and Ge₂Sb₂Te₅ films. Finally, by using X-ray diffraction measurements in laboratory and by in situ experiments at the SOLEIL synchrotron, we were able to follow the evolution of the structure of these multilayers during annealing. For example, we reported that a local percolation effect of the GeTe grains between the layers of C occurs above a certain temperature.



FLORE BOYER

CMOS-COMPATIBLE CONTACT INTEGRATION ON III-V MATERIALS FOR SI PHOTONICS APPLICATIONS IN 300 MM

University Grenoble Alpes - December 7th, 2020

In the present context of the Big Data era, the requirement for higher density data transmission is of the utmost importance, since the demand in terms of data exchange has been growing for over 20 years. As a result, innovative means of communications have inevitably emerged, as optical devices and interconnections. The later consist in technologies such as emitters (laser) and receptors (photodetector), made from III-V materials and integrated onto 300 mm CMOS Si-based circuitry: this what Silicon photonics is about. The latter indeed offers the possibility to meet the growing demand in data exchange, while (i) leveraging the benefits offered by the maturity of the 300~mm CMOS Si fabline, such as highvolume production and low cost, combined with (ii) the use of optical circuitry made from III-V materials, granting reduced power consumption and high-performance chips. In the scope of optimizing the performances of such optoelectronic circuit, an innovative integration scheme has been in developed collaboration STMicroelectronics and CEA-Leti. It consists in the full integration of the III-V emitter, which is a III-V/Si hybrid laser, onto a silicon wafer in a 300-mm CMOScompatible clean room. One of the key components required for such integration is the development of CMOS-compatible contacts on both n-lnP and p-In_{0.53}Ga_{0.47}As, which are the n- and pcontact layers of the III-V/Si hybrid laser, necessary for the generation and amplification of the optical signal. In this way, the goal of this PhD thesis lies in the

development of these innovative contacts, meeting specific requirements, and allowing the full integration of the III-V/Si hybrid laser onto a 300 mm Silicon Photonics wafer. In this way, the eligibility of four metallization, hence eight systems, are thoroughly investigated. The systems are namely Ni/In_{0.53}Ga_{0.47}As, Ni_{0.9}Pt_{0.1}/InP, $\label{eq:Ni0.9} Ni_{0.9}Pt_{0.1}/In_{0.53}Ga_{0.47}As, \quad Ti/InP \quad and \quad Ti/InP$ $In_{0.53}Ga_{0.47}As$. To do so, the formation phase sequence, layer morphology, element distribution and electrical properties of the enounced systems are studied. In addition, a reliability study has been performed on the systems, providing valuable and exclusive information regarding the evolution of the properties of the systems throughout subsequent process steps such as W-plugfilling and Back-End-Of-Line, as well as throughout the emulation of long-term thermal stress. Ultimately, a promising and reliable metallization is proposed for the full integration of the III-V/Si hybrid laser onto a 300~mm Si fab-line.



EDOUARD VILLEPREUX

CHARACTERIZATION OF OXYGEN IONS IN RESISTIVE MEMORIES WITH ELECTRICAL BIAS USING ADVANCED ELECTRON MICROSCOPY TECHNIQUES

University Grenoble Alpes – December 8th, 2020

As storage capacity requirements are ever greater, research on emerging memory device technologies and their development is booming. Among the emerging memory devices, this thesis is interested in resistive oxide-based random-access memories (OxRRAM). The movement of oxygen ions during the electrical switching of this type of memory is still very poorly understood and knowing it would help to improve and optimize these devices. An operando TEM analysis protocol has allowed the development of an experimental method dedicated to the characterization of variations in oxygen ions distributions during the electrical polarization of this kind of stack. The sample holders, on which the sample preparation used depends, as well as the artefacts to be taken into account during operando switching, have their own specificities. For this, three TEM sample holders dedicated to electrical polarizations in operando TEM were presented, that of NanoFactory, Hummingbird, and finally Protochips. An EELS hyperspectral image processing protocol based on the VCA algorithm has been developed and applied to two types of memory stacks. The first one is a reference memory stack based on

SrTiO₃ on which two studies have been made. A first study of this type of stacking was carried out on previously acquired data, the results of which have already been published with a stack based on crystalline SrTiO₃. This first analysis confirmed the correct working of the hyperspectral image processing protocol. A second analysis was carried out on a memory stack based on polycrystalline SrTiO₃, little known. The STEM-EELS operando analysis of this second sample was carried out through the use of the Protochips microarray associated with the data processing developed, allowing to learn more. This second analysis shows that the use of this data processing based on the VCA algorithm can provide additional information to conventional processing. The second type of stack studied is a La₂NiO₄-based memory device, designed for applications in the field of neuromorphic applications due to its volatile behavior. The characterization and data processing protocols developed during this thesis can thus serve as supports for the studies of other micrometric-sized memory devices.



OUSMANE MAGATTE KANE

HIGH-FREQUENCY NOISE AND CIRCUIT PROPERTIES OF ADVANCED FDSOI TRANSISTORS

University Grenoble Alpes – December 17th, 2020

Fully-Depleted Silicon-on-Insulator (FDSOI) is one of the industry technologies architected to meet the requirements of emerging mobile, Internet-of-Things (IoT), and RF applications. It is a competitive alternative to the FinFET technology in all applications where brute-force computational power is not the unique primary concern, but where endof-the roadmap device performance is counterbalanced by strict low-power/low-consumption requirements. FDSOI has also a definite advantage over competitors in simplicity and costs, due to reduced mask-count (impacting process complexity and cost) and similarity to bulk MOS devices (reducing time and effort to port/adapt existing design to the technology). A main driver for the technology adoption is the possibility of implementing in FDSOI with direct integration with the digital content of all or part of the RF circuitry that are necessary to interface the product to the outside world. Recent publications have demonstrated impressive RF figure-of-merit for FDSOI devices with Ft/Fmax reaching 400GHz. Therefore, it has viable potentials for mmW applications such as 5G. However, today's state-of-the art back-end-ofline (BEOL) interconnect poses a good amount of incertitude on the RF behavior of the devices because of the multiple layers of thin metallic interconnections but also because of the size of the devices, more specifically 20nm technology node in the present thesis. Therefore, an important part of the thesis was on assessing the impact of the BEOL on said state-of-the-art devices. This included the impact on the S-parameters as well as the high-frequency noise in the millimeter wave range. Developing deembedding methodologies was key for this purpose. Proper modeling of the BEOL in order to understand the distribution of the losses in the BEOL was pursued together with an extensive effort in geometry optimization of the device and its layout. Dedicated layout which took fully advantage of backgate (back-biasing) were implemented and investigated. The final part was on characterizing the channel noise mechanism of these devices, which is departing from the thermal noise assumptions and espousing more the shot noise paradigm, which is important in semi-ballistic and ballistic transistors.

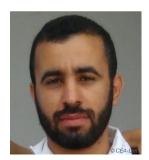


BAPTISTE NEFF STUDY AND DEVELOPMENT OF MEMS COMPONENTS FOR BIOLOGICAL APPLICATIONS

University Grenoble Alpes – December 17th, 2020

Vibrating systems offer more and more applications with liquid environment both as sensors and actuators. Immersed systems suffer from a high damping compared to a use in vacuum or air. In our approach, thanks to the use of piezoelectric actuators placed on a glass structure, antisymmetric Lamb waves are generated within the glass. In their subsonic regime of propagation, Lamb waves do not radiate in liquid and thus are not damped and exhibit a lossless behavior. Electromechanical characterizations are performed in different liquid configurations to determine the resonance frequencies, quality factors and displacements generated by the Lamb waves. Two proof of concept are presented. The first one is to use Lamb waves as a sensor to determine simultaneously density and viscosity of liquid. The developed sensor as shown to

be adapted to measure density and high viscosity thanks to its low losses and high factors in highly quality viscous environment. The second proof of concept demonstrated in a biological environment is the creation of patterns on a population of adherent living cells in culture. Thanks to acoustic forces in liquid generated by vibration it is possible to create millimetric lines of exclusion for adherent cells on the glass substrate. Dimensions of the established patterns depends on various studied parameters including Lamb wave order. The described method allows a contactless manipulation of living cells for studies about cell migration. This work shows a new approach of the use of Lamb waves used as sensor or actuator for applications in a fluidic or biological environment.

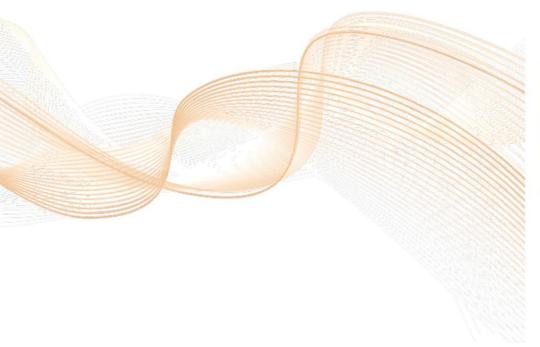


BARIK EL MOSTAFA
STUDY OF CU/SNAG SYSTEM INTERACTIONS IN THE CONTEXT OF TLPB
ASSEMBLIES FOR POWER ELECTRONICS DEVICES

University Grenoble Alpes - December 18th, 2020

electronics is continuously developing thanks to microelectronic technological advances. Thanks to the emergence of new power devices based on WBG (Wide Band Gap) materials, more powerful electronic systems could be developed. WBG devices, such as GaN and SiC, bring new challenges for the packaging. In the present work, we have studied the Cu/SnAg assemblies by Transient (TLPB) and solid state reaction (SSR) that allow to increase the stability temperature (Tstab) of the joint. The aim of this work is to study first the physicochemical transformations in the Cu/SnAg/Cu joints at 250-350°C until the total transformation of Sn into intermetallic compounds ε-Cu₃Sn and η-

Cu₆Sn₅. These transformations lead to an increase of Tstab from 227°C (melting point of SnAg alloy) to 404°C (peritectic decomposition temperature of η phase), thus ensuring high reliability. In this context, interfacial Cu/liquid Sn interactions have been studied to evaluate the growth kinetics as well as the morphological and microstructural evolution of intermetallic compounds and to determine the involved physicochemical mechanisms. A similar study has been carried out for solid state interactions between Cu and Cu₆Sn₅ that allow to transform the joint into Cu₃Sn compound which is a stable phase up to 726°C.



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