Electronics

Photonics

Annual Research Report 2014

Optics and Photonics

Welcome

Leti is an institute of **CEA**, a French research-and-technology organization with activities in energy, IT, healthcare, defence and security.

By creating innovation and transferring it to industry, Leti is the bridge between basic research and production of micro- and nanotechnologies that improve the lives of people around the world.

Backed by its portfolio of 2,200 patents, Leti partners with large industrials, SMEs and startups to tailor advanced solutions that strengthen their competitive positions. It has launched more than 50 startups. Its 8,000m² of new-generation cleanroom space feature 200mm and 300mm wafer processing of micro and nano solutions for applications ranging from space to smart devices. Leti's staff of more than 1,700 includes 200 assignees from partner companies. Leti is based in Grenoble, France, and has offices in Silicon Valley, Calif., and Tokyo.

Visit http://www.leti.fr/en for more information

Within CEA-Leti, **Optics and Photonics** activities are focused principally on big industrial markets of photonics: various wavelengths imaging (visible, infrared, THz), information displays, solid state lighting, optical data communications, optical environmental sensors. The R&D projects are performed with industrial and academic partners. The industrial partners of the Optics and Photonics department range from SME to large international companies. The projects are merging fundamental aspects with advanced technological and industrial developments; nanosciences are connected with material sciences, optics, electronics and micro & nano-fabrication.

Contents

Edito

Ludovic POUPINET
Head of Optics and Photonics Division

Dear Reader

The Optics and Photonics Division (DOPT) of LETI is focused on a few selected photonic applications where technology and integration strongly impact the final products. The expected impact could be through decreasing the cost, improving the performances or increasing the number of functions.

Photonics is recognized as a Key Enabling Technology by the European Union and attracts a lot of interest and efforts from industrial companies and research institutions throughout the world. Staying on the leading edge of photonics requires strong relationships both with industrial partners, through one-to-one or collaborative projects, and with academic partners, through strategic alliances and collaborative projects as well.

Our strong will to build a bridge between academy and industry is illustrated in this report by several results co-authored with both kinds of organizations/companies. Furthermore, we also extend the frontiers of photonics by benefiting from the multidisciplinary environment of LETI and CEATech and their wide expertise and technological capabilities.

I hope that reading this report will make you want to know even more about us, meet us during conferences, professional forums or LETI Days, join us as a researcher, a PhD or a post-doctoral fellow and, of course, build fruitful collaborations on exciting research topics tackling the behavior of photons at small scale using up to date industry compatible facilities.

Have a nice reading!

Key figures

- **185 permanent researchers**
- **35 PhD students and Post-docs**
  - **32 CEA experts: 2 directors of research**
- **and 3 international experts**

100 publications in 2014 including 35 papers in peer reviewed journals. One hundred of additional publications were co-authored with other divisions, universities and private companies

- **65 patents filed in 2014**
- **430 patents portfolio with 20% under licence**

Clean rooms dedicated to imaging & photonics fabrication, tests and component packaging.

- **Optics and opto-electronics characterization facilities**
- **Modeling and simulation**

Scientific activity

Awards

Anthony LEFEBVRE received the award for the best student paper at the SPIE Photonics Europe conference for his presentation *"Optimization of a radiative membrane for gas sensing applications"*

Michel KHOURY received the award for the best student paper at the SPIE Photonics Europe conference for his presentation: "*Growth of Semipolar GaN on Patterned Silicon Substrates for LED Applications*"

Books
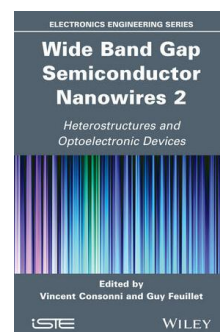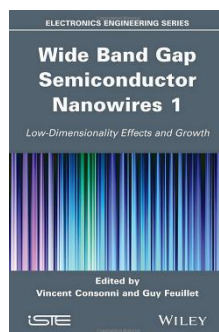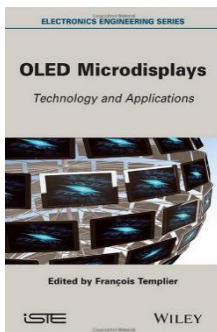
➕ François TEMPLIER edited the book *" OLED microdisplays : technology and applications"* with the participation of Karim BOUZID, Tony Maindron, David VAUFREY, published by Wiley.

➕ Guy FEUILLET co- edited with Vincent CONSONNI (CNRS) 2 books: "*Wide band Gap Semiconductor nanowires 1 and 2"* with the participation of Pierre TCHOULFIAN and Pierre FERRET, published by Wiley.

Conferences and Workshops organization

• Jean- Marc FEDELI with "Group Four Photonics" (Paris 2014)

• Yvon CAZAUX and Bruno MOUREY for "SEMICON" (Grenoble 2014)

1

Infra-Red maging:
Cooled detectors

HgCdTe Epi. growth, photodiodes design

Avalanche single photon detectors (APD)

HgCdTe focal plane arrays: SWIR, LWIR

Small pitch, hybridization, optics

A new nBn IR detection concept using HgCdTe material

Research topics : Quantum IR detection

O. Gravrand, F. Boulard, Ph. Ballet, W. Hassis

ABSTRACT: This paper presents a new HgCdTe based heterostructure to perform high performance quantum IR detection. The structure is based on the unipolar barrier heterostructure grown by MBE mimicking the valence band structure of a classical photodiode. The aim is to simplify the fabrication process, and drastically decrease the dark noise at low temperature. The concept has been studied by FEM simulation and showed promising results. First experimental characterization of the EO properties of such structures showed promising features: 60% quantum efficiency and low turn-on voltage have been measured on single pixels.

In a conventional photodiode, the minority carrier collection is done using the electric field of the p-n junction's space charge region. This electric field usually induces leakage current in the narrow gap materials used for the IR detection. We have been working on a new detection concept using a MBE grown unipolar barrier structure. The driving idea is to use the flexibility of HgCdTe (which is a narrow gap semiconductor material suitable for absorption in the IR) grown by molecular beam epitaxy (MBE) to mimic the valence band structure of a p/n photodiode while maintaining the high field into a larger band gap material (the so called barrier) thus limiting current leakage of the structure. The band gap difference between narrow and large gap has to block the flow of electron on the conduction band while facilitating the flow of holes on the valence band (see fig1). The resulting unipolar device therefore behaves like a diode and might be used for IR photovoltaic detection.

Our original barrier design makes use of graded interfaces tailored during the MBE growth in order to optimize the band diagram. This nBn detection structure is based on an asymmetrical barrier design with a uniform N type doping level through the whole structure. In this design, a graded barrier is used to manage the valence band offset and therefore facilitate the flow of minority carrier thru the structure thus optimizing the quantum efficiency of the resulting detector.

The valence band residual barrier (and the associated turn-on voltage) is managed using a graded barrier interface on the absorbing layer side. This interface has to remain as abrupt as possible on the contact side to get the highest effective barrier on the conduction band, therefore limiting thermionic currents. This structure has been extensively studied by FEM simulation to get the optimal design profile, best tradeoff between diffusion turn on voltage, GR bias and thermionic currents. At last, this structure has been grown by MBE and processed into 30µm pitch nBn pixels. Test chips hybridized on Silicon fanouts and backside illuminated demonstrated good detection performances. However, SIMS analysis showed that the grown layer composition profile was different from the targeted barrier profile. The contact layer has a larger gap and the barrier contact interface was not as abrupt as estimated. As a consequence, experimental IVs showed stronger thermionic currents than previously computed. Yet, low diffusion turn-on voltages have been observed. Experimental bariodes exhibited 60% QE, with diffusion limited spatial behavior.

Last but not least, measured spectral responses showed expected triangular response shapes, indicating a uniform QE on a large spectral band.

The work opens the gate to high yield in the fabrication of ultra-low dark current focal plane arrays in the IR range.
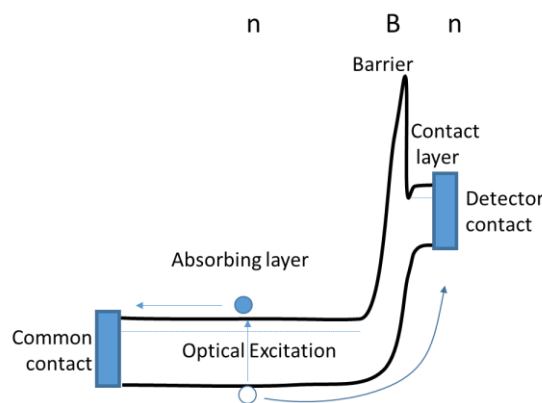
Figure 1 : Principle of the barrier structure (nBn)
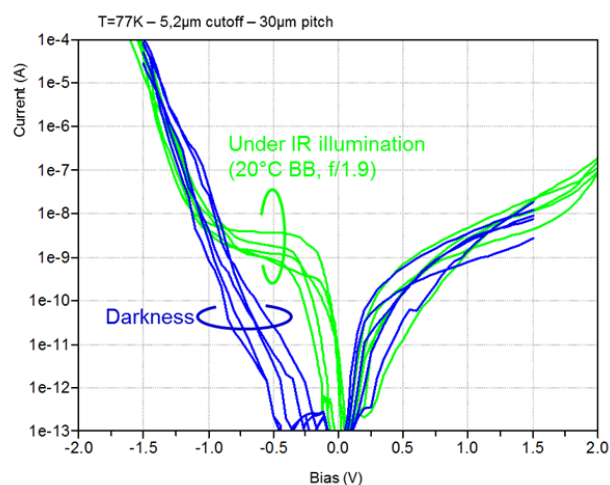
Figure 2: Experimental I(V) curves measured on nBn test structures

Related publications:
[1] O. Gravrand, F. Boulard, A. Ferron, Ph. Ballet, W. Hassis, "A new nBn IR detection concept using HgCdTe material", to be published in Journal of Electronic Materials 2015 [2] L. Lolis, T. Ayed, C. Bernier, M. Pelissier, D. Dallet, J. B. Bégueret, "Ultra Low Power Bandpass Sampling Architectures Using Lamb Wave Filters", IEEE NEWCAS, 2010.
[2] W. Hassis (2014). "Etude de structures avancées pour la détection IR quantique à haute température". Thèse Université de Grenoble

Study of systemic 1/f noise in HgCdTe IR photodiodes operated at high temperature

Research topics : Quantum IR detection, flicker noise

O. Gravrand, J. Rothman, W. Hassis

ABSTRACT: The narrow band gap on which IR detection relies requires cooling of focal plane arrays to cryogenic temperatures. In practice, increasing the operating temperature (for power issues of future portable detectors) leads to an increase in low frequency noise of the photodiodes leading to performance degradation. Therefore 1/f noise has been investigated on a very large set of IR HgCdTe photodiodes with different gaps, different dopings and various temperatures. The results of this study are trends for future optimization for high operating temperature focal plane arrays.

The dark current of IR photodiodes is highly depending on operation temperature. As a consequence, the operating temperature is usually very low, down to cryogenic temperatures for MWIR range (up to 5 µm wavelength) and LWIR (up to 10µm). However, today trend is to operate those detectors at higher temperatures and it appears that the first limiting parameter is the appearance of 1/f at high temperatures, rather than the dark current shot noise. This effect limits in fact the noise defect rate of focal plane arrays at lower temperatures than expected from the calculated dark current values and must be therefore deeply investigated.

We studied 1/f noise in MWIR and LWIR VHg-doped n+/p photodiodes with different geometries, epitaxial layer thicknesses, and doping concentrations. Contrasting 1/f noise behavior was observed in diodes operating in the different wavelength ranges. Noise measurements performed on MWIR photodiodes revealed a new type of 1/f noise mechanism, in which the noise was directly proportional to the total current generated inside the effective photodiode area. This previously unobserved type of 1/f noise is generated in the bulk of the photodetector and has an area dependence that may be explained by the modulation of the diffusion current amplitude, which itself increases with the square of the distance to the junction. This new 1/f noise mechanism led us to the development of a phenomenological relation that is reminiscent of the 1/f Hooge model. This relation involves an experimental constant, which we supposed to be related to a volumetric defect density. For LWIR photodiodes, it was found that the noise current density is independent of the diode area at constant temperature, contrary to the behavior observed in MWIR diodes (scaling with A) and also different from that expected according to the various models, which scale with $A^{1/2}$ or $A^{1/4}$. The increase of the noise current density due to the increase in temperature revealed that the noise is due to the modulation of a quantity that is proportional to the diffusion current generation rate, i.e., to n_i^2. The origin of this modulation seems not to be related to the diode geometry. The modulation of the space charge region at the junction singularities at the corners of the square diode implants may be the origin of this interesting behavior.
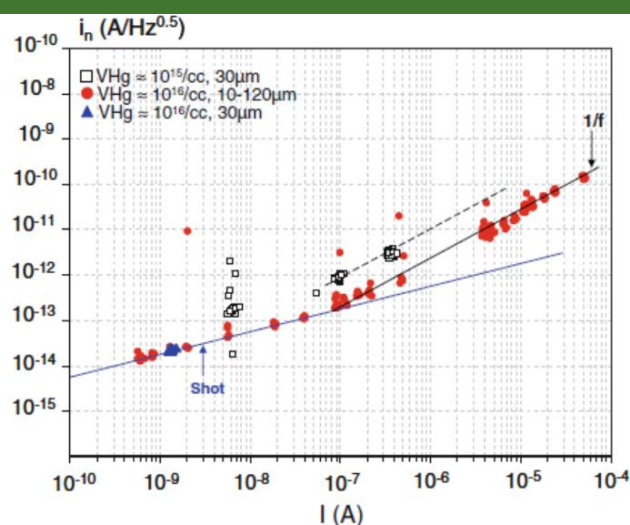

Figure 2: Noise measurements of MWIR n+/p LPE photodiodes with Different doping concentrations.
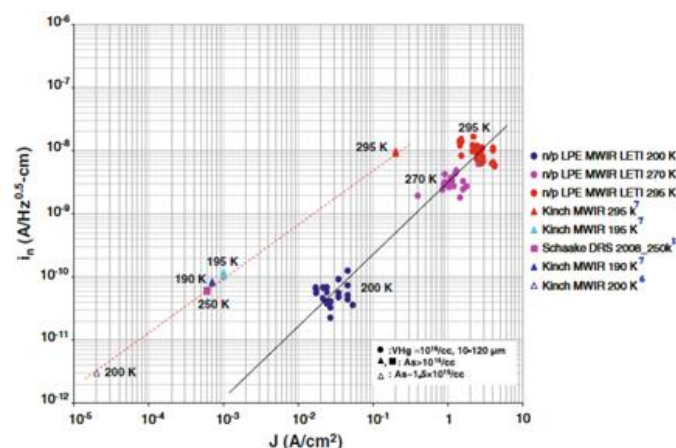
Figure 3: Normalized Noise current density versus total current for HgCdTe diffusion-limited diodes.Noise measurements of MWIR n+/p compared between different manufacturing companies

Related publications:
[1] Hassis, W., Gravrand, O., Rothman, J., & Benahmed, S. (2013). "Low-Frequency Noise Characteristics of HgCdTe Infrared Photodiodes Operating at High Temperatures. Journal of Electronic Materials", 42(11), 3288–3296.
[2] Gravrand, O., Destefanis, G., Bisotto, S., Baier, N., Rothman, J., Mollard, L., Vuillermet, M. (2013). "Issues in HgCdTe Research and Expected Progress in Infrared Detector Fabrication". Journal of Electronic Materials, 42(11), 3349–3358.
[3] Hassis W. (2014). "Etude de structures avancées pour la détection IR quantique à haute température". PhD Dissertation Université de Grenoble

Optics and Photonics

Sub-wavelength photonic structure to add spectral capabilities to MWIR HgCdTe photodiode

F. Boulard, O. Gravrand, L. Adelmini, D. Fowler, G. Badano, P. Ballet, M. Duperron, R. Espiau De Lamaestre

ABSTRACT: we present simulation and experimental results on the design and integration of sub-wavelength photonic structures to add spectral functionalities to MWIR HgCdTe photodiodes. The relationship between the metallic grating design and the excited optical mode is illustrated using numerical simulations. The agreement with the measured spectral response and dispersion relation on a test photodiode array is discussed. Finally, first results from a MWIR FPA are presented with operability as high as 99.7%.

During the last decades, thanks to its tunable band gap and small lattice parameter variation, multispectral Mercury Cadmium Telluride (MCT) heterostructures have been grown and processed to cover the whole IR range from short to long wave infrared, with intra or extra-band detection[1]. However, this approach is based on complex heterostructures with deep etching requirements increasing growth [2] and processing challenges [3] on small gap materials. Suitably designed metal dielectric nanocavities are promising candidates to add spectral capabilities on planar absorbers [4]. This paper presents experimental results on the integration of such a sub-wavelength photonic structures.

Molecular beam epitaxy mid-wave MCT layers are grown on CdZnTe substrates. Diodes are fabricated following standard n on p (vacancy doped) technology while a specific e-beam lithography and etch step is added to define metal dielectric nanocavities inside the passivation layer. Specific care is taken to minimize field stitching misalignments since the focal plane array area is larger than the electron beam field.

After processing, diodes arrays were hybridized on a silicon fan-out and characterized at 77K. Fig 1 shows a normalized spectral response on a backside illuminated MCT photodiode test array.
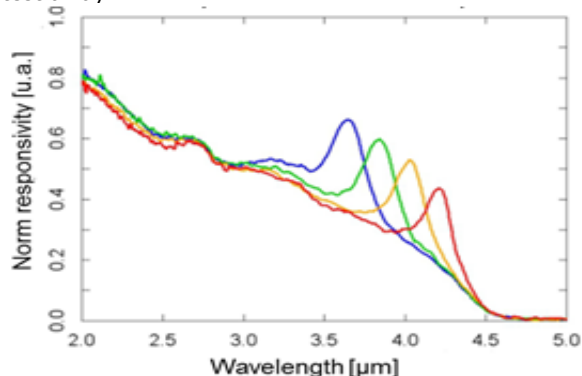

Figure 1 : Normalized spectral response of 4 colors MWIR HgCdTe photodiode test array

Tuning the nanocavitiy periods allows the spectral control of the responsivity enhancement. However, in such a design, the absorption wavelength maximum exhibits a strong dependence on the light incidence angle, as shown by the resonance splitting on the simulated (RCWA) and experimental dispersion diagram on the left side of fig2. An improved design allowing larger angular acceptance (fig 2, right) is implemented on a four color MWIR QVGA (320 x 256) 30 µm pitch FPA, with various pixel design on 160x128 subareas.
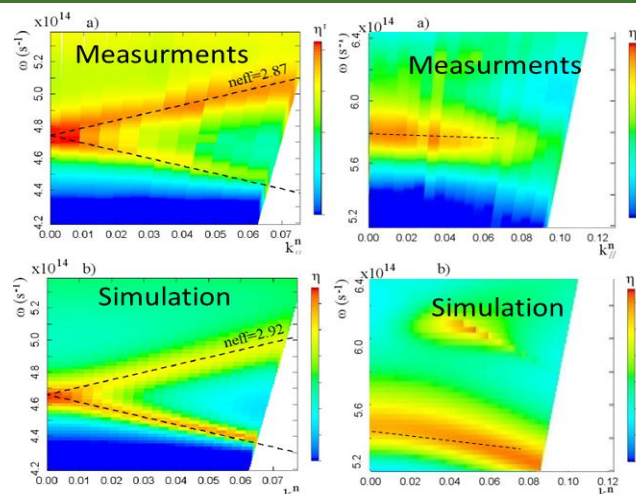

Figure 2 : Simulated and measured dispersion diagram (w,k//) of (left) diffractive and (right) hybrid IR incoming light coupling with HgCdTe absorber.

Under typical test conditions (T°=77K, FOV=30°, C=2,1pF, Tint5.5ms, T°bb=300K and 310K), the pixel responsivity check pattern (fig3 inlet) underlines the spectral capabilities given by the addition of the photonic structure. An FPA noise histogram is compared to theoretical shot noise on fig 3. The distribution is centered on 1 without a tail, representing excellent operability (±50% criterium) greater than 99,7%, and demonstrating the process quality, from MCT layer growth to color device processing.
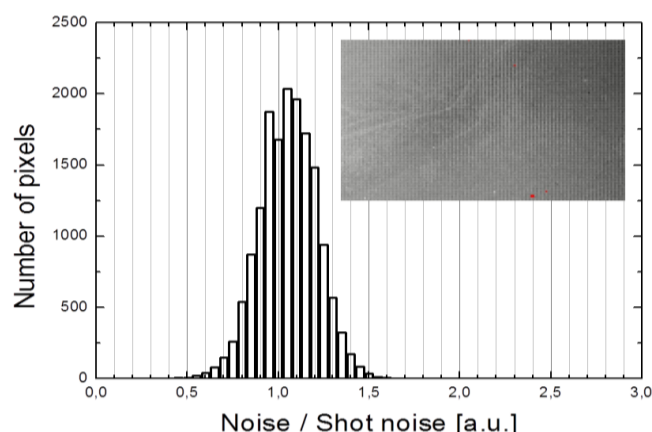
Figure 3 : Noise to shot noise ratio histograms and responsivity mapping (inlet) of 4 colors 30 µm pitch MWIR 128x160 FPA at 77K

Related publications:
[1] J. Baylet, et. al., Study of the pixel-pitch reduction for HgCdTe infrared dual-band detectors, J. Electron. Materials, 33 (6) (2004).
[2] P. Ballet, et.al., Dual-band infrared detectors made on high-quality HgCdTe epilayers grown by molecular beam epitaxy on CdZnTe or CdTe/Ge substrates J. Electron. Materials, 33 (6), 667-72 (2004).
[3] F. Boulard, J. Baylet, C. Cardinaud, Influence of cadmium composition on CH 4-H 2-based inductively coupled plasma etching of Hg 1-xCd xTe J. Electron. Materials 39 (8), 1256-61 (2010).
[4] D.Fowler & al. Partially localized hybrid surface plasmon mode for thin-film semiconductor IR photodetection Optics Letters 38 (2013)

Very-long wavelength infrared detection with HgCdTe for space applications

N. Baier, O. Boulade* (* CEA/ IRFU/ SAP)

ABSTRACT: New technological design and improved growth process of HgCdTe have been evaluated to determine performances of p/n photodiodes in specific conditions. For space applications, long cutoff wavelength (up to 17µm) and very low dark current (low light flux conditions) are required. Quarter VGA format focal plane arrays have been tested and exhibit good performances: 17.2µm cutoff and state-of-the art dark current at 78K has been obtained with high operability (<0.1% defects) and homogenous mapping. Dark current reference model in literature has been revisited at low temperature (>20K) with these results.

The p-on-n photodiodes architecture relies on an In-doped HgCdTe active base layer grown on a lattice matched CdZnTe substrate by horizontal-slider Liquid Phase Epitaxy (LPE). This process grants a homogenous cadmium composition, critical in the very-long wavelength IR spectral band as a small variation in composition will result in a large variation of cutoff wavelength. p-on-n junction is made with ion implantation of As.

A new heterojunction process has been evaluated [1], designed to reduce depletion dark current (typically generation-recombination) and the temperature at which this kind of current becomes larger than diffusion current. Moreover, this heterojunction places interface between active layer and passivation in a larger bandgap, thus lowering the defects impact on performances (operability and homogeneity). The challenge here is to control the depth of the LPE heterojunction as if it is placed too deep, it may result in the formation of a potential barrier which will lower the quantum efficiency.

Two sets of detectors have been manufactured. The first one has a cutoff wavelength of 17.2µm at 78K, highest value obtained on this kind of structure in literature. Focal plane array (quarter VGA format) operability is 99.7% and quantum efficiency near 70%. Electronic noise is limited by photon noise. Dark current density is at the state of the art.
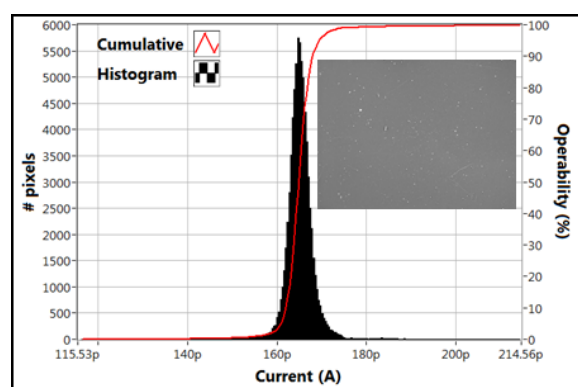

Figure 1: Photonic current histogram and mapping obtained on quarter VGA format array.

The second set of detectors has been manufactured to fulfill specific requirements for space astrophysics: low flux detection at low operating temperature (to reduce dark current).

Cutoff wavelength is 12.5µm at 40K. Operability is over 99.9%, the best result has been obtained on an array with heterojunction process, better than with standard homojunction process. This new process shows its benefits in terms of stabilization of photodiodes performances. Quantum efficiency is above 80%. Dark current tends to be in good agreement with "Rule07" model at 78K [Tennant, W.E & al," Journal of Electronic Materials 37 (9) (2008)].

This heuristic model is a reference for p-on-n HgCdTe infrared detectors. However, at lower temperatures, results measured on arrays presented above and on other ones realized by different manufacturers [McMurtry, C. & al, Optical Engineering 52 (9), 091804-1 (2013)] are not following this model. The dark current tends to vary with a pure diffusion model with the temperature down to 42K, reaching $6 \cdot 10^{-10}$ A/cm². At this point, the dark current is limited by another regime, based on a depletion current behavior with an ideality exponential factor of 4.2. At 23K, dark current is $8 \cdot 10^{-13}$ A/cm² (45 electrons/s in a pixel of 30µm pitch). This results meets the requirements given for space applications low flux detection.

Further investigations will be done on new detectors to understand the origin of the limiting current regime at low temperature. With improvements of the process, we may manage to decrease this transition temperature.
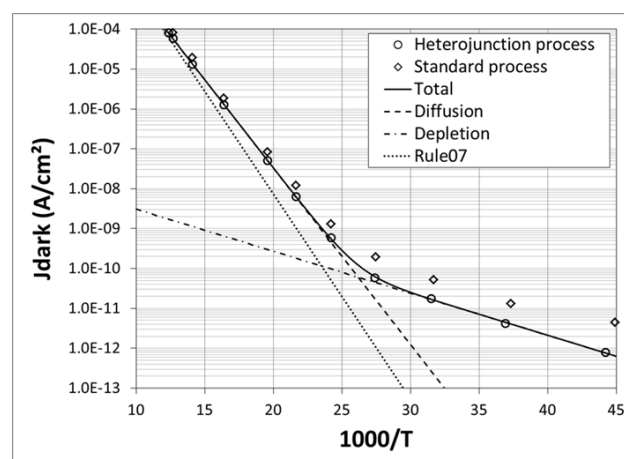

Figure 2: Dark current densities as a function of 1000/T. Comparison between measurements and models.

Related Publications:
[1] Baier, N. et al., "MCT planar p-on-n LW and VLW IRFPAs," Proc. SPIE 8704, 87042P (2013)

Demonstration of a 10µm pixel pitch XGA HgCdTe focal plane array

S.Bisotto, F.Marion, M. Volpert, F.Guellec*, Y. Reibel** (*LETI/DACLE, **Sofradir)

ABSTRACT: Small pitch large focal plane arrays are now available in HgCdTe technology, 15µm being the standard industrial pitch; academic studies have proved a potential benefit provided by going to smaller pitches, as far as 5 µm.
The 10µm pitch XGA demonstrator presented here is a n-on-p HgCdTe HOT technology focal plane array operating in the mid-wave infrared (MWIR).
The overall development has been carried out with Sofradir, french IR detectors manufacturer. A first demonstration of the Sofradir device was performed at Baltimore SPIE 2014.

Reducing the pixel pitch and increasing the focal plane array size are two conjugate tendencies that have proven to have benefits, not only in producing very compact products, but also in providing a better image resolution [2] without degrading NETD and pixel operability at high temperature. Considerable efforts have been carried out at LETI and Sofradir in technology improvement in order to solve the related issues, more particularly the noise operability for HOT operation, as well as hybridization techniques at small pitches [3]. The 10µm pitch pixel takes advantage from these studies, with a reduction on dark current, and an increase in operating temperature over 110K.

The development of this demonstrator has been carried out by Sofradir and LETI. The difference between the two approaches resides mainly in the hybridization technique. The standard Sofradir process is based on indium microbumps formed on the Si ROIC (Read Out Integrated Circuit) side; Sofradir has presented a demonstrator at Baltimore SPIE 2014 prefiguring Sofradir's DAPHNIS line [1].
An alternative low thermal budget process, working at room temperature, is developed by LETI, and is especially suitable for ultra-small pitch. The LETI demonstrator is the first HgCdTe large array successfully hybridized with this technique. A 2kx2k 10µm pitch HgCdTe mechanical demonstrator is expected this year.

The pixel architecture is based on a DI stage, with a 2Me-well. The ROIC enables to read out 1024x768 10µm pitch photo diodes, in snapshot mode, up to 20MHz. The integration mode is either integrate-then-read (ITR) or integrate-while-read (IWR), and the operational temperature is 90K to 130K.
The power consumption is kept low thanks to circuitry implemented in dual analog-digital threshold voltages. It has been measured at 80mW at 10MHz (102 nW/pixel).

The electro-optical performances of the demonstrator are quite good: at an aperture of F/#2, the NETD at 50% well fill is 26mK at 110K (see figure 1) and remains stable up to 130K. The residual fixed pattern noise (RFPN) is below the temporal noise.
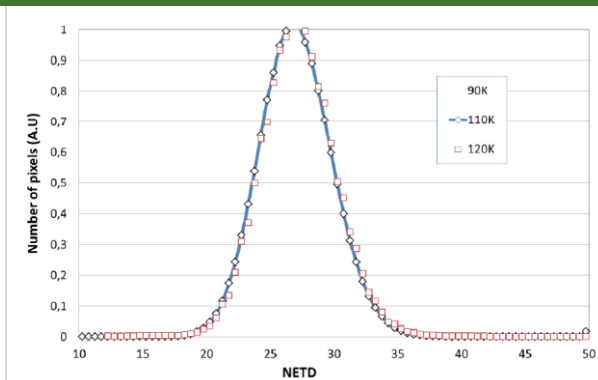

Figure 1: NETD at 50% well fill Tpf=110K from the Sofradir device

The LETI hybridization process enables an excellent operability with an exceptional reliability: after ageing for 15 days at 80°C and 2000 thermal cycles from +20°C to -180°C, the operability is 99.99% for opens and the short rate is 0.035%. Moreover the electro-optical performances remain unchanged.

Figure 2: IR image from the LETI demonstrator

Related Publications :
[1] Y. Reibel, N. Pere-Laperne, T. Augey, L. Rubaldo, G. Decaens, ML. Bourqui, A. Manissadjian, D. Billon-Lanfrey, S. Bisotto, O. Gravrand, G. Destefanis, G. Druart, N. Guerineau: "Getting Small, new 10µm pixel pitch cooled infrared products" , Proc. Of SPIE Vol. 9070, 2014
[2] O.Gravrand, N.Baier, A. Ferron, F. Rochette, J. Berthoz, L. Rubaldo,R. Cluzel: "MTF Issues in Small-Pixel-Pitch Planar Quantum IR Detectors", Journal of Electronic Materials 10.1007/s11664-014-3185-3, 2014
[3] O. Gravrand, G. Destefanis, S. Bisotto, N. Baier, J. Rothman, L. Mollard, D. Brellier, L. Rubaldo, A. Kerlain, V. Destefanis, and M. Vuillermet: "Issues in HgCdTe Research and Expected Progress in Infrared Detector Fabrication", Journal of Electronic Materials, vol. 42, n° 11, pp. 3349-3358, 2013

3D modeling of Flip-Chip assemblies

Research topics: Flip-Chip, 3D numerical simulation, high count ball grid array

W. Kpobie, P. Lipinski*, N. Bonfoh*, M. Fendler, C. Dreistadt* (* ENIM, Metz, France)

ABSTRACT: we present an original approach for 3D numerical simulation of fine-pitch high-count ball grid flip-chip assemblies. With the increase of the resolution of imagers, the interconnection layer of flip-chip assembly includes more than 1 million solder micro-balls (10 µm in diameter) at fine pitches down to 10 µm and the optimization process of such structures through numerical simulations turns out to be a very time-consuming task. For such configurations, we propose an alternative approach, which consists in replacing this heterogeneous interconnection layer by a homogeneous equivalent material (HEM) which thermomechanical properties are determined by using homogenization methods.

The most sensitive area of a flip-chip electronic assembly is the interconnection layer, which, for example, in the case of an infrared detector, connects the readout and detection circuits (each being about 500 µm thick). This heterogeneous layer is composed of a very large number (over one million) of solder bumps with small dimensions (about 10 µm diameter), with or without adhesive (e.g., epoxy) underfill (Fig. 1). Numerical modeling of such a structure may generate a large number of degrees of freedom and requires the use of powerful supercomputers. Faced with this problem, we proposed an original approach, which consists in replacing this interconnection layer (solder bumps embedded in an epoxy matrix) by a macro-HEM. For this purpose, thermoelastic homogenization schemes can be used to estimate the effective properties of such a fictitious HEM.
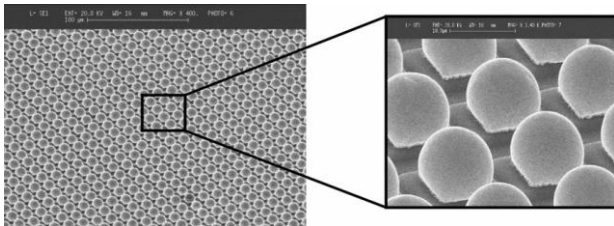

Figure 1 : Fine-pitch (15 µm) indium microbumping

To take into account the thermomechanical interactions between the local phases of this heterogeneous interconnection layer, multisite micromechanical modeling (Mori-Tanaka approximation) of the effective thermoelastic properties of heterogeneous materials, based on the corresponding general thermoelastic integral equation, has been proposed [1].

The developed micromechanical model was then implemented in the finite-element code Abaqus Standard via the user subroutine UMAT.

The considered flip-chip assembly for a megapixel array consists of 1280 × 1024 bumps at 15 µm pitch (Fig. 2).
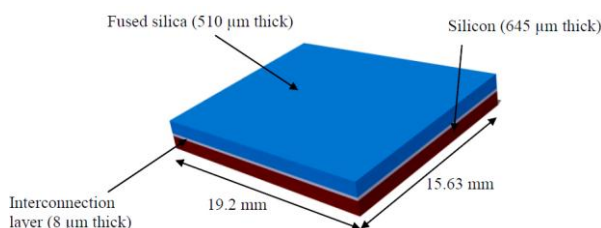

Figure 2 : Description of the assembly studied

Predictions of the implemented model with the HEM are analyzed in terms of the vertical displacement as depicted in Fig. 3a. The corresponding maximal deflection on the fused silica surface is about 24.2 µm. This simulated result is compared with experimental measurements (Fig. 3b), carried out with an optical chromatic confocal surface analyzer (Altisurf© 520).
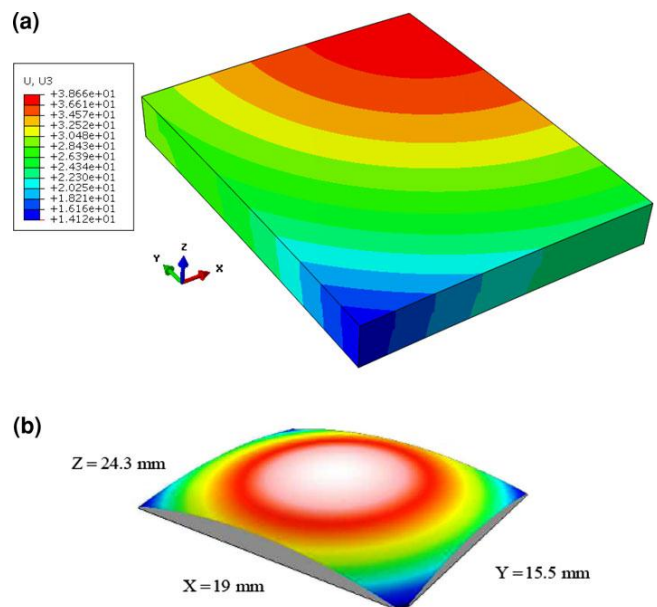

Figure 3 : Vertical displacement U3 (µm): (a) megapixel model and (b) experimental deflection measured on a megapixel dummy sample (fused silica/silicon substrates)

These measurements were performed on six samples of the megapixel flip-chip assembly. For these tested samples, the measured vertical deflection is distributed between 19.4 µm and 24.3 µm (with average of 21.53 µm). The relative error between the results of the numerical simulation and the experimental measurements is less than 12.4% [2].

To estimate the stress and strain fields in the indium bumps, submodeling was used for structural zoom. Applied to a megapixel-format assembly, it revealed that local stresses are maximal in the vicinity of the interfaces between solder bumps and the chip. Cracks are therefore expected to initiate in this area of the flip chip because of the presence of IMC formed during soldering.

Related Publications :
[1] W. Kpobie, S. Ben Khlifa, N. Bonfoh, M. Fendler, and P. Lipinski, "Multi-site micromechanical modelling of thermo-elastic properties of heterogeneous materials," Compos. Struct., vol. 94, no. 6, pp. 2068–2077, 2012.
[2] W. Kpobie, N. Bonfoh, C. Dreistadt, M. Fendler, and P. Lipinski, "Three-Dimensional Thermomechanical Simulation of Fine-Pitch High-Count Ball Grid Array Flip-Chip Assemblies," J. Electron. Mater., vol. 43, no. 3, pp. 671–684, 2014.

Optics and Photonics

Overview of curved and flexible image sensors at LETI

Y. Gaeremynck, E. Hugot, K. Tekaya, A. Vandeneynde, A. Gueugnot

ABSTRACT: we present an overview of developments in curve and flexible image sensors based on CMOS chips. A first part presents applications, with a focus on a wide field imaging system currently under fabrication. Second part presents results obtained for infrared sensors as well for micro-bolometers as for cooled quantum sensors. Last part details flexible sensor for visible wave length, the assembly of this sensor is under patent procedure.

Research topics: CMOS Image sensors, Optics, mechanics

The emergence of curved detectors, first proposed by Ko et al in their Nature paper [Ko et Al. Nature (letters), 454, 748-753, 2008], certainly represents the major disruptive technology for imaging systems that will come up in a near future. This technology is very versatile and can be integrated to enhance existing systems as well as to allow full new applications.

For example in existing systems, it is possible to simplify imaging system and enhance image definition as we compensate Petzval field curvature with the image sensor. Petzval field curvature is one of the main optical aberrations, it affects in particular wide field imaging systems. That is why we demonstrated competitive advantage of this technology on a fish-eye zoom. With comparable performances as a patented 8-15 mm/4 professional Canon zoom [Okumura T. & al, patent EP 2407809A1], the introduction of curved sensor allowed a reduction of necessary lenses, from 14 to 9, glass types, from 11 to 3 and suppressing the 2 aspherical surfaces. We notice far better optical tolerances with sensitivity to defects divided by 4. This optical system has been fabricated to makes a first full optimized optical system using curved sensors. The system will be full characterized in coming months.
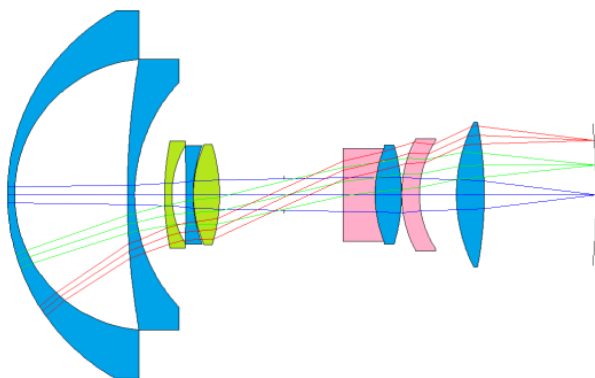

Figure 4 : side view of simplified fish-eye imaging system. The simplification of optical design is obtained thanks to introduction of curved sensor.

A second example for innovative systems, curved sensors allow also innovative systems like wide field multi-pupillar systems. In this case by taking advantage of the curvature of the sensor, the introduction of micro-prism matrix becomes obsolete.
First results of curvature were obtained by D. Dumas and M Fendler [1].

They realized spherical and cylindrical shapes both on micro bolometers and cooled infrared detectors. In all cases the chip is thinned to reach less than 100 µm of thickness. Under this condition, we get fully operating micro-bolometer chip of 1 cm² up to a spherical curvature radius of 80 mm. these chips are made of full silicon. The team performed the same process of curvature on hybrid cooled infrared arrays. These arrays are composed of silicon and CdHgTe chips Notice that CdHgTe is a very brittle material that implies high difficulties to curve it. Nevertheless, we also reach 200 mm spherical curvature radius and 100 mm cylindrical curvature radius. These sensors performed image shots at 80 K attesting the operability [2].

Figure 5 : Picture obtained with spherical curved cooled infrared CMOS array.

Based on these good results, we carry on developing a very reproducible curvature system, allowing also adjustable radius of curvature of the sensor. In a partnership with LAM (Laboratoire d'Astrophysique de Marseille) we developed 3D printed carrier adapted to images sensors. These carriers are the results of finite element simulations; in addition to image sensor the assembly is currently under patent procedure.

Related Publications:
[1] D. Dumas & al" Curved focal plane phetector array for wide field cameras » applied optics (51) 22, 2012
[2] K. Tekaya et Al. "Hemispherical curved monolithic cooled and uncooled infrared focal plane arrays for compact cameras" DSS SPIE, 90702T, 2014

High operating temperature SWIR HgCdTe APDs for remote sensing

Research topics : High sensitivity photo detection, avalanche photodiodes, LIDAR

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ABSTRACT: Large area high operating temperature HgCdTe avalanche photodiode detector modules have been developed for remote sensing of gazes and free space optical telecommunications. The detectors with an active optical diameter of about 200 μm are cooled in a dedicated vacuum packaging using thermo-electric cooling (TEC) to operating temperatures around 200 K. The use of HgCdTe APDs with high linear gain and low excess noise factor made it possible to achieve record high sensitivity for such versatile detectors, with noise equivalent powers of 30 fW/√Hz for bandwidth ranging between 20 and 300 MHz.

HgCdTe APDs have been shown to exhibit close to optimal amplification properties characterized by an exponential increasing linear gain as a function of reverse bias, up to multiplication factors higher than 1000, close to negligible excess noise and a response time which is not dependent on the gain. These characteristics have opened new perspectives in most fields of low photon number detection at wavelengths reaching from the UV to the Infra-Red (IR) detector cut-of wavelength. The high performance of HgCdTe APDs is principally due to multiplication through impact ionization which is exclusively initiated by the electrons. All laboratories capable of making functional HgCdTe APDs are mainly focused on imagery. This fact concentrated the first developments of detector modules on high performance focal plane arrays. However, a large number of applications, such as remote sensing using LIDAR and free-space optical telecommunications (FSO) do the measurement of the temporal variation of the photon-flux on a single element detector. The detectors described in this paper are the result of the first efforts at Leti, supported by a Carnot project and by CNES and ESA, to develop such detectors based on a versatile and potentially low cost approach.

The required temporal resolution in most LIDAR and FSO applications ranges between 50 ns to 250 ps, corresponding to bandwidths between 10 MHz and 2 GHz. The active optical diameter depends on the receiver optics and is typically in the range of 80 to 200 μm. These specifications define the parameter space in terms of Cd composition, operating temperature, sensitivity and active area. The sensitivity is ultimately limited by the dark noise of the APD, induced by the dark current and residual thermal flux. The noise of these contributions should be lower or equal to the input referred noise of the pre-amplifier. In the present development, we have chosen to work with detectors cooled down to temperatures around 200 K. This allows using thermo-electric cooling (TEC), in ground based applications, or passive cooling, in space applications. In order to obtain the lowest possible temperature and largest optical active area, we have chosen to deport the amplifier off the cold-down surface rather than to hybridize the APD on the amplifier. This choice implies a higher amplifier noise which needs to be overcome by a higher APD gain. This choice enables a lower operating temperature of the APD and is versatile, as it allows changing the APD cut-off wavelength and surface with a given amplifier and/or the amplifier with a given APD as a function of application requirements. The performance of the detector module can be predicted taking into account the TIA noise, the expected APD dark current and residual thermal radiation [1]. We have shown that the equivalent input noise reaches values below 10 photons per characteristic time for the aimed operating temperature and detector areas. Such sensitivities open a new horizon of applications which requires resolving the temporal variation of faint IR signals, such as LIDAR, FSO and range finders.

Figure 1 : Photography of the inside of a HgCdTe APD detector module.

Figure 1 shows a photograph of the detector assembly. A large packaging has been used that allows keeping the TIA inside the packaging to reduce the influence of parasitic impedances and RF noise pick-up. At present, we have developed two detector modules using a low BW TIA (20 MHz for LIDAR detection of greenhouse gases, with CNES), and a high BW TIA (300 MHz for FSO with ESA or range finding). Figure 2 illustrates the measured gain and equivalent input noise of the high-bandwidth detector. At a gain of 100, the equivalent input noise is close to 10 photons. At this limit, the detector noise generated by the detection of residual IR light starts to limit the sensitivity and lower noise can be achieved using optical filters. Nevertheless, this value corresponds to a record low noise equivalent input optical noise (NEP) of 34 fW/√Hz. An equally record low NEP of 30 fW/√Hz was measured on the lower BW detector [1]. The next step of the present development is the space qualification of the LETI HgCdTe APD technology, in collaboration with CNES, and the optimization of the APD bandwidth for high data rate FSO.
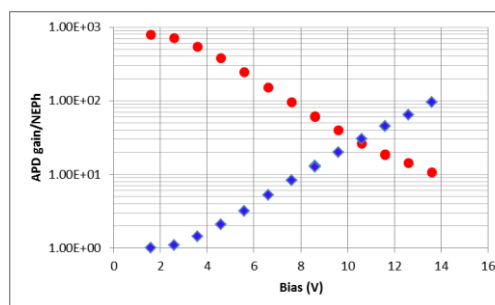

Figure 1 : Variation of the detector gain and input equivalent photon noise of the high BW detector module developed for FSO in collaboration with ESA

[1] J. Rothman, et al., "High operating temperature SWIR HgCdTe APDs for remote sensing" Proc SPIE, DSS, 9254P, (2014)

Lunar Laser Communication Demonstration (LLCD) using HgCdTe APDs

J. Rothman in collaborration with European Space Agency (ESA) and the German Aerospace Center

ABSTRACT: This paper presents the results of the Lunar Laser Communication Demonstration using a receiver module made with a large area HgCdTe APD detector manufactured at CEA/Leti. The receiver was used to detect and decode a position pulse modulated (ppm) 40 and 80 Mbit/s signal emitted from Nasas Space craft LADEE. Error free data transfer was demonstrated for both modes when the average power corresponded to more than 40 photons per laser pulse. Gbps data transfer rates can be expected in detector modules with optimized sensitivity and bandwidth.

Figure 1 : Illustration of the laser emission of PPM data from the LADEE space craft, orbiting the moon, to earth ©Nasa.

Free space optical communications is considered to be a key enabling technology to access data at high rate both from satellites orbiting the earth and for deep space mission beyond the moon. The interest in FSO is motivated by the capacity to send data higher rates than in radio communications using smaller and lighter components which consume less. In addition and in opposite to the crowded radio spectrum, the IR spectrum is free of use for commercial applications. The Lunar Laser Communication Demonstration was launched by Nasa in 2008 to demonstrate the maturity of FSO for very long range high data rate laser communications to and from the moon [1]. ESA joined the project in 2011, with the aim to evaluate the maturity of commercially existing components for long range FSO. CEA/Leti joined the project in the beginning of 2013, when ESA concluded on the lack of detectors which could decode the faint signals at high speed. Thanks to a development already undertaken in an internally funded CARNOT program, we were able to deliver in time for the LLCD demonstration a detector module with a bandwidth (80 MHz) associated with a record low noise equivalent power (NEP) of 0.59 nW [2].
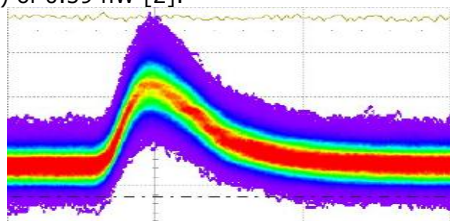

Figure 2 : Impulse response of a 160 µm diameter APD coupled with TIA-1, operated at T=190 K with a gain of M=95 to an impulse of 100 photons. The vertical and horizontal scales are 5 ns and 10 mV per division, respectively.

The data emitted from the moon was encoded using 16ary pulse position modulation (PPM) with pulse durations from 3.2 ns (Mode 5, decoded transmission rate of 39 Mbits/s) down to 0.2 ns (Mode 1, decoded transmission rate of 625 Mbits/s) by modulating a CW laser with an average power of 0.5 W. The expected average power on the detector is around 300 pW, corresponding to about 120 photons per pulse during Mode 5 modulation. Fig. 2 illustrates the response of the detector to this signal level in the lab. At this power the signal is much larger than the noise and an error free detection can be expected.

The performance of the APD detector module was first tested as a function of input average power using laboratory generated Mode 5 and Mode 4 modulated light. Fig. 3 reports the variation of the symbol and decoded frame error rate as a function of the average power on the detector. Error rates below 10^{-5} were achieved for average optical power down to 100 pW, which corresponds to 20 photons per decoded bit in mode 5. Due to bandwidth limitations of the detector, the mode 4 required higher optical power, at least 200 pW to achieve error rates below 10^{-5}. A stable error free Mode 5 (40 Mbits/s) down link was first demonstrated on 3/4/2014 for an operation lasting over 9 minutes. A Mode 4 down link (80 Mbits/s) was demonstrated later the same day.

The data obtained at OGS should be compared with the results obtained by NASA using super-conducting nanowire single photon detectors (SNSPD operated at 2 K), which have been optimized for LLCD by the Lincoln lab at MIT [1]. Error free down-link connexion was demonstrated even in mode 1 (625 Mbits/s) for average signal levels down to 2 photons per pulse [D.M. Boroson et al., Proc. SPIE 8971 (2014) 89710S]. To compete with this performance we need to improve the sensitive and the bandwidth of the HgCdTe APD detectors. Our measurements have shown that 10 GHz BW should be improved with HgCdTe APDs detectors and the sensitivity can be increased by the hybridization of the APD on a CMOS circuit [1]. These perspectives imply that HgCdTe APDs are strong candidates for space and ground based Gbit/s FSO.
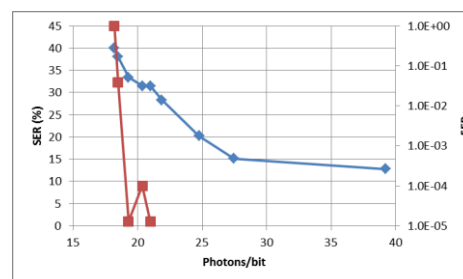
Figure 3: Mode 5 Symbol error rate (SER) and frame error rate (FER) as a function of the number of photons per decoded bit after error correction.

Related Publications :
[1] Zayer, I, J. Rothman et. al., Lunar optical communications link (LOCL) demonstration between NASA's LADEE spacecraft and ESA's optical ground station, Int. Conf. on Space Operations, SpaceOps Proc. 2014, (2014)

2

Infra-Red imaging:
Microbolometers

Room temperature IR detectors

Multispectral: IR to THz range

Focal plane arrays: small pitch

Pixel Level Packaging arrays

Latest improvements in microbolometer thin film packaging: paving the way for low cost consumer applications.

J.J. Yon, G. Dumont, V. Goudon, S. Becker, A. Arnaud and S. Cortial*, C.L. Tisse* (*ULIS)

ABSTRACT: Silicon-based vacuum packaging is a key enabling technology for achieving affordable uncooled Infrared Focal Plane Arrays (IRFPA) required by a promising mass market that shows momentum for some extensive consumer applications; such as automotive driving assistance, smart presence localization and building management.
Among the various approaches studied worldwide, CEA, LETI in partnership with ULIS is committed to the development of a unique technology referred to as PLP (Pixel Level Packaging). In this PLP technology, each bolometer pixel is sealed under vacuum using a transparent thin film deposition. As a result, PLP operates as an array of hermetic micro caps above the focal plane, each enclosing a single microblometer.

Over the last 20 years, the uncooled microbolometer IRFPA technology has plainly emerged in the infrared (IR) imaging business. Most current products cover the pixel range from 160x120 to 1024x768 with a pitch as low as 17µm [1] [2]. More recently, the success of the microbolometer technology has attracted new interest for IR sensors of lower resolution for addressing a large set of smart applications that cannot comply anymore with conventional PIR-based motion sensors because of their very limited pixel count and sensitivity.
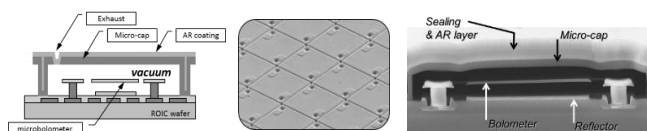

Fig. 1: PLP architecture. Schematic view (left); SEM top view (center); SEM cross section view (right)

However, the cost target for these new markets imposes the need for a technological breakthrough, mainly in regard to the vacuum packaging which remains an adverse cost driver for the microbolometer technology. In this context, CEA, LETI has been involved for several years in the development of such a disruptive packaging technology referred to as PLP (fig. 1). Toward this objective, CEA, LETI and ULIS have been developing a PLP-based thermal IR sensor with a resolution of 80x80 pixels featuring the right performance-cost tradeoff for the targeted applications.
Typical performance for 80x80 PLP-IRFPA is reported below in Table1. Its performance is compared to the one obtained from a previous development carried out on a 320x240 PLP-based IRFPA [3]. Both PLP-IRFPA feature a pixel pitch of 34µm.

Parameter	Performance	
Format	QVGA (320x240)	(80x80)
Pitch	34µm	34µm
Spectral range	8-14µm	8-14µm
Frame rate	60Hz	120Hz
Responsivity (mean value)	10.2mV/K	14.3mV/K
Temporal NETD (F/1)	77mK	73mK

Table 1: PLP-IRFPA performance characteristics (2 different formats)

All measurements are performed at room temperature with F/1 optical aperture and integration time of 65µs. The frame rates are 60Hz and 120Hz, respectively to comply with the format of each PLP-IRFPA. The IR responsivity is calculated from the output signal measurements with respect to the flux delivered by two blackbodies set at 293K and 303K respectively.

The flux is limited to the usual 8-14µm spectral range with the use of a germanium frontal window whose both sides are coated with an antireflective film.
For both formats, the PLP-IRFPA exhibits high responsivity as an evidence that a high vacuum level is reached. NETD values are around 75mK and fully in line with the product requirement (<100mK).
To push forward the technology, much effort was devoted to improve its robustness and yield. The technology has currently achieved excellent repeatability, high uniformity along with pixel operability typically better than 99.7%. These results translate into high image quality. Figure 2 shows a comparison of IR images obtained from the two products (at 50Hz, with F/1 optics)
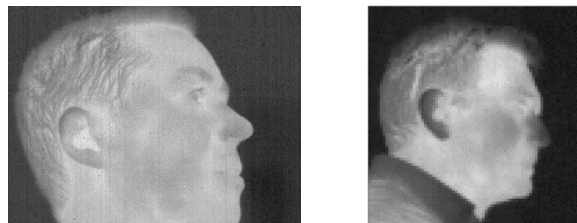

Fig 2: PLP infrared imaging ability. QVGA IRFPA (left); 80x80 IRFPA (right) with a pitch of 34µm

The right IR image in figure 2 features 80x80 pixels with a bad pixel rate as low as 0.27%. It should be emphasized that bad pixels are only related to electrical defects, without any occurrence of vacuum defects. This result demonstrates that PLP is a disruptive technology that is ideally suited for high yield, cost-effective production of medium-format IRFPA.

Beside its compliance with the currently targeted market, PLP turns out as a scalable technology to address a broad set of applications. Its pixel-wise architecture gives a natural and straightforward scalable capability as a function of pixel count (see Fig. 2). Moreover, the scalability of the technology was also demonstrated through the achievement of two different pixel designs which differ by their thermal insulation. In both cases, the product of NETD by the thermal time constant is unchanged and amounts to 550mK.ms. This major outcome, indicates that thermal insulation of a PLP pixel is essentially controlled by the leg's thermal conduction rather than the residual vacuum level. It is a key point to further address the reduction of the pixel pitch. A reduction of the leg width from 0.8µm down to 0.3µm is expected to suffice for the reduction of the PLP pixel pitch from 34µm to 17µm, respectively.

Related Publications :
[1] Yon J.J. et al, "Latest amorphous silicon microbolometer developments at LETI-LIR", Proc. SPIE Vol. 6940, 69401W, 2008.
[2] Fieque B. et al, "Uncooled amorphous silicon XGA IRFPA with 17µm pixel-pitch for high end applications", Proc. SPIE Vol 6940, 69401X, 2008.
[3] Yon J.J. et al, "320x240 uncooled IRFPA with pixel wise thin film vacuum packaging", Proc. SPIE Vol. 8541, 85410D, 2012.

Uncooled Terahertz bolometer arrays and camera

Research topics : THz, micro-bolometer, imaging, spectroscopy, Mie scattering in

F. Simoens, F. Guellec*, J.L Ouvrier-Buffet, S Martin, S Pocas, and J. Meilhan (*LETI/ DACLE)

ABSTRACT: Thanks to its mature know-how in thermal infrared bolometer sensors, CEA-Leti has designed and fabricated proprietary uncooled QVGA terahertz bolometer arrays with unique antenna-coupled architecture. The characterization of the prototyped arrays integrated in a camera has demonstrated state-of-the art sensitivity in video camera operation mode.
Real-time active imaging capabilities have been tested in several set-ups. In particular THz spectro-imaging has been demonstrated for discrimination of sugar powders compressed in pellets. The Mie scattering at terahertz frequencies in powder materials has been specifically studied in order to extract the spectral signatures necessary for spectro-imaging analysis.

For several decades, cooled bolometer imaging arrays have been developed for ambitious spatial programs and extremely sensitive bolometer FPA are being operated in low-background platforms or satellites for scientific researches. Some institutes are now trying to decline this know-how to larger volume applications, with some promising demonstrations like the video-rate THz camera developed by the VTT-NIST collaboration.

Nevertheless, even if uncooled bolometers are much less sensitive than cooled thermal sensors, they are in a position to meet easily large-scale commercial market. In particular, thanks to the maturity of the bolometer technology, THz-customized room temperature bolometers can potentially suit many applications that require 2D sensors with low cost in production (standard Si microelectronics) and operation (no cooling), compactness (monolithic), and 2D real-time & advanced image functions (array above CMOS). And indeed, uncooled microbolometer focal plane arrays (FPAs) are nowadays recognized as a relevant technology for fast 2D imaging compact, with commercial hand-held cameras by NEC or INO. The reader of this paper is invited to refer to the chapter written by Leti for a general review of bolometers for THz sensing ([1])

Thanks to its strong know-how in thermal infrared bolometer sensors, CEA-Leti has designed and fabricated proprietary QVGA terahertz bolometer arrays with unique antenna-coupled architecture (Figure 1).
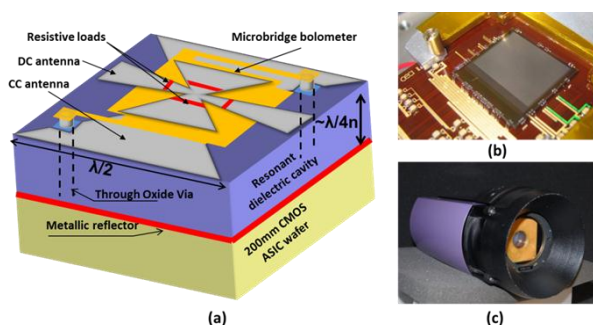

Figure 1 : Uncooled THz antenna & cavity coupled microbolometer pixel structure (a). Prototyped 320x240 pixel array chip (b). Camera prototype integrating the THz bolometer array in its vacuum packaging (c). (extracted from reference [2])

The characterization of the prototyped arrays integrated in a camera (b & c of Fig 1) has demonstrated state-of-the art sensitivity in video camera operation mode : a minimum detected power par pixel of the order of 30 pW has been measured at 2.5THz.

Real-time active imaging capabilities of the prototyped 2D FPAs have been tested in several set-ups, both in reflection and transmission configurations. In particular THz spectro-imaging applied to the discrimination of sugar components has been demonstrated with fructose, glucose and lactose powders compressed in pellets imaged in reflection conditions (a in Fig 1). The spectro-imaging method combines multicolor THz images and a data base of the spectral reflectivity of these materials (refer to b of Figure 2).
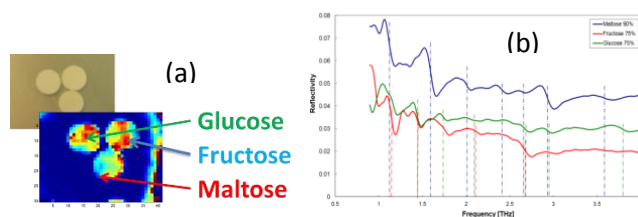

Figure 2 : (a). visible and THz image of the sugar pellets (b). Spectral reflectivity of the sugar components characterized in collaboration with the University of Savoie (IMEP-LAHC)

The acquisition of this data base requires careful experimental preparation and data analysis. In particular the University of Savoie and CEA-LETI have studied the scattering effect in the powder materials with grain size of the order of the wavelength [3]. In such conditions, scattering effect cannot be well predicted by the simple models like the one by Raman or by the Christiansen approach: modelling using Mie theory is necessary in order to describe the absorption and scattering phenomena, and to evaluate its contribution to the THz power attenuation in the powders. For typical sub-millimeter size particles, the scattering contribution reaches 80~90% of the total power attenuation, even at frequency for which the particle material shows a rather strong absorption. The scattering contribution to the total losses greatly depends on the particles characteristics as size, distribution, shape, intrinsic refractive index and absorption. These models have been applied in order to extract the spectral fingerprints of sugar powders.

Related Publications :
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[2] F.Simoens and J.Meilhan, "Terahertz real-time imaging uncooled array based on antenna- and cavity-coupled bolometers", Phil. Trans. R. Soc. A 28 March 2014 vol. 372 no. 2012 20130111; doi:10.1098/rsta.2013.0111, (2014)
[3] F. Garet, M. Hofman, J. Meilhan, F. Simoens and J.-L. Coutaz, "Evidence of Mie scattering at terahertz frequencies in powder materials", Appl. Phys. Lett. 105, 031106 (2014); http://dx.doi.org/10.1063/1.4890732

Optics and Photonics

Demonstration of large field of view fast scanning based on a real-time uncooled antenna & cavity coupled bolometer array camera

F. Simoens, J.L. Lalanne-Dera, S Martin, S Pocas, S Gidon, W Rabaud and J. Meilhan

ABSTRACT: Real-life applications of terahertz (THz) systems often require fast imaging of large field of view of opaque scenes. Such features have been demonstrated by the development of a complete reflection active THz imaging system that combines QCLs as sources and antenna & cavity coupled micro-bolometer as THz video camera. While better than 1 mm resolution images of 40x60 mm² illuminated surfaces are acquired in real-time, a rotating planar mirror provides fast scanning of large areas, e.g. 20 x 30 cm2 in less than 10 seconds. This paper gives an overview of the developed system and video demonstrations.

Uncooled microbolometer focal plane arrays (FPAs) tailored specifically for THz sensing are nowadays recognized as a relevant technology for fast 2D image acquisition by compact and hand-held cameras [1]. The LETI/ DOPT has developed and fabricated innovative 320-240 bolometric arrays: bolometric pixels that are coupled to antennas and a resonant quarter-wavelength cavity are processed above CMOS wafers with fully standard Si microelectronics technology. Broadband sensing and better than 30 pW NEP have been demonstrated in video mode in the 2-4THz range [2].

In order to demonstrate the capability of this camera in close-to-real life application conditions, a complete system [3] has been developed to provide fast scanning of large field of view of opaque scenes. We reported spectro-analysis of single image acquired by this system [4]. This paper emphasizes the fast acquisition of large field resulting from the tiling of images.
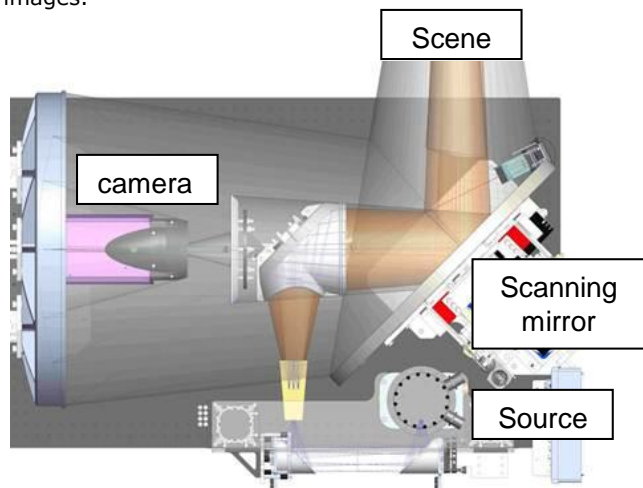

Figure 1 : Large field of view fast scanning demonstrator scheme

The demonstrator combines a QCL THz source, an optical system and an uncooled bolometer camera, each of these components being optimized for operation in the vicinity of 2.5 THz (Fig. 1).

The scanning of the scene is ensured by a reflective mirror located on an alt-azimuth mount.

Thanks to a confocal scheme, this movement ensures simultaneously fast illumination and collection of the signal reflected by the scene. Then a 80 cm paraboloid mirror focuses the beam onto the camera FPA with an equivalent f/0.8 relative aperture.

Figure 2 : Visible (the shirt has be removed for clarity) and THz image of a objects hidden under a shirt on a human trunk

The mirror is successively moved to cover the targeted large FoV. For each mirror position a switched source ON/OFF acquisition of the scene is operated by the camera that delivers the differentiated frame. The single image that is then acquired in real-time corresponds to 40x60 mm² illuminated surfaces.

The fast actuator and mechanical configuration of the system were optimized in order to dump vibrations during displacement of mirrors. The camera allows the scanning of a human trunk, typ. 20x30cm2, in 10 seconds.

High spatial resolution –i.e. less than 5mm- of hidden objects under a shirt has been achieved (Fig. 2).

This work has demonstrated that uncooled THz cameras can be applied to fast scanning of large areas in reflection configuration. Such features are suitable to many applications in different domains where opaque materials and objects are hidden by obscurant.

Related Publications :
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[4]. J. Meilhan, et al., 'Reflection 2D real time THz camera to image and identify sugar pellets', IRMMW-THz Conf., 2013, doi : 10.1109/IRMMW-THz.2013.6665499

3

Optical environmental sensors

Gas detection in Infra-Red

Non-dispersive IR sensors

Integrated photo-acoustic sensors

S. Nicoletti, P. Barritault, S. Boutami, M. Brun, A. Glière, P. Labeye, M. Carras*, G. Maisons*
J. Czarny, H. Lhermet (* III-V Lab)

ABSTRACT: We present a compact optical gas sensor working in the MID-infrared by assembling a multi-wavelength QCL source with a small photo-acoustic cell (~ few cm3). The multi-wavelengths source is composed of QCL (Quantum Cascade Laser) array coupled to photonic combiner. QCL array have been fabricated through an original approach that greatly simplifies the fabrication anf improves the yield. The wavelength of each laser can also be selected independently after the growth of the epitaxial layers. Low loss waveguides based on SiGe alloy have been achieved with losses <1dB/cm at 4.5 μm, <1.5 dB/cm at 5.65 μm and <2dB/cm 7.4 μm. Mini acoustic Helmholtz cavities enabling a differential measurement have been designed and made by micro machining.

Research topics: gas sensing, quantum cascade laser, MIR photonics

The photo-acoustic detection is based on the generation of an acoustic wave induced by the absorption of a laser pulse. This absorption is due to the excitation of rovibrational energy levels of molecules in the mid-infrared. The absorbed energy is restored in the form of a transient heating, which generates a pulse wave measured by a microphone. The amplitude of the wave is directly related to the concentration of the compound in the ambient gas.

The QCLs sources were quickly considered well suitable for this kind of analysis technique. Indeed QCL wavelength range between 3μm and 11μm corresponds to most gases of interest (alkane, Volatile Organic Compounds, sulfur oxides and nitrogen oxides)[1]. Moreover, the power exceeds several mW, improving hence the limit of detection (LOD). QCLs coupled to photonics circuits, specifically engineered to guide the light over the spectral range, enable to achieve multi-wavelengths source for an efficient spectroscopic analysis of gas mixtures. Since each molecule has a distinct absorption spectrum which represents a unique "signature", the choice of a given adsorption peak or of a characteristic band of the spectrum allows to detect the chemicals and to estimate their concentration. The paper presents some major achievements toward the miniaturization of such an optical sensor fabricated by merging on the same chip different functionalities spanning from integrated optics, fluidics, acoustics and electromechanical transduction.

A schematic of the devices is shown in figure 1: the output of each source in the QCL array is combined into a miniaturized photo-acoustic cell by a photonic multiplexer.
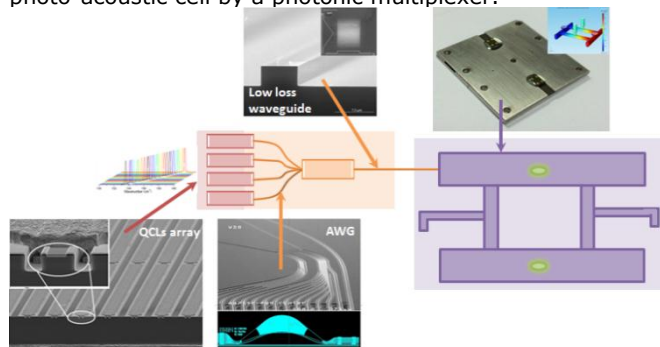

Figure.1: Schematic of the fully integrated sensor including an array of QCL sources, a multiplex to combine and drive the laser outputs and the MEMS photo-acoustic cell.

The widely tunable Mid-IR QCLs, Fig.1, have recently been developed [2] through a proprietary metal grating approach

where the feedback in the cavity comes from the interplay between guided waves in the active medium and surface waves at the interface with the metal grating. The wavelength of each laser can be selected independently after the growth of the epitaxial layers. Moreover, a strong coupling can be obtained without the use of buried grating and the second mode is suppressed because of the higher losses while principal mode is favored.

Photonic multiplexers (at 4.5μm and 7.4μm) (see Fig. 1.) based on specific SiGe technology (having step index profile and graded index profile in the in-plane and out-plane direction, respectively) were fabricated and characterized. Losses of such waveguides were <1dB/cm at 4.5 μm, <1.5 dB/cm at 5.65 μm and <2dB/cm 7.4 μm, which represent to our knowledge, state-of-the-art performances for this wavelengths range [3].
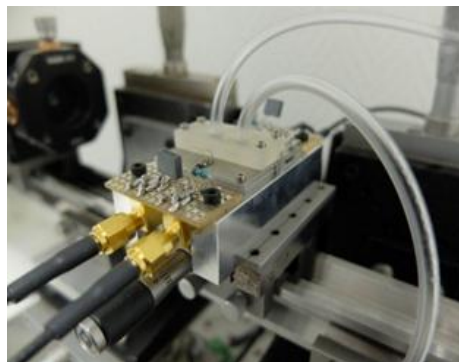

Figure.2: Set-up for gas measurement with photo-acoustic cell

The small differential Helmholtz resonator (DHR) [4] has been investigated. In DHR two identical chambers are connected by two capillaries. Although only one chamber of the sensor is illuminated by a laser beam, acoustic waves are established in both chambers allowing an intrinsic differential measurement. This scheme is also relatively insensitive to the shape of the energy deposition localization [4] and keeps constant pressure in each chamber.

The feasibility of such a system based on the assembly of QCLs, a multiplexer and a photo-acoustic cavity has recently been demonstrated. A Limit Of Detection of 1ppm has been reached injecting diluted CH4 gas in a carrier gas, Fig. 2.

Related Publications:
1 S. Nicoletti et. al., IEEE Sensors 2014. Proceed-ings (2014), p. 649.
2 G. Maison et al., 2014International Semiconduc-tor Laser Conference (ISLC) Proceedings (2014), p. 169
3 M. Brun, et. Al., OPTICS EXPRESS Vol. 22, No. 1 (2014), p. 508
4 A. Glière, et al., Int. J. Thermophys (2013), 34, p. 2119 & A. Glière, et al., SENSORS (2014), Vol. 14 p. 957

Towards non linear conversion from mid to near infrared wavelengths using silicon germanium waveguides

Research topics : gaz sensors, mid infrared, non linear optics

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ABSTRACT: We report on nonlinear conversion from mid infrared to near infrared optical wavelengths in silicon germanium waveguides using phase-matched four wave mixing. These waveguides, originally developed for gas sensing by infrared spectroscopic optical absorption, offer interesting non-linear characteristics and could lead to new detection schemes for gas sensing.

The mid-infrared (mid-IR) spectral region has attracted a significant amount of interest during the past few years. It contains the absorption "finger-prints" of most molecules of interest, thus suggesting several applications both in spectroscopy and chemical and biomolecular sensing. The recent development of mid-IR sources, most notably quantum cascade lasers (QCLs)[Y. Yao, (2012)], has further stimulated the interest of the research community in this area. However, the lack of small size, room temperature detectors exhibiting suitably high sensitivity at this wavelength region still remains an issue.

To overcome this issue, wavelength conversion of the mid-infrared signals to the near-infrared is a promising alternative. This conversion can be performed either through sum-frequency generation in a second-order nonlinear medium, such as periodically poled lithium Niobate [K. D. Buchter (2009)], or through four-wave mixing (FWM) using a third-order nonlinear medium, such as silicon [B. Kuyken (2011)]. Silicon is an excellent candidate for such applications, thanks to its transparency up to 7µm, reduced two-photon and free-carrier absorptions beyond 2µm and its potential for monolithic integrated solutions. These features however, are not restricted to pure silicon. For instance, silicon germanium (SiGe) alloys have been identified as promising candidates for nonlinear applications in the mid infrared and long infrared thanks to their enhanced nonlinearity compared to pure Si [N. K. Hon (2011)].

In this context, and using our SiGe grade index waveguide platform [1], we adapted the waveguide geometry in order to obtain good nonlinear characteristics, namely: a) Strong confinement with small effective mode area for intense nonlinearities, b) low loss throughout the wavelength span c) sufficient coupling with the dominant mid-IR sources, e.g. QCLs, and d) zero dispersion around 2 µm.

The waveguide design as well as simulated dispersion curves is shown in Fig.1. The main factor affecting the waveguide dispersion is the ratio H/L. For a given H value, an increase in L results in a blue shift of the zero dispersion wavelength. However by further increasing the waveguide width, the effective mode area becomes too large to support strong non-linear phenomena.

Fig. 2 summarizes the measurements and compares them with numerical simulations which considered an input launched power of 75 mW for the pump, 10 mW for the signal, and waveguide losses of 2 dB/cm, in line with the experimental values. The comparison is in qualitative agreement.
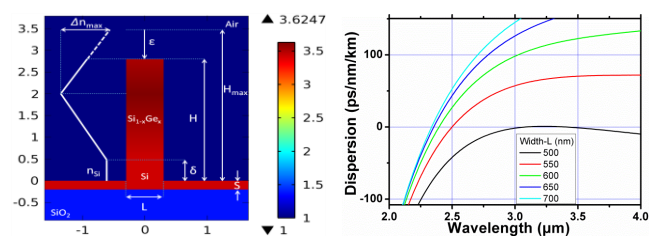

Figure 1: LEFT: schematic view of the waveguide structure. RIGHT: theoretical dispersion curve for 5 different widths (H=2.05µm, δ=1µm).
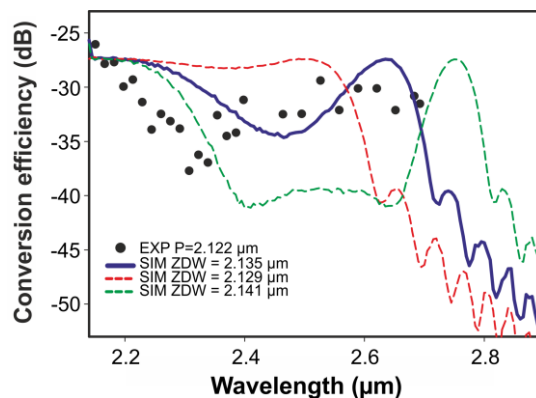

Figure 2: Conversion efficiency as a function of the signal wavelength. Comparison between experiments (black dots) and numerical simulation for the dispersion shown in Fig. 1 (blue solid line) and for the zero dispersion shifted of + 6 nm (green dashed line) and - 6 nm (red dashed line).

The figure 2, also demonstrates a Conversion Efficiency of −32 dB for the conversion from 2650 nm to 1771 nm, which represents one of the highest values ever reported. Note that it was not possible to demonstrate broader conversion than this due to limitations in the tunability of the lasers used.

Related Publications:
[1] M. Brun & al, "Low Loss SiGe graded index waveguides for mid-IR applications", Op. Ex. 22 (1) pp508-518 (2014)

Optimization of a radiative membrane for gas sensing applications based on NDIR method

Research topics: gas sensing, MEMS, membrane, spectral efficiency

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ABSTRACT: In order to design cheap and efficient sources of radiation for gas sensing applications, we propose a model to optimize the device wall-plug efficiency relative to application driven constraints. Typically, suspended micro-hotplates realized using MEMs technology are used, but their efficiency is rather low. Considering constraints such as the available energy-per-measurement and the maximum operating temperature, we demonstrate that the size and the switch-on time of the membrane can be optimized in order to emit the largest possible amount of light in the gas spectral window of absorption. We also show that the efficiency can be drastically improved by tuning the hotplate emissivity to match this absorption profile, and provide an insight into the thermo-optical mechanisms governing these devices.

To engineer a cheap, portable and low-power optical gas sensors, incandescent sources are strongly competing expensive quantum cascade lasers and low-efficiency light-emitting diodes. Such sources of radiation have already been realized by us, using standard MEMS technology, consisting in free standing circular micro-hotplates. Once sealed under vacuum, the main drawback of these membranes is known to be the power lost through conduction to the substrate, thus not converted in (useful) radiated power. If the membrane temperature is capped by technological requirements, radiative flux can be favored by increasing the membrane radius. However, given a finite amount of energy (ensuring the low-power characteristic of the device), the larger the membrane and its heat capacity, the shorter the time it can be turned on. This clearly suggests that an efficiency optimum has to be found. We use a 1D thermo-optical model, based on hypotheses allowing us to retain the essential characteristics of the membrane depicted on figure 1, while drastically reducing the computation time compared to standard FDTD.
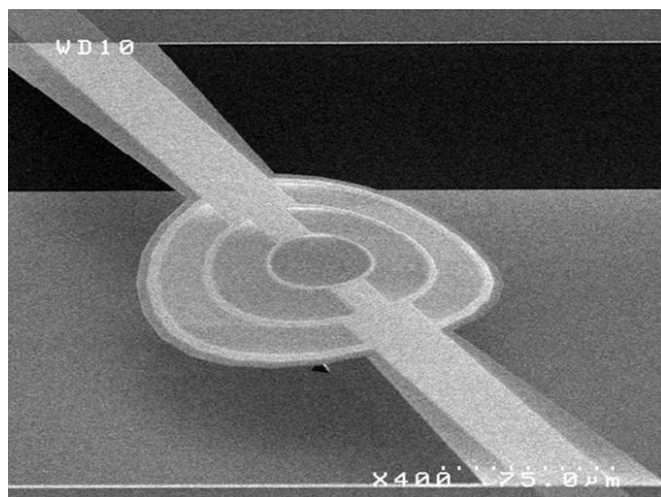

Figure 1: SEM image of the modeled suspended membrane. Light grey areas are the electric tracks providing Joule heating.

These simulations are based on a spatio-temporal radial profile, which allow us to compute precisely the amount of

light emitted in the absorption window of the gas of interest, namely CO_2 in this example. Only certain couples (membrane radius / heating time) are allowed in order to meet both the energy and the maximum temperature requirements, and an optimum is found as intuited, as depicted on figure 2.

In the case of a blackbody emission with unitary emission, efficiency is capped to a few percent, for even if conduction has been strongly reduced, most of the radiation is emitted outside the CO_2 absorption window. In order to tackle this problem, we study the possibility of tuning the membrane emissivity, using optical coatings for example, in order to match closely the absorption window. In the optimum case where light is only emitted in this spectral range, the efficiency jumps by an order of magnitude, and is only limited by the conduction through the arms, see figure 2.
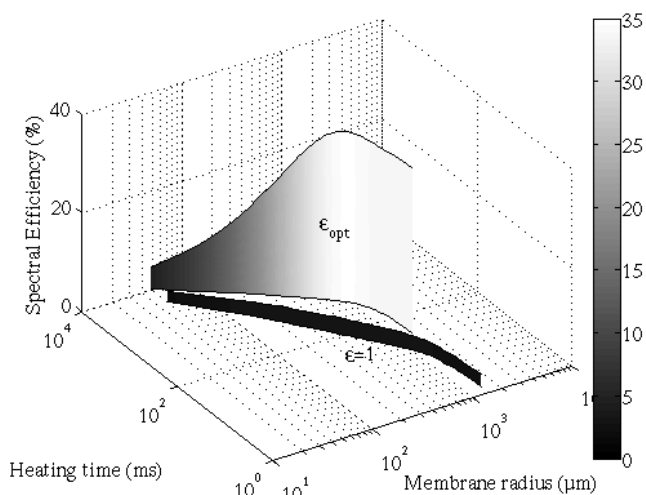

Figure 2: R(t) solution and corresponding spectral efficiency of the constrained thermal equations with E=5mJ and Tf=923K for the optimal emissivity and the unitary emissivity.

This optimization process can be made with different membranes, constraints, gases, and will always yield the best possible design in order to fabricate low-power, high efficiency thermal sources for gas sensing applications
.

Related Publications:
Lefebvre, A., Boutami, S., Greffet, J. J., & Benisty, H. (2014, May). Optimization of a radiative membrane for gas sensing applications. In SPIE Photonics Europe (pp. 91410G-91410G). International Society for Optics and Photonics.

4

Silicon Photonics

CMOS photonic III-V/Si devices

Modulators and receivers

Hybrid optical lasers

Photonic systems

Low-crosstalk fabrication-insensitive echelle grating demultiplexers on Silicon-On-Insulator (SOI)

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ABSTRACT: In this communication, we report about the design, fabrication, and testing of echelle grating (de-)multiplexers for the 100GBASE-LR4 norm in the O-band (1.310 nm) for Silicon-based photonic integrated circuits (Si-PICs). In detail, 20th-order echelle gratings on the 300-nm-thick SOI platform are designed for 4x800-GHz-spaced wavelength division multiplexing. The devices are featuring extremely low crosstalk (~ -30 dB), precise channel spacing, and optimized insertion losses (-3 dB). State-of-the-art absolute lambda registration over the wafer and the lot claim the excellent robustness of these demonstrators.

Silicon-on-insulator (SOI) high-index contrast allows for the small-footprint implementation of optical functions constituting the whole silicon photonics toolbox such as optical resonators, laser sources, input/output (I/O) couplers, high-speed modulators, Si-Ge photodiodes, as well as filters and wavelength (de)multiplexers.

Concerning the latter, wavelength-division multiplexing (WDM) constitutes an essential building block for the development of high-capacity inter-rack, inter-board optical interconnects and on-chip transceivers. Optical filters working as wavelength (de-)multiplexers (WMUX) are needed for reaching higher aggregate system bandwidths, by transmitting/receiving data over several optical carriers. Specifically, a low crosstalk at the receiver is crucial for ensuring a correct data transfer at high rates, while a precise interchannel spacing and a minimized non-uniformity are necessary to minimize insertion losses. Moreover, wafer- and lot-level performance stability is essential for power-efficient transceivers, as the active realignment of the spectral comb transmission peak respect to absolute ITU grid wavelengths represents an extra thermal and power budget.
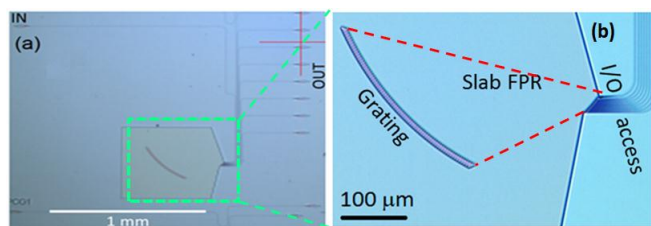

Figure 1: Optical images (a, b) of the echelle grating (de-)multiplexers.

In diffractive-based echelle gratings (EGs), phase delay is obtained by using a free propagation region (FPR) comprising a slab waveguide, while the chromatic dispersion is attained via the wavelength-dependent reflection from a high-order (usually m>10) diffraction grating.

Echelle gratings are diffraction grating spectrometers whose principle is based upon phase matching the light reflected from neighboring facets. In addition to the diffractive properties, the shape and the curvature of an echelle grating provides, at a given wavelength, the focusing of the input waveguide mode onto the plane of the output waveguides.

Optical and scanning electron microscope (SEM) images of the echelle grating (de-)multiplexer are illustrated, respectively, in Figs. 1. The fabrication process made use of 200-mm CMOS pilot lines processing tools on SOI substrates, characterized by 310 nm of silicon over 800-nm buried oxide (BOX). Dose-optimized VISTEC variable-shape electron-beam (e-beam) lithography and HBr-based reactive-ion etching are used for the silicon patterning. High-density plasma (HDP) silica deposition is used for Si encapsulation, then followed by chemical-mechanical polishing (CMP) for surface planarization.
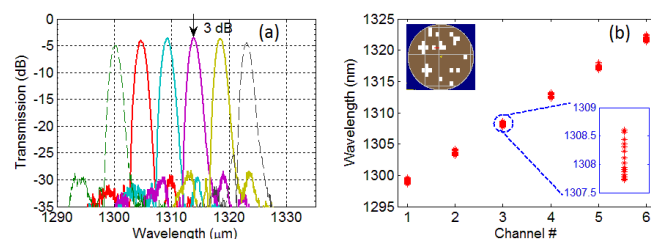

Figure 2: (a) 20th-order 800-GHz-spaced echelle grating transmission spectrum around 1310 nm. (b) Wafer-level channel-by-channel wavelength dispersion. Randomly-chosen dies (25) over the SOI wafer (upper left inset).

A 20th-order echelle grating transmission spectrum for 4×800-GHz (de-)multiplexing is reported in Fig. 2(a). The test results confirm a very good interchannel isolation (average > 27 dB), a precise channel spacing (800 GHz), a 0.8 dB channel-to-channel uniformity and overall insertion losses in the 3 to 3.8 dB range. Design and fabrication robustness is also very important, especially for interconnects networking. Wafer-level performance statistics have been derived by comparing the echelle spectral response of 25 randomly chosen dies over the wafer. These 25 devices present crosstalk values averaging at -30 dB, with channel spacing and absolute wavelength registration remaining very stable over the wafer as shown in Fig. 2(b). This implies a notable advantage for PICs development as energy consumption needed for active thermal re-alignment among devices would remain limited. In addition, the excellent interchannel isolation achieved over the whole wafer would significantly reduce symbol errors at the receiver, ensuring minor latency power-efficient data transmission at both circuit and system levels.

Related Publications :
[1] C. Sciancalepore, et al., "Low-crosstalk fabrication-insensitive echelle grating demultiplexers," IEEE Photon. Technol. Lett., (in press), Oct. 15, 2014.
[2] C. Sciancalepore, et al, "Low-crosstalk fabrication-insensitive echelle grating multiplexers and passives for the silicon photonics toolbox," Photonics West 2015, San Francisco (CA), USA, February 7-12, 2015.
[3] F. Horst, W. M.J. Green, S. Assefa, St. M. Shank, Y. A. Vlasov, and B. J. Offrein, "Cascaded Mach-Zehnder wavelength filters in silicon photonics for low loss and flat pass-band WDM (de-)multiplexing," Opt. Exp., vol. 21, pp. 11652-11658, 2013.

Germanium avalanche receiver for low power interconnects

Research topics : Germanium photodiode, silicon photonics

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ABSTRACT: We report a 10Gbit/s waveguide avalanche Germanium photodiode (APD) under low reverse bias. The proposed APD scheme only requires simple technological steps fully compatible with CMOS processes without any nanometer accuracy and/or complex epitaxial growth schemes needs. An intrinsic gain higher than 20 was demonstrated under a bias voltage as low as -7V. The Q-factor relating to the signal-to-noise ratio at 10Gbit/s was maintained over 20dB without the use of a trans-impedance amplifier (TIA) for an input optical power lower than -26dBm thanks to an aggressive shrinkage of the Ge multiplication region. A maximum gain over 140 was also obtained for optical powers below -35dBm.

The main challenges of silicon photonics are today power consumption and cost reductions as well as the increase in bit rate of optical integrated circuits. Whereas cost reduction will be addressed by large scale production in 200 mm and/or 300 mm fabrication lines, the consumed energy/bit and the transmission bit rate figures will only be solved by improving the devices themselves. On the receiver part, several levers exist to reduce the power consumption. The use of avalanche photodiodes (APD) could push the responsivity beyond the limit imposed by external quantum efficiency by multiplying the photo-generated carriers, leading to a reduction of the overall optical power into the photonic circuit. The reduction of the capacitance of the photo-detectors also helps in reducing power consumption.

For that we thus use a compact p-i-n Ge photodiode biased in avalanche mode with a thin multiplication Ge layer for dead space enhanced noise reduction, for receiver-less operation at 10Gbit/s. Figure 1 shows a schematic view and a scanning electron microscopy image of a p-i-n diode-based Ge APD integrated in a Si waveguide. Both absorption and multiplication take place in the Ge layer. The multiplication process is initiated by electrons and holes, and both are multiplied within the intrinsic region. The Ge layer is 300nm thick and 10µm wide and long. The intrinsic region, designed to have a width of 500nm, was defined by the ion implantation of n-type and p-type regions. The narrow intrinsic Ge region ensures the presence of a high electric field inside the intrinsic region over the full depth. The 10µm long Ge layer was selectively grown by Reduced Pressure – Chemical Vapour Deposition in an etched Si recess at the end of the waveguide yielding high absorption efficiency with a small device capacitance. The back-end-of the-line (BEOL) processing consisted in standard Complementary Metal Oxide Semiconductor (CMOS) metallization with tungsten (W) plug-type contacts on Ge followed by Aluminium Copper (AlCu) electrodes. Figure 2 shows the -3dB optical bandwidth at λ=1550 nm of a p-i-n photodiode as a function of the gain for a -19dBm optical power. When the photodiode is operated with unity gain, the maximum bandwidth is over 40GHz. As the gain increases, the bandwidth decreases as the carrier multiplication time then increases. Both holes and electrons contribute to impact ionization in germanium as their ionization coefficients are rather similar. Hence, the bandwidth drops, as it is dominated by the multiplication time.
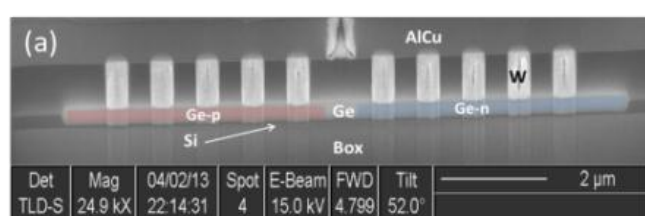

Figure 6: SEM view of the lateral p-i-n Ge on Si photodiode integrated at the end of a Si waveguide.

At a gain of 17, the measured photodiode bandwidth still remains about 11GHz, allowing a 10Gbit/s operation. The Gain-Bandwidth product is then higher than 190GHz.
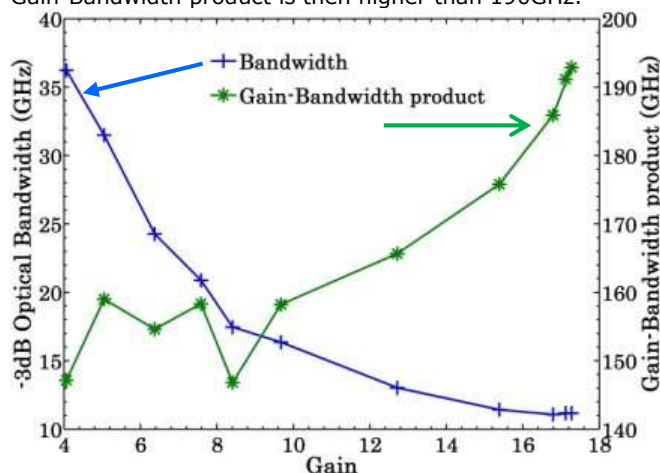

Figure 2: -3dB optical bandwidth versus gain.

The future integration of such photodiodes with low noise TIA and equalizer should lead to very high sensitivity receivers for optical communication applications requiring low power consumption. Moreover, we were able to achieve a gain over 140, which is among the highest reported so far for Ge APDs, albeit with much more complex integration schemes. This demonstration may enable the development of new applications including secure quantum key distribution which requires photon counting receivers, as well as on chip optical clocking.

Related Publications:
[1] Virot, L & al "Germanium avalanche receiver for low power interconnects" Nature Communications 5, number: 4957 (18 Sept 2014)
[2] Vivien, L. & al. Zero-bias 40Gbit/s germanium waveguide photodetector on silicon. Opt. Express 20, 1096–101 (2012)
[3] Hartmann, J-M. & al. Reduced pressure-chemical vapor deposition of intrinsic and doped Ge layers on Si (001) for microelectronics and optoelectronics purposes. J. Crystal. Growth 274, 90–99 (2005)

Structural and optical properties of 200 mm optical Germanium substrates for Silicon Photonics Applications

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(* LETI/ DTSI & DCOS, ** CEA/ INAC)

ABSTRACT: Integrated laser sources compatible with microelectronic technologies is currently one of the main challenges for silicon photonics. Germanium (Ge) has an indirect band gap leading to an inefficient photo-generation process which, however, is drastically improved when high mechanically strain is induced. Our objective was to obtain highest Ge crystalline quality layers to be able to apply strains. A complete study on the impact of PH3 flows on the structural and electronic properties of Ge:P layers was performed on the Ge layers grown by Reduced Pressure Chemical Vapour Deposition.

Germanium has been highly investigated as a potential light emitting material for the integration of photonic devices on silicon-based electronics, in the search of merging electronics and photonics using Group IV materials [1]. By doping n-type Ge, the electrons given by the n-type impurities occupy the indirect valleys of the conduction band, exalting fast, direct transitions between the Γ point of the conduction band and the heavy and light holes sub-bands of the valence band [J. Liu, X. Sun and Al, Opt. Express, 15, (2007)]. Low deposition temperatures and high growth pressures can yield the high P contents aimed for Ge light emission. Germanium was grown at 400°C, 100 Torr on 200 mm on slightly p-type Si(001) substrates with various PH3 flows. X-Ray Diffraction showed that all Ge:P layers were slightly tensile-strained and diffracted coherently irrespectively of the process conditions used. The tensile strain was slightly higher after a cyclic temperature annealling.
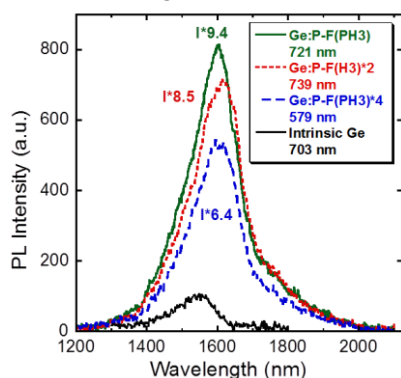

Figure 1: Room temperature micro photo-luminescence spectra associated to thick Ge:P layers grown at 400°C, 100 Torr for various PH3 flows. Incident laser wavelength (output power): 488 nm (8 mW); CdHgTe Avalanche Photo-Detector.

Such a strain state is due to thermal dilatation coefficient differences between Ge and Si. They come into play during the cooling-down to room temperature of the fully relaxed Ge(:P) layers (at the annealing temperature) on the much thicker Si substrates underneath [1]. The room temperature micro-Photoluminescence measurements showed a factor close to 10 increase of the PL peak Intensity in Ge:P layers, as shown in Figure 1. The integrated PL intensity dropped dramatically irrespectively of the process conditions when the F(PH3)/F(H2) become too high.

Due to the mismatch of Si and Ge lattice constants, dislocations at the interface of Silicon and grown Ge (Figure 2a) weaken the whole layer when tensile strain is applied. The highest Ge crystalline quality is required to avoid mechanical breaking of the Ge when a strong tensile strain is applied. To combine the advantages of high quality Ge layers on a silicon host substrate with a SiO2 layer that isolate optical modes, the Ge layer has been transferred to obtain a Germanium-On-Insulator (GeOI) substrates.
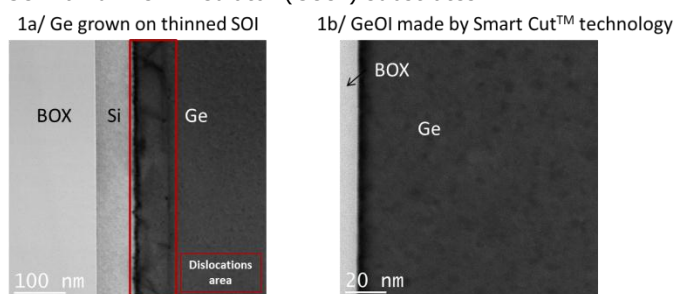

Figure 2 : a/ TEM images of a/ Ge grown on SOI and b/GeOI

We obtained for the first time 200 mm "optical" GeOI substrates for Silicon Photonics made from epitaxial wafers using the Smart CutTM technology composed by a thick germanium layer (>500 nm and up to 1 µm) on 1µm buried oxide (BOX). Compared with conventional GeOI fabricated for microelectronic applications, a deeper splitting step had to be optimized, requiring H+ implantation at higher energy and higher dose than for standard applications. A homogenous transfer of thick Germanium layer was reached on 200 nm wafer with a drastically reduced number of dislocations at the interface SiO2 – Ge (Figure 2b). GeOI photoluminescence was compared to the one from Ge grown on Si or SOI. The PL intensity is higher for intrinsic GeOI sample. The photo-generated careers seem to not recombine on the Si layer or in the dislocations. This observation seems to confirm the high Ge quality of the GeOI sample. Lifetime career measurements will be performed on samples to confirm this hypothesis.

The feasibility of the process was demonstrated to provide optical GeOI and could open the way to wafer based fabrication process of new devices based on strained [2] and doped germanium for Silicon photonics and Sensing applications.

Related Publications:
[1] K. Guilloy, N. Pauc, E. Robin, V. Calvo, P. Gentile, K. Foubert, J. Rothman, V. Reboud, A. Chelnokov, V. Benevent, J. M. Hartmann, Band structure engineering of strained and doped germanium nanowires and 2D layers, IEEE 11th International Conference on Group IV Photonics (GFP), DOI : 10.1109/Group4.2014.6961940 (2014).
[2] M. J. Süess, R. Geiger, R. A. Minamisawa, G. Schiefler, J. Frigerio, D. Chrastina, G. Isella, R. Spolenak, J . Faist, H. Sigg, Nature Photonics, Volume 7, Issue 6, pp. 466-472 (2013).

Optics and Photonics

1310 nm Hybrid InP/InGaAsP on Silicon Distributed Feedback Laser with High Side-Mode Suppression Ratio

H Duprez, A Descos, T Ferrotti, C Sciancalepore, C Jany, K Hassan,
C Seassal*, S Menezo, and B Ben Bakir (*Institut Nanotechnologies Lyon, France)

ABSTRACT: We report on the design, fabrication and performance of a hetero-integrated III-V on silicon distributed feedback lasers (DFB) at 1310 nm based on direct bonding and adiabatic coupling. The continuous wave (CW) regime is achieved up to 55 °C as well as mode-hop-free operation with side-mode suppression ratio (SMSR) above 55 dB. At room temperature, the current threshold is 36 mA and the maximum coupled power in the silicon waveguide is 22 mW.

The need for high data transmission rates keeps increasing and this trend is unlikely to slow down in the foreseeable future. In this context, doubts are casted on the capability for current copper-based interconnects and electronics circuits to follow this tendency. Shrinking microelectronics nodes gets harder both because of the density limit and the heating managements within the circuits, which become increasingly expensive to cool. Power-efficient optical interconnects appear as a way to withstand the relentlessly growing bit stream.

Although silicon is a poor light emitter due to its indirect bandgap, making lasers out of silicon has been investigated during the last ten years showing promising results. The demonstration of a continuous wave silicon laser based on Raman scattering incites to keep looking in this direction as well as the use of strained heavily doped Ge as a gain-enabler material. However, both solutions need further development to be power-efficient.

One approach in III-V/Si laser architecture lies in designing the hybrid active region so that the optical mode stays mainly confined within the underlying silicon waveguide, interacting with the III-V quantum wells (QWs) only with its evanescent tail which limits the modal gain. Though such a configuration is subject to less complexity regarding coupling, the amplification is restricted and the bonding layer thickness is critical. In our approach, we opted for a design that uses the III-V gain region as efficiently as possible by having the optical mode confined in the QWs [1, 2]. To allow for the mode to transit from the III-V to the silicon waveguide, adiabatic mode transformers were designed using the deterministic adiabaticity criterion demonstrated in [X. Sun et al, Opt. Lett. 34 (2009).].

We report herein hybrid III-V on silicon DFB lasers operating at 1310 nm based on direct bonding and adiabatic coupling between both materials.
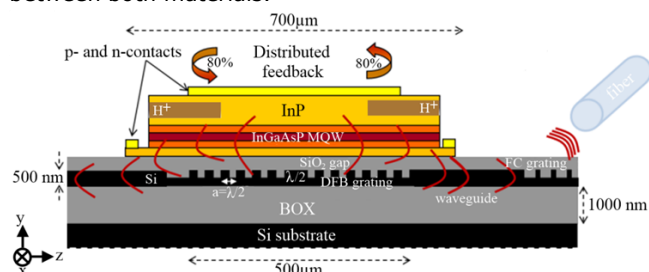

Figure 1: Longitudinal schematic view of the laser. The III-V and the silicon waveguide are separated by a SiO2 gap of 75nm.

Schematic longitudinal view of the device is presented in Fig. 1. The III-V and the silicon waveguide are separated by a SiO2 gap of 75nm.

The quarter-wave shifted (QWSh) DFB grating is etched along the 500-nm-thick silicon waveguide underneath the III-V active layers. The active region is 700-µm-long and consists of InGaAsP multiple QWs (MQWs) exhibiting maximum gain centered on 1310 nm, surrounded by p- and n-doped InP layers. The silicon rib is 200-nm-thick and needs to be narrow enough to confine the light mostly in the III-V QWs. At both terminations of the grating, the silicon waveguide is widened adiabatically, enabling light to be coupled into the silicon with more than 90% efficiency, allowing as much optical power to be produced at both outputs of the laser. Those 100-µm-long mode transformers are a key point in the design of the device. Laser light emission is collected with a fiber positioned on the top of a waveguide-to-fiber surface grating coupler.
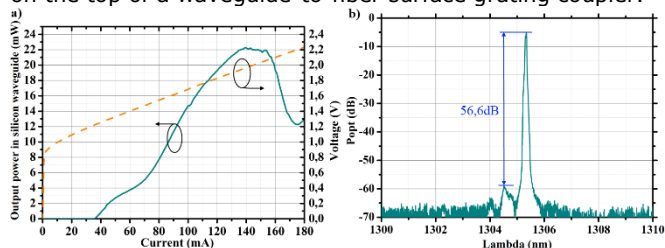

Figure 2: Room-temperature LIV (a) and spectrum of the laser at I=107mA (b). The resolution of the optical spectrum analyser (OSA) is 0.02 nm.

Laser operation with a classic DFB signature was demonstrated on the whole wafer. The device was mounted on a Peltier module to set its temperature from 20°C up to 80°C. The output power was measured collecting the light from the surface grating coupler with a multimode fiber (MMF). L-I curves in CW regimes for different temperatures show lasing effect up to 55 °C.

As presented in Fig. 2(a), the room temperature (RT) threshold current is 36 mA which corresponds to a 1.03kA/cm2 current density for a 700-µm-long and 5-µm-wide active region. The maximum output power is then 2.8 mW in the waveguide. The fiber coupling losses were measured to be 6 dB. We can therefore conservatively assess an output power of 11 mW coupled into the silicon waveguide and 22 mW if we consider both outputs. The L-I slope being 0.24W/A, the resulting differential quantum efficiency of the laser is 25%. Moreover, the laser diodes are characterized by a turn-on voltage of 1.23 V and a series resistance of 10.5 Ω. Current and future work are focused on the improvement of maximum operation temperature as well as the co-integration of the laser either with a III-V on silicon electro-absorption modulator or with a SOI Mach-Zender modulator. Development of the whole process on the 200-mm-platform is ongoing.

Related Publications :
[1] B. Ben Bakir et al., "Electrically driven hybrid Si/III-V Fabry-Pérot lasers based on adiabatic mode transformers," Opt. Express. 19, 10317-10325 (2011).
[2] B. Ben Bakir et al., "Heterogeneously integrated III-V on Silicon Lasers," in ECS 64, 211-223 (2014).

Hybrid III-V/Silicon tunable laser modules

Research topics : Silicon photonics, WDM data transmissions, Molecular bonding

S. Olivier, S. Malhouitre, C. Kopp, N. Girard*, G. Levaufre*, G.-H. Duan*, F. Mallecot* (*III-V Lab)

ABSTRACT:
Silicon photonics is a key technology to develop low-cost and compact circuits that integrate photonics and microelectronic elements on a single chip. We used the molecular wafer bonding technique to develop a hybrid widely tunable, singlemode III-V/Si laser for wavelength division multiplexing, with a tunability over 35 nm and an output power in excess of 3 mW. This approach exploits the highly efficient light emission properties of direct-bandgap III-V semiconductor materials and the low-loss and highly integrated passive circuitry in silicon.

The field of silicon photonics is attracting a lot of attention due to the prospect of low-cost and compact circuits that integrate photonics and microelectronic elements on a single chip. Such silicon chips have applications in optical transmitter and receiver circuits for short-distance communications as well as for long-haul optical transmissions. Silicon photonics has proven to be a successful platform for many functional elements such as low-loss waveguides, filters, multiplexers/demultiplexers, optical modulators and Ge-on-Si photodiodes. However the integration of a light source remains a key challenge in silicon photonics. Today, the most promising approach is the heterogeneous integration of III-V light sources on silicon via wafer bonding techniques. This approach exploits the highly efficient light emission properties of direct-bandgap III-V semiconductor materials and the low-loss and highly integrated passive circuitry in silicon.
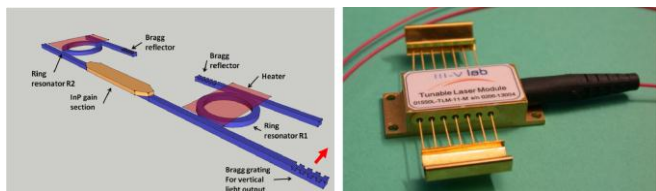
The structure of our hybrid widely tunable laser for wavelength division multiplexing is illustrated in Fig. 1. It consists of an InP-based amplification section, tapers for modal transfer between III-V and Si waveguides, two ring resonators for single mode selection, metal heaters on top of the rings for the thermal wavelength tuning, and Bragg gratings that provide reflection and output fiber coupling. The two ring resonators have slightly different free spectral ranges, such that the Vernier effect is used to achieve wide-range wavelength tuning. The laser was packaged in an optical module. A wavelength tuning range of 35 nm was achieved with a side mode suppression ration (SMSR) higher than 50 dB and an optical output power level in excess of 3 mW across the whole wavelength range (see Fig. 2). The measured laser linewidth falls in the range of 500 kHz to 5 MHz over the entire wavelength range. Such a laser can be used as a local oscillator in a coherent receiver for polarization-division multiplexing quadrature phase-shift keying of a signal at 100 Gb/s.

Figure 1 : Schematic view (left) and photograph (right) of the widely tunable single mode hybrid III-V/Si laser

The fabrication process includes the following steps. First, SOI wafers are patterned on a 200 mm CMOS line to form Si passive rib waveguides, which are optimized for coupling with III-V waveguides that will be later aligned on them, thanks to the definition of adiabatic coupling sections [3-4]. Additional etching steps are completed to form the passive circuitry. The patterned SOI substrate is then encapsulated with silica and planarized by chemical-mechanical polishing. Then, an unstructured InP wafer containing multiple quantum wells is bonded onto the SOI substrate, epitaxial layers facing down, and the III-V growth substrate is removed. Advantageously, no precise alignment is required for the molecular bonding step. The III-V waveguides are fabricated after bonding and are encapsulated before the metallization of the contacts. Finally, the fabricated lasers are ready for wafer-level testing, with vertical gratings in silicon designed for in- and out-coupling to optical fibers.
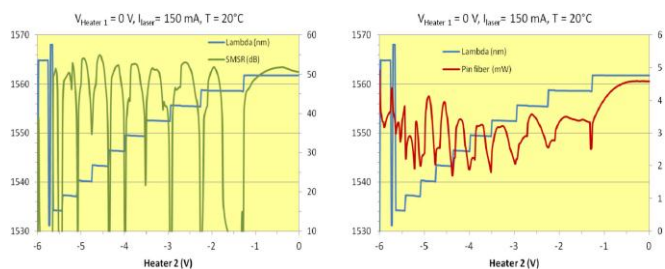

Figure 2 : Plots of wavelength tuning with its corresponding SMSR (left), and wavelength tuning and output power level coupled to a single mode fiber (right), all as a function of the voltage applied to the heater.

The performances of our hybrid III-V/Si laser approach that of a monolithically integrated InP-based laser. Functionalities such as spectral filtering and wavelength tuning were integrated thanks to the silicon platform. Moreover, the integration of hybrid lasers on silicon further allows for the fabrication of more complete photonic circuits such as transmitters and receivers for applications ranging from short-distance data communications to long-haul optical transmissions.

Related Publications :
[1] G.-H. Duan, C. Jany, A. Le Liepvre, A. Accard, P. Kaspar, A. Shen, P. Charbonnier, F. Mallecot, F. Lelarge, J.-L. Gentner, S. Olivier, S. Malhouitre and C. Kopp, "Hybrid wavelength tunable III-V and lasers on Silicon", SPIE Newsroom, 10.1117/2.1201403.005370 (2014)
[2] S. Olivier, S. Malhouitre, C. Kopp, G.-H. Duan, P. Kaspar, C. Jany, A. Le Liepvre, A. Accard, D. Make, N. Girard, G. Levaufre, A; Shen, P. Charbonnier, F. Mallecot, F. Lelarge and J.-L. Gentner, "Hybrid III-V Lasers on Silicon", Invited paper at the IEEE International Phtonics Conference (2014)

A CMOS-compatible Franz-Keldysh effect plasmonic modulator

40 Gb/s silicon modulators fabricated on 300 mm SOI wafers

S. Olivier, N. Abadia, L. Vivien* (*IEF, Orsay, France)

ABSTRACT:
Silicon photonics is a key technology to develop low-cost and high-performance optical interconnects. A major challenge is the development of low-power consumption optical modulators to reduce the power budget of optical links. We present a design of a CMOS-compatible germanium-on-silicon Franz-Keldysh effect plasmonic modulator. The modulator length is below 30 μm, it operates at -3V and features a power consumption as low as 20 fJ/bit.

Research topics : Silicon photonics, optical modulator, plasmonics, Franz-Keldysh effect

There is a growing interest for silicon photonics to develop low-cost and high-performance optical interconnects. Most of the electrical consumption of an optical interconnect is to be attributed to the optical modulator. It is therefore key to develop low-consumption optical modulators.

For this purpose, we have investigated a CMOS-compatible Franz-Keldysh effect (FKE) modulator assisted by plasmons. FKE is the change in the optical absorption of a material under the application of an electric field. This change occurs near the band-edge of the direct band-gap of the material. Several photonic modulators based on the FKE have already been demonstrated but it is expected that using a more confined plasmonic mode, the interaction with the electro-optical material will be enhanced, leading to more compact devices, and in consequence to less power consumption.
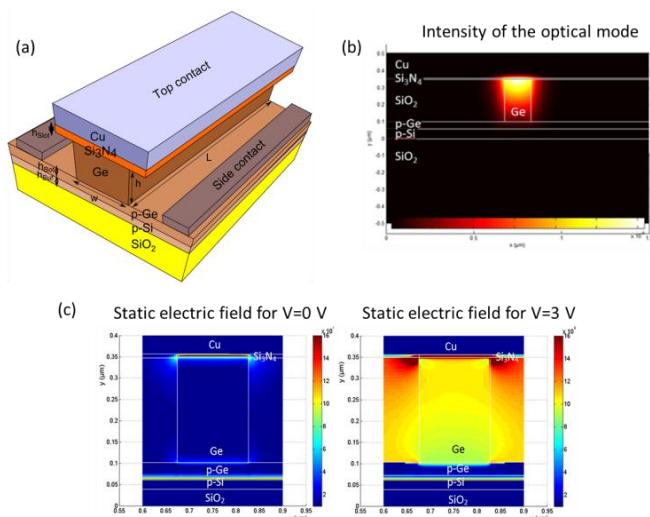

Figure 1 : Fig. 1, (a) Structure of the plasmonic modulator, (b) Intensity distribution of the plasmonic mode and (c) static electric field distribution in the structure for V=0 V (left) and V=3 V (right)

The structure of the proposed device is presented in Fig. 1 (a). It consists of a metal-insulator-semiconductor (MIS) plasmonic waveguide formed by a stack of Cu/Si3N4/Ge. The core of the modulator is made of Ge of width w and height h. This structure is deposited over a slab of p-doped Ge and p-doped Si layers, on which the side contact is deposited. The other contact is directly the top metal of the MIS waveguide.

The proposed structure allows simultaneously to concentrate the optical field in the Ge region and to apply a static electrical field using a driving voltage V. The plasmonic MIS waveguide supports a plasmonic mode whose field is present in the Ge core (Fig. 1 (b)). The electrical fields obtained at 0V and 3V are shown in Fig. 1 (c). At 0V, there is no static electric field in the Ge core whereas at 3 V, a significant static electric field appears in the Ge core, overlapping the plasmonic mode. This electrical field changes the absorption of Ge, hence producing direct intensity modulation of the plasmonic mode.

Electro-optical simulations were performed to estimate the performances of the device such as propagation losses, extinction ratio, bandwidth and power consumption. The static electric field was calculated using the commercial electrical simulator ISE-Dessis. Once the distribution of the static electric field in the structure was obtained, the distribution of the change in the absorption coefficient of Ge due to the FKE was calculated using an analytical model. Then a finite difference method (FDM) mode solver was used to calculate the effective index and the effective losses of the mode allowing to estimate the extinction ratio (ER) and the propagation losses (PL) of the device.

Optimized modulator performances were obtained for w=150 nm, h=250 nm, hslot=5 nm, hbuf=60 nm and hbot=40 nm. The main characteristics of the optimized device at 1650 nm are an extinction ratio of 3.3 dB, propagation losses of 11.2 dB, a power consumption of 20 fJ/bit and a cutoff frequency of 350 GHz for a device length of L=30 μm. The power consumption is one of the lowest reported in the literature for both Ge-based photonic modulators and plasmonic modulators. The working wavelength could be modified by using controlled epitaxy of GeSi to achieve modulation around 1.55μm.

Input and output coupling of the modulator to standard silicon waveguides were also investigated in order to minimize the total insertion losses of the device. A butt-coupling scheme to a standard Si rib waveguide of width w=450 nm and total height h=350 with a slab height of 100 nm, as for the Ge modulator, was studied. The coupling losses were calculated using 3D FDTD simulations with the commercial software Lumerical and found to be around 1 dB only.

Related Publications :
[1] N. Abadia, T. Bernardin, P. Chaisakul, S. Olivier, D. Marris-Morini, R. Espiau de Lamaëstre, J.-C. Weeber and L. Vivien, "Low-Power consumption Franz-Keldysh effect plasmonic modulator", Opt. Exp. 22, 11236 (2014)
[2] N. Abadia, S. Olivier, D. Marris-Morini, L. Vivien, T. Bernardin and J.-C. Weeber, "A CMOS-compatible Franz-Keldysh effect plasmonic modulator", Proceedings of the Group IV Photonics Conference (2014).

Optics and Photonics

S. Olivier, J.-M. Fedeli, A. Souhaite, D. Perez-Galacho*, D. Marris-Morini*, L. Vivien*, C. Baudot*, F. Bœuf* (* ST Microelectronics, Crolles, France)

ABSTRACT:
Silicon photonics is a key technology to develop low-cost and high-performance optical interconnects. We demonstrate high speed silicon modulators based on carrier depletion in a PN junction implemented in a ring resonator. The modulators were fabricated on a 300 mm SOI platform and feature an efficiency of 2.2 V.cm and insertion losses of 2.5 dB/mm. 40 Gb/s operation is demonstrated at 1550 nm with more than 3 dB extinction ratio.

dispersion effect, using either carrier injection, accumulation or depletion in a PN junction. The latter attracts particular interest due to its high intrinsic bandwidth. The depletion active region can be implemented either in a Mach-Zehnder interferometer [1] or in a ring resonator to convert phase modulation into intensity modulation. The ring resonator has the advantage to be very compact and to feature a low energy consumption for modulation. We report on the development of a silicon ring resonator modulator based on carrier depletion in a PN junction operating at 40 Gbit/s [2].
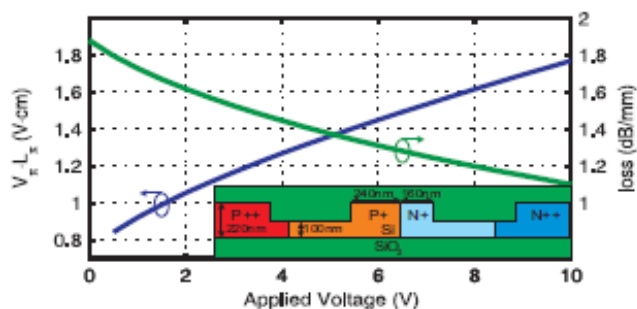

Figure 1: Simulated performance (modulation efficiency and loss) of the designed phase shifter as a function of the reverse applied voltage. (Inset) Schematic cross-section of the phase shifter.

The ring radius is 100 µm and corresponds to a free spectral range of ~0.95 nm. A schematic view of the phase shifter is shown in Fig. 1. The ring modulator waveguide has a width of 400 nm, a total height of 220 nm and a slab height of 100 nm. A lateral PN junction is introduced in the core of the modulator ring. The doping concentrations are $5\,10^{17}cm^{-3}$ and $10^{18}cm^{-3}$ for p-doped and n-doped regions respectively, and larger concentrations of $10^{19}cm^{-3}$ for P++ and N++ regions. When the PN junction is reverse biased, a depletion region is formed in the center of the waveguide. The variation of free carrier concentration induces a change in the refractive index of silicon and thus introduces a phase shift on the light travelling through the ring waveguide.

Fig. 1 shows the simulated modulator static performances. For an applied voltage of 3V, the modulation efficiency given by the product $V_\pi L_\pi$ is 1.2 V.cm and the losses are 1.5 dB/mm.

The modulator was fabricated on a 300 mm SOI wafer with a 2 µm buried oxide (BOX) and a 220 nm Si layer. A silicon dioxide layer was deposited and used as a hard mask, then

employed to define the waveguides. The PN junction was defined by means of four different implantation steps. Finally a metal layer stack of tungsten, copper and aluminum was used to contact the N++ and P++ zones and to define the electrodes.

In order to evaluate the performances of the modulator, TE polarized light was coupled in/out the modulator circuit through vertical fiber grating couplers. The output optical power was measured as a function of wavelength and applied voltage. The critical coupling condition was obtained at wavelength around 1512 nm. Extinction ratio of 20 dB was achieved. Optical loss was lower than 1 dB. A modulation efficiency $V_\pi L_\pi$ of 2.2 V.cm can be deduced from these measurements. Specific test devices were used to evaluate the optical loss of the phase shifter yielding a value of 2.5 dB/mm.
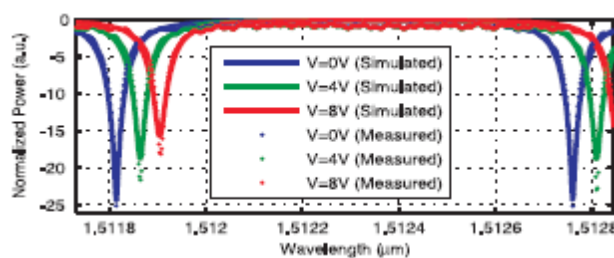

Figure 2: Measured output power as a function of wavelength for several reverse bias applied voltages.

The electro-optical bandwidth was measured, showing a 3 dB cut-off frequency of 26 GHz. Data transmission measurements were performed using a pseudo-random binary sequence electrical signal. Fig. 3b shows an open eye diagram at 43 Gb/s.
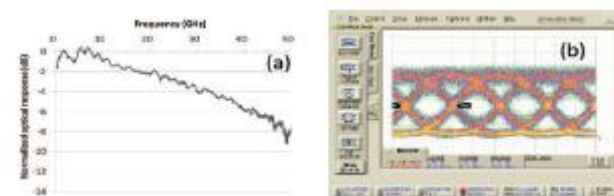

Figure 3: High speed performance measurements. (a) Normalized optical response; (b) Eye diagram at 40 Gbit/s.

Related Publications :
[1] D. Marris-Morini, C. Baudot, J.-M. Fedeli, G. Rasigade, N. Vulliet, A. Souhaité, M. Ziebell, P. Rivallin, S. Olivier, P. Crozat, D. Bouville, S. Menezo, F. Boeuf and L. Vivien, "Low loss 40 Gbit/s silicon modulator based on interleaved PN junctions and fabricated on 300 mm SOI wafers", Opt. Exp. 21, 22471 (2013)
[2] D. Perez-Galacho, D. Marris-Morini, C. Baudot, J.-M. Fedeli, N. Vulliet, A. Souhaité, S. Olivier, X. Leroux, F. Boeuf, L. Vivien,"40 Gbit/s silicon ring resonator based modulator fabricated on 300 mm SOI wafer", Proceedings of the Group IV Photonics Conference (2014)

Photonic-Electronic modules using copper microbumps

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(* LETI/ DCOS)

ABSTRACT: Among the various photonic-electronic approaches which aim at merging electronic drivers and photonic integrated circuits, microbumps present real advantages like: assembly flexibility, process compatibility with CMOS standard flows, and low RF parasitics. Together with 3D packaging technologies like Through Silicon Vias , it enables highly integrated architectures to be designed for next generation modules and photonic interposers.

In order to increase the data rate of photonic integrated circuit (PIC) based telecommunication modules, and to decrease the overall power consumption, it is needed to reduce the RF parasitics between the photonics active functions (photodiode, modulator) and the related electronic circuits (EIC, respectively: amplifier, or driver). Several approaches can be considered, from legacy hybrid modules using high inductance wire bonds to monolithic approaches [1]. Between these two configurations, flip-chip stacking of the EIC onto the PIC using copper micropillars exhibits several advantages.
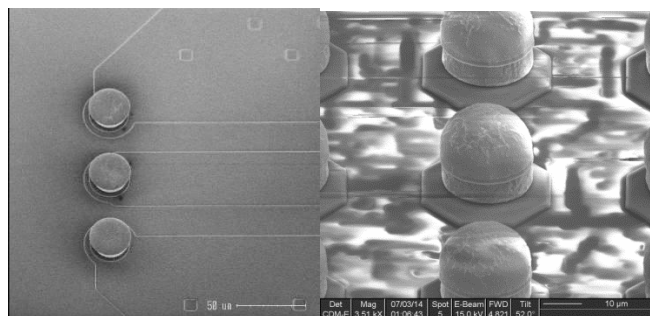

Figure 1 : SEM view of 50µm pitch microbumps made of SnAgCu eutectic solder on the top of a copper pillar.

Among these advantages, one can mention : a great flexibility in assembly ("Known Good Die" approach), density improvement compared to older technologies like wire bonding or stud bump bonding, and reduced capacitance. In addition, this new process is becoming a new standard in CMOS components fabrication flow.

At Leti, we have processed 50µm pitch copper microbumps on Photonic Circuits or Electronic circuits, using Electrochemical deposition (ECD) of copper micropillars with eutectic solder (SnAgCu) on the top, on full 200mm or 300mm wafers (Fig1.).

RF test structures using microbumps to interconnect the top and bottom dies have been used in order to check the very low influence of the microbump interconnection on the RF signal integrity, from DC to 40 GHz (Fig.2). RF parasitics as low as 20 mOhms and 5fF per connection have been modelled.
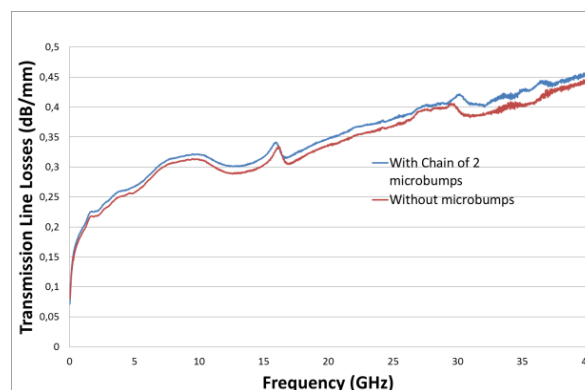

Figure 2 : Microbump impact on transmission losses of test CPW lines.

These structures are now used in functional devices like 4x25 Gbps photoreceiver using a CMOS 65nm amplifier, or a low consumption photoreceiver using a state-of-the art FDSOI electronics circuit [3] which have been assembled at Leti (Fig.3)
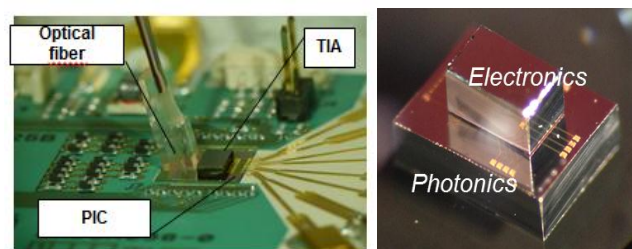

Figure 3 : View of two packaged receiver modules : 4x25Gbps (left) and single channel (right)

Using this interconnection technology, Leti is also building models of advanced photonics micromodules using Through Silicon Vias (TSV), photonics interposers and state-of-the-art organic laminates. These models combine RF, thermal and optical simulations [2].

The modelled modules will address next generation photonics modules used in High performance Computers, with aggregated data rate of 1 Terabit/s ([4]).

Demonstrators will be implemented within the frame of the IRT-Nanoelec Photonics Program with the core partners STmicroelectronics and SAMTEC.

Related Publications :
[1] J.M. Fedeli, F. Schrank, E. Augendre, S. Bernabé, J. Kraft, P. Grosse, T. Enot, "Photonic-Electronic Integration with bonding", IEEE J. of Selected Topics in Quantum Elec., 20,4, 2014
[2] S. Bernabé, "Opportunities and challenges of silicon photonics based System-In-Package" (invited), Panel Session "Emerging Technologies and Market Trends of Silicon Photonics", 64th Electronic Components and Technology Conference (ECTC), Orlando, 2014
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[4] Y. Lamy, H.B. Jamaa, H. Metras, S. Bernabé, S. Menezo, L. Fulbert, "Heterogeneous Integration of photonic integrated circuits using 3D assembly techniques: Silicon technology and packaging", IMAPS (US), 2014

5

Solid State lighting (LED)

Micro. & Nanowire light emitters

LED light extraction

LED packaging

Smart lighting

Complete Solid State Lighting (SSL) Line at CEA LETI

Research topics: Solid State Lighting, LED

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ABSTRACT: With a long experience in optoelectronics, CEA-LETI has focused on Light Emitting Diode (LED) lighting since 2006. Today, all the technical challenges in the implementation of GaN LED based solid state lighting (SSL) are addressed at CEA-LETI who is now an R&D player throughout the entire value chain of LED lighting.

The SSL Line at CEA-LETI first deals with the simulation of the active structures and LED devices. Then the growth is addressed in particular 2D growth on 200 mm silicon substrates. Then, technological steps are developed for the fabrication of LED dies with innovative architectures. For instance, Versatile LED Array Devices are currently being developed with a dedicated µLED technology. The objective in this case is to achieve monolithical LED arrays reported and interconnected through a silicon submount. In addition to the required bonding and 3D integration technologies, new solutions for LED chip packaging, thermal management of LED lamps and luminaires are also addressed.

LETI is also active in Smart Lighting concepts which offer the possibility of new application fields for SSL technologies. An example is the recent development at CEA LETI of Visible Light Communication Technology also called LiFi. With this technology, we demonstrated a transmission rate up to 10 Mb/s and real time HD-Video transmission.

We will focus here on the array LED technology currently being developed at LETI.

Figure 7: (a) Monolithic LED array with a very small pitch. (b) Individual LED characterization after monolithic LED array fabrication: J(V) and L(V) curves

Recently, a "Thin Film Flip Chip (TFFC)" technology, was developed. This structure requires a transfer on a host substrate which has to be functionalized. In this TFFC technology, all the contacts are taken on the same side of the wafer. The TFFC technology was adapted to fabricate Monolithic LED arrays (Figure 2). Monolithic LED arrays with a very small pitch were realized. After process and report, excellent characteristics of individual LEDs were kept: the leakage current densities, the turn on voltage and light turn on voltage measured for a conventional 2D LED process in Figure 1(b) for an individual LED in a LED array are very similar.

Figure 2: Monolithic LED arrays

This monolithic LED technology is being further developed to inter connect the LEDs of the monolithic array in series in order to operate at higher voltage. The process flow is compatible with parallel and/or series interconnections of the individual LEDs of the array. Smart architectures able to switch the LEDs from series to parallel depending on the wall voltage and for dimming are being studied. The design of ASIC integrated drivers and the report on those ASICs is also under study. Those architectures using Versatile LED Array Devices will optimize whole system efficiency and minimize thermal resistivity for heat extraction.
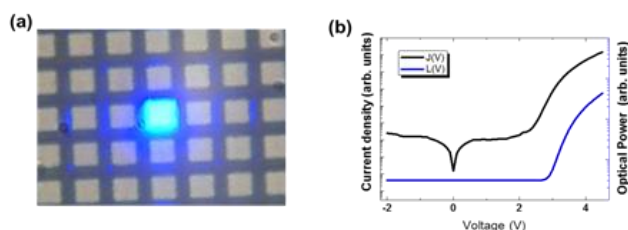
Related Publications:
[1] Robin, I.C., Ferret, P., Dussaigne, A., Bougerol, C., Salomon, D., Chen, X.J. et al, Complete Solid State Lighting (SSL) Line at CEA LETI, SPIE Optics+Photonics (2014)

Growth of Semipolar (20$\bar{2}$1) GaN layers on patterned Silicon (114) 1° off, by Metal Organic Vapor Phase Epitaxy.

Research topics : Semipolar, GaN, Silicon, Selective Area Growth

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ABSTRACT: With the objective of introducing further GaN semipolar orientations adequate for the fabrication of optoelectronic devices on silicon, we report on the selective area growth of semipolar (20$\bar{2}$1) GaN layers on patterned silicon (114) 1° off substrates. The patterning and subsequent anisotropic etching of the Si substrates allows exposing Si {111}-type facets on which GaN grows along the [0001] direction before coalescing and forming a continuous semipolar layer. Observed dislocation bending in the initial growth stages enables improved structural and optical quality leading to significant defect-free regions.

To-date, III-nitride optoelectronic devices are grown along the [0001] c-direction that undergoes two inherent impediments. On one hand the quantum confined Stark effect, which results in spatially separating electrons and holes and consequently, in a significant decrease of optical oscillator strengths; on the other hand, indium incorporation on the (0001) plane is relatively limited when compared with its incorporation on other crystallographic planes. These deleterious effects can be reduced by performing the growth of GaN on planes inclined with respect to (0001), such as semipolar ones leading to the eventual improvement of device performances [A.E. Romanov et al, J Applied Physics, 2006].

Growth of device-quality semipolar GaN, however, comes at a price, and the only currently available option is homoepitaxy which is limited in size, and highly priced. As a result, [Honda, Y. et al. J. of crystal growth, 2002] proposed to use a selective area growth method involving the patterning of silicon (001) 7° off substrates. The essence of the approach was to expose Si (111) facets on which inclined GaN polar growth along [0001] would take place. Further coalescence of consecutive GaN bands allows the formation of a continuous semipolar layer with a reduced density of extended defects. This approach was developed in 2008 on Si (113) to yield (11$\bar{2}$2) GaN and subsequently adapted for the growth of semipolar layers on sapphire substrates.

In this communication [1], we report on the selective area growth of semipolar (20$\bar{2}$1) GaN layers on patterned silicon (114) 1° off substrates [1]. The patterning and subsequent anisotropic etching of the Si substrates allows exposing Si {111} facets on which GaN grows along the [0001] direction. Upon coalescence of neighboring GaN stripes, a continuous (20$\bar{2}$1) semipolar layer is obtained, displaying a facetted surface morphology dominated by more thermodynamically-stable crystallographic planes, i.e. semipolar (10$\bar{1}$1) and nonpolar (10$\bar{1}$0) (Figure 1).
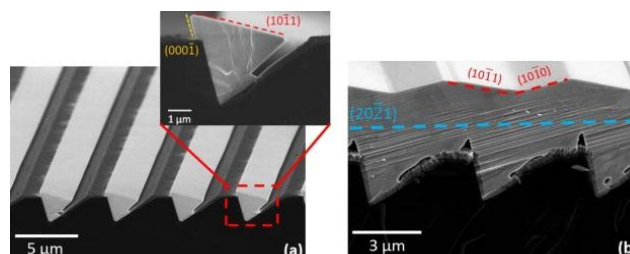

Figure 1: (a) Bird's eye view SEM image of the crystals in the initial growth stages (inset: cross-section of a single crystal), and (b) the coalesced layer displaying the alternating micro-facets.

Transmission electron microscopy shows that dislocation bending in the early growth stages determines the structural quality of the final semipolar (20$\bar{2}$1) layer (Figure 2a - illustration shown instead for clarity). Optical characterization by cathodoluminescence (CL) displays regions having threading dislocations (black spots) and stacking faults (white clusters) alternating with almost defect-free regions, which correlate well with the transmission electron microscopy study (Figure 2b).
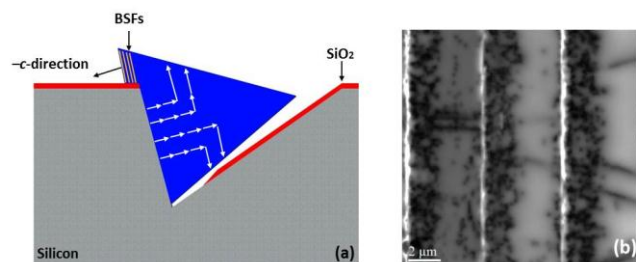

Figure 2: (a) Cross-sectional illustration of TD bending (b) the corresponding plane-view panchromatic CL image (77K).

The selective area growth described in this work is anticipated to be a first step towards using the (20$\bar{2}$1) semipolar orientation in a practical process to achieve low-cost devices on semipolar GaN-on-silicon.

Related Publications:
[1] M. Khoury, M. Leroux, M. Nemoz, G. Feuillet, J. Zúñiga-Pérez, and P. Vennéguès, Growth of semipolar (20$\bar{2}$1) GaN layers on patterned silicon (114) 1° off by metal organic vapor phase epitaxy, Journal of Crystal Growth, in press.

Sample preparation of heterogeneous semiconductor structures for (S)TEM analyses: The case study of III-N on Si-based substrates

N. Mante, G. Feuillet, V. Delaye*, G. Audoit*, and P. Vennéguès*
(*CNRS / CRHEA, Sophia Antipolis)

A dedicated process has been developed to obtain TEM samples for the particular case of heterogeneous structures. It consists in preparing wedge shaped samples, by controlled mechanical polishing and ion milling, leading to large observation areas without any unwanted preparation artefact. The technique is demonstrated for nitrides epilayers grown on either Si or SOI substrates

Gallium nitride is a widely used material in optoelectronic devices like LEDs. The LED structures are mostly grown by epitaxy onto sapphire substrates, but, for cost reasons, silicon is studied as a possible contender.

In order to better understand the growth mechanisms of nitrides on silicon and to assess the structural quality of the epitaxial layers, one has to resort to TEM. Then one is left with the problem of preparing cross section samples of stacks of materials with different mechanical properties or chemical reactivity like GaN on the one hand and Silicon on the other hand. The problem is even more acute when the grown structure is composed of different nitride materials like AlN and GaN and/or when the Si substrate is non-monolithic like for instance silicon on insulator (SOI).
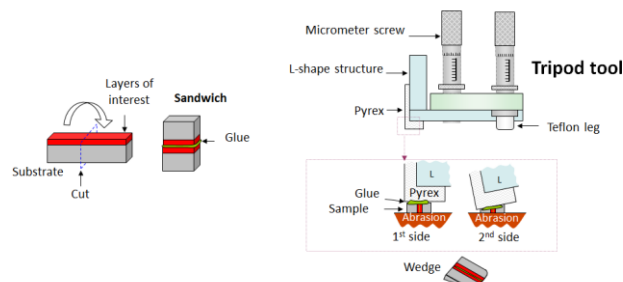

Figure 1: Wedge polishing principle.

In order to tackle the problem, we have developed a particular process (fig. 1) and implemented it on the Nano-Characterization Platform (PFNC). The process was carried out for GaN/AlN heterostructures grown either on Si or SOI (Silicon on Insulator) substrates, so as to obtain TEM samples without any preparation induced artifacts [2]. Indeed, this is not the case for usual TEM preparation techniques like FIB (Focused Ion Beam) or PIPS (Precision Ion Polishing System). These ones are mainly ion based preparation techniques, creating some implantation defects or surface re-depositions. The process is based on a wedge polishing method. It consists in polishing the sample with a very low angle (1-4°), in order to obtain an area on the wedge thin enough for TEM observations. The obtained samples need to be as thin as possible, without any induced preparation damage in order to carry out complete (S)TEM studies: from high resolution allowing to analyze interfaces at atomic scale (fig. 2), to diffraction contrast studies with fields of view reaching several µm². These large areas are necessary in order to yield a better statistics of defects in the layers and to better understand dislocation behavior (fig. 3).

From fig. 2, no surface amorphization or re-deposited species could be detected using this controlled tripod polishing method, which would otherwise drastically hamper high resolution TEM observations.
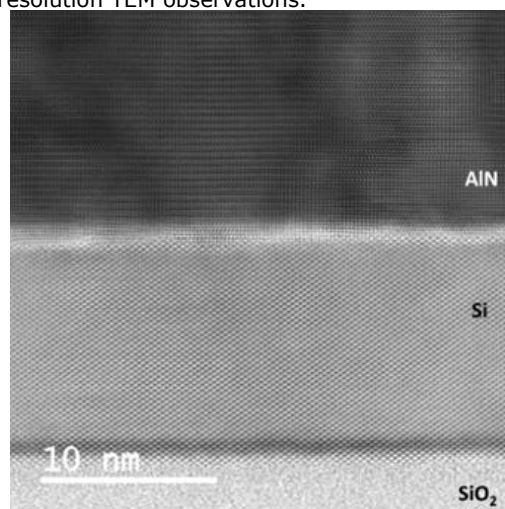

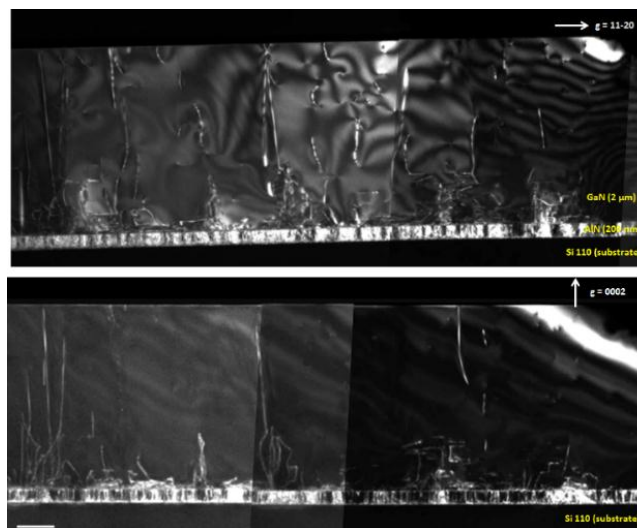Figure 2: HRSTEM image of an AlN/SOI interface.

Figure 3: Dark Field TEM image of a GaN/AlN/Si stack.

The samples studied were grown in CRHEA CNRS laboratory in Sophia Antipolis, then prepared with an "Allied Multiprep" polishing tool. TEM observations were done on PFNC microscopes, especially the FEI-Titan at 300 kV.

Related Publications:
 [1] M. Khoury, M. Leroux, M. Nemoz, G. Feuillet, J. Zúñiga-Pérez, and P. Vennéguès, Growth of semipolar (20‾21) GaN layers on patterned silicon (114) 1° off by metal organic vapor phase epitaxy, Journal of Crystal Growth, in press.

Direct Imaging of p-n junction in Core-Shell GaN wires

Research topics: Solid State Lighting, LED, Nanowires

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ABSTRACT: While wire-based devices are promising for optoelectronic applications such as LEDs, their development is hampered by the present uncertainty about essential semiconductor properties. Thanks to a cross-sectional approach, scanning electron beam probing techniques were used here to obtain a spatially resolved analysis of GaN core−shell wire p−n junctions. This nanoscale approach provides essential guidance to the further development of core−shell wiredevices.

Core-shell wire-based devices offer a promising path toward improved optoelectronic applications. Similar to the planar epitaxial case, measurements of material properties in these three-dimensional (3D) structures are crucial to fabricate efficient optoelectronic devices. Because of this 3D geometry, the full promise of core-shell wire devices relies on a nanoscale spatially resolved understanding of their properties along the axial (c-plane) and radial (m-plane) p-n junctions.

A combination of scanning electron beam probing techniques such as Electron Beam Induced Current (EBIC) and Secondary Electron (SE) Voltage Contrast (VC) was used to directly image the 3D p-n junction present in a cleaved GaN core-shell microwire[1].
Core-shell GaN microwires with buried p-n junction were grown using catalyst-free MOVPE on N-polar GaN free standing substrate and n-type (100) silicon substrate. After collective contact process of a wire group on its growth substrate, a simple manual cross-sectional approach provided access to the 3D buried junction and was found to be successful for GaN substrates as well as for Si substrates (Fig.1a).

EBIC measurement demonstrates the presence of a radial junction along the non polar m-plane sidewalls even on uncleaved wires (Fig.1b) while inspection of cleaved wires also reveals the existence of an axial junction along c-plane at the top of the wire. This demonstrates the interest of the cross-sectional approach to readily image the p-type shell presence all around the n-type core and the p-n junction activity in core-shell wire-based devices.
Thanks to a controlled ebeam exposure on wires without p-GaN activation annealing, EBIC mapping was also evidenced to dynamically infer Mg dopant ebeam activation.
This provides a probe to locally check the success of an activation annealing (Fig.1c).
From EBIC profile (Fig.1d), minority carrier diffusion length on n- and p-side was inferred to be $L_n=15$ nm and $L_p=55$ nm in the radial junction. Depletion width W was also determined in the range 50-60 nm for a bias voltage of 0 V while this value was found to follow a V1/2 dependence with applied reverse bias as expected in an abrupt p-n junction model.

VC technique is shown not only to delineate the 3D p-n junction but also to locally map the electrostatic potential

In its vicinity (Fig.1e). The depletion widths on both n-side Wn and p-side Wp were directly extracted from SE profiles. Then, by using classical p-n junction theory, both donor Nd and acceptor Na doping levels were spatially estimated.

The good agreement in measured W from EBIC and VC measurement demonstrates the consistency of these ebeam probing approaches, which paves the way to the development of more efficient core-shell wire-based p-n junction devices.
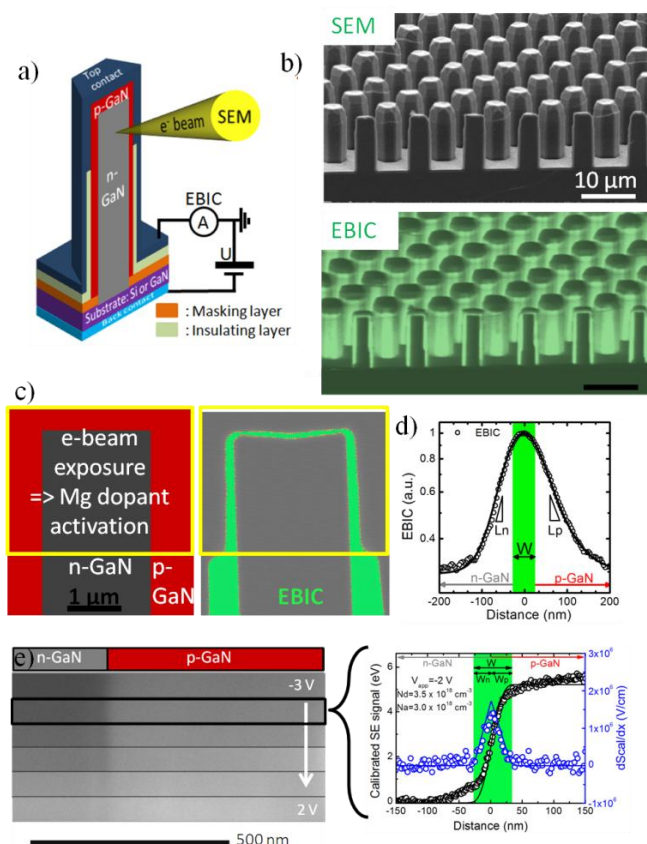
Related Publications:
[1] Tchoulfian, Pierre, et al. "Direct Imaging of p−n Junction in Core–Shell GaN Wires." Nano letters 14.6 (2014): 3491-3498.

GaN on SOI: from growth investigations to devices

Research topics: GaN, AlN, SOI, substrate

G. Feuillet, N. Mante, P. Gergaud and F. De Crécy (CEA/ LETI/ DCOS)
F. Semond*, E. Frayssinet*, Y Cordier*, B. Damilano*, J. Brault*, M. Leroux* , P. Vennegues*,
R Comyn*, M. Portail*, V. Brändli*, S. Chenot*, G. Gommé*, M. Khoury*, M. Nemoz*, J. Zúñiga-Pérez*, and P. Vennéguès* (* CNRS CRHEA, Valbonne, France)

ABSTRACT: While wire-based devices are promising for optoelectronic applications such as LEDs, their development is hampered by the present uncertainty about essential semiconductor properties. Thanks to a cross-sectional approach, scanning electron beam probing techniques were used here to obtain a spatially resolved analysis of GaN core−shell wire p−n junctions. This nanoscale approach provides essential guidance to the further development of core−shell wiredevices.

The growth of GaN based layers and heterostructures on Si is handicapped by the presence of numerous dislocations because of the misfit between layer and substrate and the textured type of growth, and by the possible cracks induced by the large thermal mismatch between the nitrides and Si. Complex growth processes have been employed to cope with these problems, which mostly result in lengthy epitaxial processes and add up to the cost of the envisaged device.

Using compliant substrates could be an alternative that allows one to circumvent the difficulties. Indeed, theoretically, compliance would allow the epitaxial or thermal stress to be shared between substrate and epilayer and/or would allow dislocations to be partially buried into the substrate. We have used SOI (Silicon On Insulator) substrates to try and implement this idea. SOI substrates with different top Si thicknesses and/or different orientations have been selected.

On « thick » SOI, i.e. with a 2µm top Si layer, MOVPE nitride layers have structural and optical properties identical to those of layers grown onto bulk Si; in particular, low dislocation densities, down to $2.10^8/cm^2$, were routinely obtained (figure 1-a), which is a low figure for GaN when grown onto Si. Similarly, nitride devices (LEDs and HEMT) have properties identical to those obtained on bulk Silicon (figure.1b). Indeed, one would not expect any compliance when using thick SOI, with no strain partitioning effect. But being a heterogeneous substrate, one can take advantage of SOI substrates in that they would allow for processes difficult to implement when using bulk Si substrates or add new opportunities while keeping the quality of the grown nitride devices identical. Among others: easy layer transfer, increased and simplified light extraction, electrical insulation from the substrate, low loss wave guiding etc…
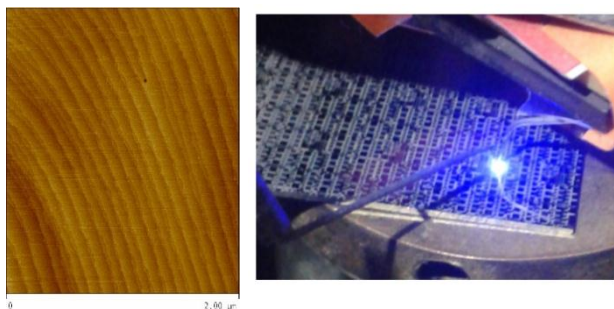
Beyond this validation step, "thin" SOI was used to try and demonstrate if compliance effects were actually occurring. For this purpose, we grew nitride layers (starting with an AlN buffer before growth of the GaN layer itself) on top of "thin" SOI substrates with a 15 nm thick, but <110> oriented (instead of usual <111>) top Si layer; in this case, the misfit at the interface is non isotropic: on one direction, the involved misfit is rather small, of the order of 0.8%, while in the orthogonal direction, the misfit is large, 19 %. This somehow allows us to study the compliance effects according to the involved misfit. Using large TEM examination zones, the number of dislocations present at the AlN/Si interface was counted in the case of bulk Si and SOI substrate; it was found that in the high misfit direction of the interface, misfit dislocations were present with exactly the same concentration for the two cases, while in the low misfit direction, less or no dislocations were present in the case of SOI, possibly indicating elastically strained layers in this case. For further analysis, microdiffraction in the TEM is being carried out to map out the strain at the atomic level in the different epitaxial layers in the two cases.
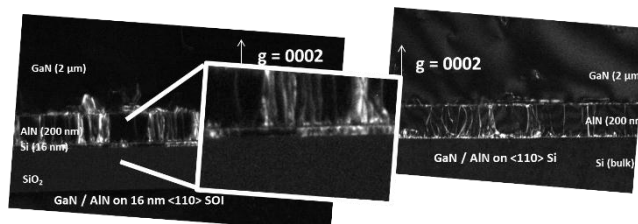

Figure 2: Cross sectionnal TEM of the GaN /AlN stack on "thin" SOI (left) and on bulk Si (right) in the "high" misfit direction of the AlN/<110> interface.

As seen from the TEM cross sectional view of figure 2, the contrast in the Si top layer of the SOI might also indicate that plastic deformation has occurred. Further analysis is in progress to confirm or infirm these points.

These two findings relate to the strain state of the AlN interlayer, but no strain relaxation was found out, either through structural of optical characterization, in the GaN layer. Work in progress relates to the effect of nano-patterning the SOI substrate to try and facilitate elastic and plastic compliance effects in the overall epitaxial stack.

Figure 1: left- AFM image of the GaN surface grown onto "thick" SOI substrate. right: electroluminescence of LEDs on "thick" SOI.

Thermal management: a key point for the integration in Solid State Lighting systems

Research topics: thermal management, LED, packaging, lamp

A Gasse, A Ait-Mani

ABSTRACT: Thermal management strongly impacts efficiency but also color stability and reliability of LED-based systems. We analyzed the heat transfer mechanisms and their impact on the choice of materials and integration technologies. Transient thermal analysis was performed to derive both the junction temperature and the discrete thermal resistances of the systems. In particular, we present results on LED light engines based on the Chip On Board technology ; finally, the optimization of the heat sink is presented on a LED retrofit MR16 lamp.

Thermal management in SSL systems has already been extensively described at the die and component level [1]. In fact, thermal dissipation occurs at each level of integration: chip, package, board and finally heat sink. In this paper [2], we propose to focus first on the Chip On Board technology. Then the optimization of the heat sink is presented on a LED retrofit MR16 lamp.

To suppress the component thermal resistance, it has been proposed to use Chip On Board (COB) technologies but the improvements are not straightforward due to spreading effects. The impact of the die size was evaluated in a COB configuration where the dielectric thermal conductivity is changed. T3ster® measurements have also been conducted on samples having a COB configuration (1 mm² die) as well as on a standard XP-E. Below a 2 mm edge die size, the MCPCB thermal resistance increases exponentially.

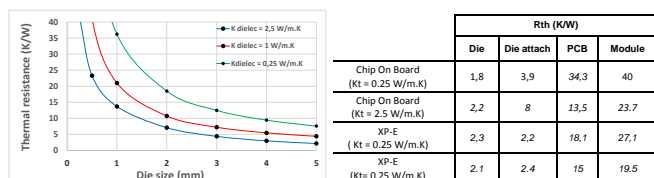|		Rth (K/W)		
	Die	Die attach	PCB	Module
Chip On Board (Kt = 0.25 W/m.K)	1,8	3,9	34,3	40
Chip On Board (Kt = 2.5 W/m.K)	2,2	8	13,5	23.7
XP-E (Kt = 0.25 W/m.K)	2,3	2,2	18,1	27,1
XP-E (Kt= 0.25 W/m.K)	2.1	2.4	15	19.5

Figure 1: Impact of the die size of the COB PCB thermal resistance (analytical simulation) and T3ster® experimental results

Using the COB configuration in place of a XP-E component on the same board does not reduce the total thermal resistance but it is on the contrary almost doubled due to the large spreading effect in the low thermal conductivity dielectric. Using a high thermal conductivity material for the dielectric layer allows to drastically reduce the thermal resistance in the Chip On Board configuration of about one third (~34 to 13 K/W). Note also that the COB measurements values are in a relative good agreement with the calculated thermal resistances. Such improvements have also been observed on LED engines made of either a low thermal conductivity MCPCB with XP-E components and a Chip On board ones on a high thermal conductivity MCPCB [3]. Taking into account the thermal load, the gap in thermal resistance leads to a 20 °C difference. The consequences are a 7 % increase in light flux with an estimated doubled lifetime in the COB configuration

In a MR16 type spot, the heat sink should have a specific small volume and the working environment is generally confined in a recessed casing with a limited convection. We designed a MR16 prototype in view of optimizing all the internal thermal resistances of the lamp.
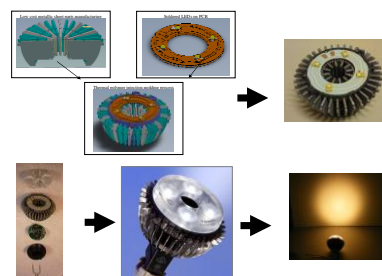

Figure 8 : Basic design of the MR16 LED lamp

First of all the LED engine is located at the vicinity of the heat sink made of thin fins embedded in a thermal polymer by an injection process. The architecture also allows to cool the electronic driver board which is a very sensitive part as well because it includes an electrolytic capacitor. In addition, the structure includes a central hole to enhance convection within the lamp. To characterize the thermal behavior, thermocouples have been located in different areas of the lamp (board, fins near or away from the board, capacitor….). Measurements have been carried with/without a potting material for the thermal coupling heat sink/driver. In addition, effect of free or confined air (representative of a recessed environment) has been assessed. Some of the results are summarized in the graph below.
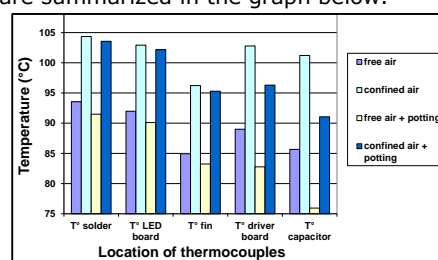

Figure 9 : Thermocouples measurements in free or confined air with/out potting of the electronics

Without going into details, it is shown that the recessed environment increases the temperature of about 10°C for the LED board and about 15°C for the capacitor. Potting of the driver board has a minor effect on the LED board but allows to decrease the capacitor temperature of about 10°C as well. The influence of the emissivity of fins, number and spacing of fins has also being investigated allowing to have a heat sink thermal resistance as low as 8 K/W for such a compact system. Thermal cycling, High Temperature Operating Life and Humidity testing have proved the robustness of the concept.

Related Publication:
[1] Pardo, B., Gasse et al, (2013) Microelectronics Reliability 53 (8) PP. 1084 – 1094
[2] A. Gasse, A. Corfa, S. Bernabe, N. Aitmani, N. Lhermet, D. Henry, P. Alibert, Thermal management: a key point for the integration in Solid State Lighting systems, 5th ESTC Conference, 16/09/2014 - 18/09/2014, Helsinki , Finlande,
[3] A. Aitmani et, State of the Art of a LED Module using Chip on Board Technology, 4th Micro/Nano-Electronics Packaging and Assembly Design and Manufacturing Forum 2014 – IMAPS Europe, Grenoble.

LED dynamic electro-optical characterization: A key domain for Lighting and Smart Lighting applications

Research topics: LED, Dynamic ElectroOptics, LiFi, Smart Lighting, LED drivers

D. Vaufrey, D. C. Nguyen, E. Bialic, A. Lagrange et L. Maret* (*LETI/ DSIS)

ABSTRACT: With a long experience in optoelectronics, CEA-LETI has focused on Light Emitting Diode (LED) lighting since 2006. Today, most of the technical challenges in the implementation of GaN LED based solid state lighting (SSL) are addressed at CEA-LETI among which we find High Efficiency LEDs, LiFi, new drivers architecture.

LED open new domains for the lighting industry. Not only novel LED structures, as Nanowire LED developed and spun off (ALEDIA), but also innovative driver architectures and smart lighting uses (LiFi) required a strong knowledge of LED dynamic behavior.

High efficiency LED require an extremely well controlled balance of both electron and hole transport in the LED structure. Innovative drivers are based on high frequency power modulation to reduce passive component size and cost. And LiFi (or visible light communication) need for high speed LEDs and optimized modulation schemes.

We have developed an expertise in dynamic Electro optical characterization of LED based on
1. Impedance Spectroscopy
2. Pulsed Electroluminescence
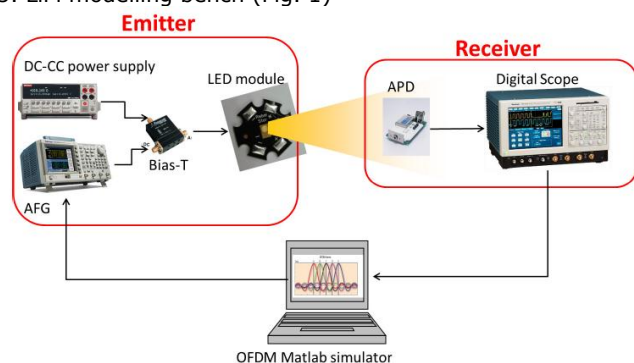3. LiFi modelling bench (Fig. 1)

Figure 1 :Example of LiFi modelling bench used for Dynamic Electro Optics Characterizations.

The impedance spectroscopy studies led to the construction of an equivalent electrical model of commercial LED as shown in figure 2 & 3.
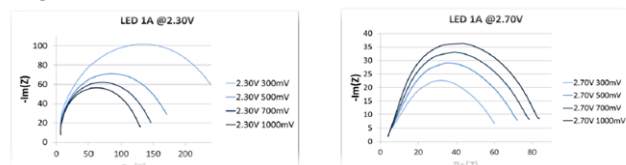

Figure 2: Electrical characteristics of commercial LED (CREE at 2.3V and 2.7V)

In Parallel, pulsed electroluminescence measurements have pointed that intrinsic LED opto-electrical bandwidth is slightly higher than few MHz as displayed in figure 4. Consequently pulsed driver design has been modified to overcome this

frequently limitation. The first experiments are expected in 2016.

$$R_p = Re(Z) + \frac{[Im(Z)]^2}{Re(Z)} \quad (1)$$

$$C_p = -\frac{1}{2\pi f} \frac{Im(Z)}{[Re(Z)]^2 + [Im(Z)]^2} \quad (2)$$

Figure 3: Equivalent Electrical Model for a LED used for driver optimization.
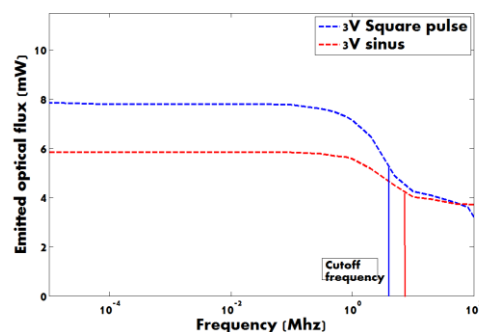

Figure 4: Bode diagram of a commercial LED for 3V square and sinus voltage applied

LiFi test bench have pointed that the bandwidth for visible light communication was larger than few MHz. This is due to the modulation scheme that have been used: OFDM, which supports very low signal levels. But it has also pointed out that the SNR curves and the resulting acceptable bandwidth was strongly dependent on operating point of the driver (Vf and I).
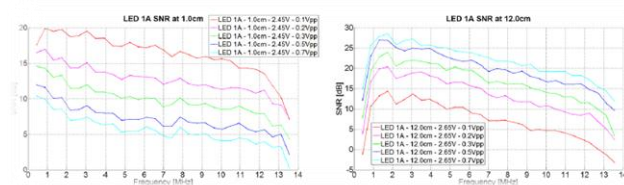

Figure 5 : LiFi characteristics of commercial LED (CREE at 2.45V and 2.65V)

In addition, these characterizations and their results explain dynamic behavior of the ZCE of a LED. This point is important for the technological design of higher efficiency structures.

Related Publications:
[1] Bialic, E., Nguyen, D,C; Vaufrey, D, LED dynamic electro-optical responses and light-fidelity-application optimization, Applied Optics 53(31) (2014)

Light extraction in Chip On Board (COB) LED modules

Research topics: Solid State Lighting, LED, Chip On Board technology, ray-tracing

M Consonni, J Routin, A Piveteau* and A Gasse
(*CEA/ LITEN, DTNM)

ABSTRACT: High-power LEDs require a high-efficient packaging to optimize their performances for lighting. In order to optimize the thermal and optical properties of Chip On Board (COB) light sources and to propose high optically efficient encapsulation geometry, ray-tracing simulations have been performed. The impact of the shape and volume of the silicone encapsulation on the light extraction and on the intensity distribution of the module was derived. Then, simulation results were correlated with experimental measurements on blue light-emitting COB sources. It is shown that a nearly hemispherical encapsulation is the optimal configuration regarding both the light extraction and the intensity distribution.

The integration of high power LED chips for SSL requires an efficient packaging with low thermal resistance and compact size, of which Chip On board implementation is very promising. From the optical point of view light extraction is a key parameter. At the package level, the extraction is limited by the losses which occur during light propagation within the package. A lot of work has been done to reduce these losses and to optimize the light extraction of a packaged LED. Nevertheless, to our knowledge, these works stayed at the theoretical stage, and they were not demonstrated experimentally. That is why we combined both a ray-tracing and an experimental approach for optimizing the light extraction and intensity distribution of a LED COB module. The experimental results are found to be in good agreement with simulations.

First studies were focused on the impact of the encapsulation shape defined by the H/R ratio where H is the height of encapsulation and R the radius diameter respectively (fig. 1).
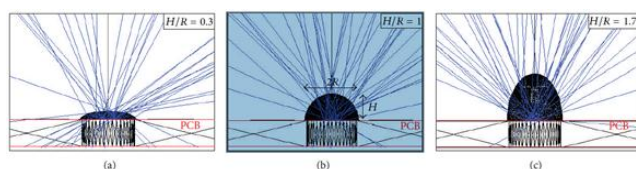

Figure 1 : Cross-sections of the geometries for evaluating the impact of the encapsulation shape (a) Nearly flat encapsulation, with an aspect ratio H/R of 0.3; (b) hemispherical encapsulation; (c) oblong encapsulation, with an aspect ratio H/R = 1.7.

From simulations, the related relative light extraction efficiency and light intensity distribution are shown in figures 2 a) & b)
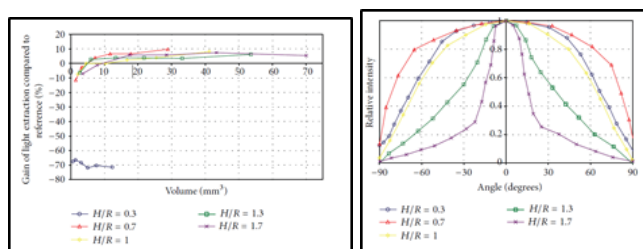
Figures 2: a) Variation of the light extraction and b) light intensity distribution as a function of H/R aspect ratio (Reference with R =1.4 mm)

Chip On Board modules have been manufactured with various H/R ratios using a 1.35 mm² LED die and silicone encapsulation (fig. 3).
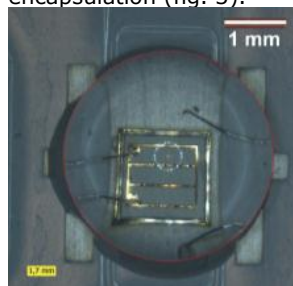

Figure 3: Top view of one LED COB module.

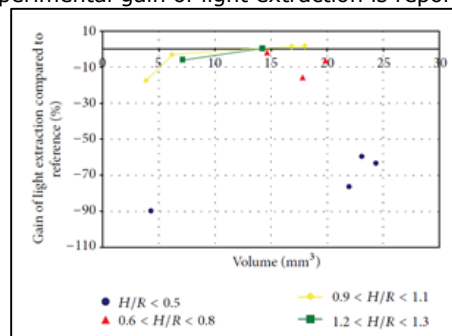The experimental gain of light extraction is reported fig. 4.

Figure 4: Gain of light extraction as a function of the encapsulation volume for various H/R ratio (experimental results).

These measurements confirm the simulation results which stipulated that a flat encapsulation never provides a good light extraction. Whatever the encapsulation volume is, the samples which present an aspect ratio H/R smaller than 0.6 all lead to a poor light extraction. The dispersion is larger than the simulated one. This is mainly due to the fact that the encapsulation shapes are not always ellipsoidal as it was modeled in the simulations. Nevertheless, these light extraction measurements generally show the same trend than the one which was observed with the simulations. Angular distributions measurements (not shown) are also in accordance with simulations.

Next studies will be devoted to apply these results to white modules and to optimize the insertion of phosphors particles within the encapsulation to obtain efficient white LED COB light sources.

Related Publications:
M. Consonni, J. Routin, A. Piveteau and A. Gasse, Combined Experimental and Monte-Carlo Ray-Tracing Approach for Optimizing Light Extraction in LED COB Modules, ISRN Optics, Volume 2013, Article ID 385345, 5 pages,

LED reliability studies: automotive packaging, failure analysis and life time prediction

Research topics: reliability, LED, failure analysis, intermetallics, life time prediction

L. Mendizabal, B. Chambion, B. Hamon, A. Gasse

ABSTRACT: Reliability studies are a key point for the acceptance of LED lighting sources. In this paper, we first discuss these issues through temperature and current robustness tests (out of Safe Operating Area) on automotive multi-chip modules. Then we focus on a particular flip chip component through a detailed analysis of electrical contacts degradation during temperature and current aging. Then a study is performed to quickly predict the lifetime of components based on crossed electrical and optical measurements.

Due to high brightness light sources needs in automotive, LEDs are packaged in multichip module (e.g. 4 chips in series), to deliver up to 1000 lumens at 1A. Currently, different packaging strategies have been implemented in terms of chip configuration (VTF, Flip Chip), bonding, down conversion phosphor layer and mechanical protection to optimize performances. In this context, a methodology is proposed to define and anticipate failure behaviors of each LEDs module through a robustness study (over-stress) [1, 2]. LED A and LED B are respectively based on VTF and FC A setup measurement has been developed focusing on the monitoring of electrical, optical, and thermal parameters of these modules during thermal and electrical step-stress robustness tests.
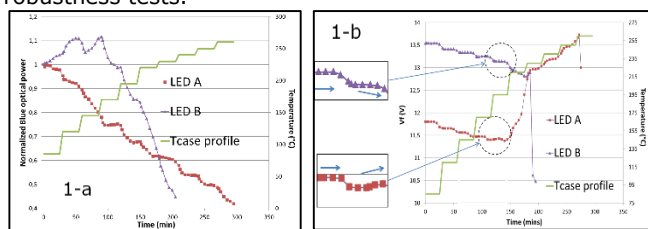

Figure 1: Variations of the Normalized blue optical power during the temperature step-stress test and Vf for each LEDs module during the temperature step-stress test (1a) and zoom on Vf shift beginning (1b).

The behavior of LED B is explained by cracks in the phosphor layer (phosphor powder dispersed in silicone) which was confirmed by the failure analysis. Because LED A uses pure inorganic phosphor layer (sintered phosphor plate, non-organic material), the optical power steady decrease during the test is evidenced (no structure modification due to temperature). The analysis of the Vf shift and then catastrophic failure is attributed to a delamination for the LED A and wire bonding melting (VTF) and degradation of contacts and finally cracks for LED B (Flip Chip).
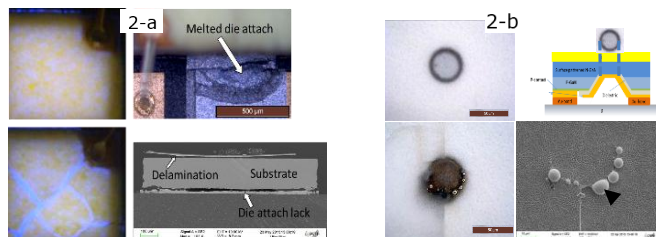

Figure 2: Failure analysis of LED A (2-a) and B (2-b).

This last behavior has also been observed during aging in temperature and current within the SOA [3]. It was shown that inter-diffusion led to the Au4Al intermetallic formation at N-contact area.

The same robustness methodology was operated as a current step-stress. Based on these results, we extracted the strength and weakness of each LEDs module packaging strategy against thermal or electrical over-shots.

	Temperature Step-stress Test		Current Step-stress Test	
	LED A	**LED B**	**LED A**	**LED B**
V_f variation before failure	Increasing	Decreasing	Increasing	Decreasing
Failure mode	Short-circuit	Short-circuit	Open-circuit	Open-circuit
Failure mechanism	GaN cracks at via level	Hot spot at N-type contact	GaN layer delamination	Wire bonding melting
Impact on optical efficiency (functional devices)	-5%	0%	-2,5%	0%
Impact on R_s (functional devices)	+79.5%	0%	+31.2%	0%
Failure kinetic	Progressive	Catastrophic (partial failure)	Progressive	Catastrophic

Table 1: Temperature and current robustness tests summary.

For lifetime prediction of a specific flip chip component [4], 150 have been aged using nine current-temperature stress conditions. With I(V) and optical measurements, a cross study has shown two main failure mechanisms regarding lumen maintenance.
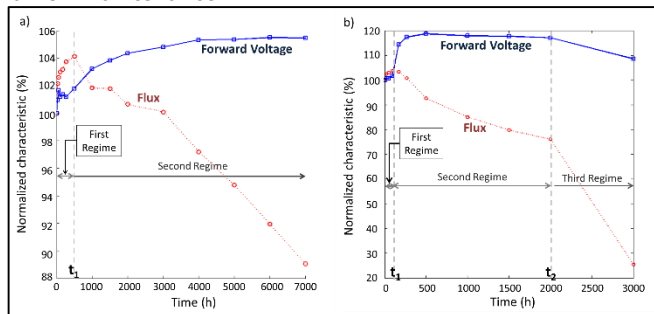

Figure 3: Normalized flux and forward voltage vs. time for (a) 700mA/80°C aging condition and (b) 700mA/120°C aging condition highlighting three regimes of variations

The first one is the typically observed lumen depreciation and the second one is a much quicker depreciation related to an increase of the leakage and non radiative currents. Models of the typical lumen depreciation and leakage resistance depreciation have been made using electrical and optical measurements during the aging tests. The combination of those models allowed a new method toward a quicker LED lifetime prediction.

[1] B. Chambion et al, Electro-optical strength assessment of white LEDs multichip modules for automotive forward-lighting application: Failure analysis and packaging influence (2013) EMPC 2013

[2] B. Chambion et al, Electro-optical characterizations for robustness assessment of automotive qualified white LEDs multichip modules: failure analysis and packaging influence, 10th ISAL; 23/09/2013 - 25/09/2013; Darmstadt; Allemagne

[3] B. Hamon et al, N-contacts degradation analysis of white flip chip LEDs during reliability tests, Reliability Physics Symposium, 2014 IEEE International, 1-5 June 2014, Page(s):FA.1.1 - FA.1.6, Waikoloa, HI

[4] B. Hamon et al, A new lifetime estimation model for a quicker LED reliability prediction, Proc. SPIE 91907, Int. Conf. SSL (2014)

6

Display components

Electrical modeling, active matrix

OLED micro-displays technology

OLED encapsulation

Visualization systems

Head-up displays

High luminance white fluorescent OLED via WO3/Ag/WO3 cathode engineering to enhance light out-coupling

K. Bouzid, T. Maindron, H. Kanaan and E. Viasnoff

ABSTRACT: An alternative design of a semitransparent cathode for top emission white fluorescent OLED has been investigated. The use of an optical simulation tool allowed the optimization of the tri-layer cathode WO3/Ag/WO3 to increase the light out-coupling coefficient of the device for a broad band visible spectrum. The WO3/Ag/WO3 (WAW) cathode was confirmed to be compatible with Atomic Layer Deposition (ALD) technique for thin film encapsulation purposes. An increase of ca. 40 % in luminance was obtained .

Organic light emitting diodes (OLED) are becoming increasingly present in today's technological products, especially in display and lighting applications. Several generations of OLED structures have been presented since Tang's hetero-structure based on Alq3 [C.W. Tang, & al, Appl. Phys. Lett., 51 (12) (1987)] as well as p-i-n stacks, allowing very low turn on voltages and implementation of hole blocking layers (HBL) for better charge confinement [J. Birinstockm, & al, IDW'04, 1265 (2004)]. Nevertheless requirements in luminance continue to increase for display applications such as Head Mounted Displays (HMD) and for white OLED lighting panels to be competitive compared to LED-based LCD panels. These requirements can go up to 100000 cd/m² and it seems delicate to reach these numbers only by engineering exciton recombination process and charge carrier balance or concentration. It is known that common semi-transparent electrodes such as Ag thin films or bi-layers such as Mg/Ag, Ba/Ag or Ca/Ag are outclassed by multilayer structures such as dielectric/metal/dielectric (DMDs). WAW electrodes already presented as a way to increase light extraction for monochrome devices [K.S. Yook & al, Appl. Phys. Lett., 93, 013301 (2008)]. Their implementation in top-emission OLEDs as a cathode was also been documented [K. Hing, & al, j. Phys. Chem. C, 115, 3453 (2011)]. Due to the very small pitch of pixels, micro-displays and some larger displays rely today on the white emission plus RGB color filters concept. WAW cathodes for such white OLEDs should also fit the electrical characteristics requirements for displays. Here we report OLED devices with WAW films used as a cathode, optimized for white emission, compatible with ALD deposition used for thin-film encapsulation and displaying unchanged current density versus voltage characteristic compared to control device.
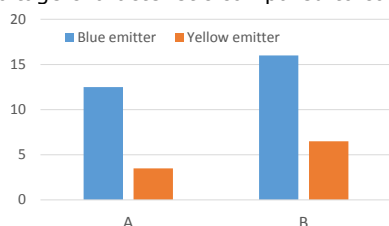

Figure 1: Mode analysis simulation results concerning light out-coupling of devices A and B for blue and yellow emitters

Device A and device B were compared. Their basic structure are as follows: anode / p-doped HIL (29 nm) / Yellow-doped HTL (5 nm) / Blue-doped ETL (27 nm) / HBL (5 nm) / n-doped EIL (22 nm) / cathode / Al2O3. For device A, the cathode is a semi-transparent Ca (7 nm)/ Ag (10 nm) metallic bilayer; for device B, the cathode is made of the WAW sequence with Wo3 (5 nm)/Ag (10 nm) / WO3 (25 nm). Using the commercial software SETFOS from Fluxim, simulation results have been provided (Figure 1).

In these top-emitting OLEDs, adjustment of the resonant frequency of the micro-cavity has allowed balancing the blue and yellow emitters' contributions to the final spectrum. Thickness adjustments were also made in order to keep the exciton recombination zone relative position, i.e. the interface between the yellow doped HTL and the blue doped ETL, constant within the micro-cavity. One can observe that device B has a better light out-coupling than control device A for both emitters. Figure 2 shows the current density and luminance versus voltage for control device A and device B. Current density curves are identical, which testify a good electron injection from the WAW cathode. Concerning the luminance, device B displays an increase of 30.6 % at 5 V, 39.5 % at 6 V and 42.74 % at 7 V with respect to control device A.
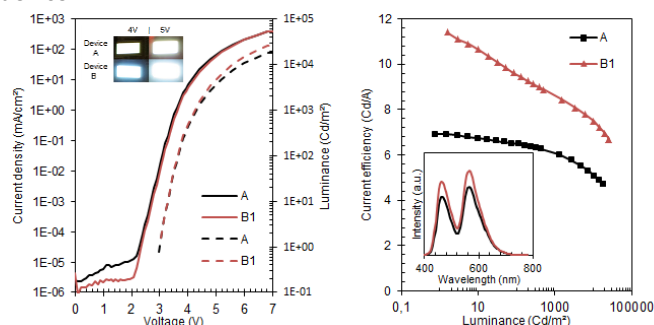

Figure 2: (left) Current density (full lines) and luminance (dashed lines) versus voltage for devices A and B - (inset) Photography of devices A and B at 4V and 5V; (right) Current efficiency versus luminance - (inset) spectra of devices A and B at 1000 cd/m²

The J-V curves, almost identical, and the measured luminance (Figure 2), are increased in efficiency by 40 % at different luminances: +45.5 % luminance at 100 cd/m², +40.6 % at 1000 cd/m² and finally +47.4 % at 10000 cd/m². An operating point for display application of 1000 cd/m² is obtained for device B1 at 4.2 V with a current efficiency of 8.6 cd/A for (0.35; 0.38) CIE coordinates. The maximum measured luminance of 27000 cd/m² is obtained for device B1 at 7 V for a current efficiency of 6.7 cd/A and (0.32; 0.33) CIE coordinates. The color point tends however to blue shift at higher luminance for this OLED stack. In conclusion, the optimization of WO3/Ag/WO3 cathodes for white top-emitting OLEDs was studied. Particular attention was paid to electron injection via this cathode, through the use of an n-doped EIL, for acceptable voltage addressing for display applications. Our predictive calculations and experimental results showed roughly 40% increase in luminance and current efficiency. We found that the WAW cathode was totally compatible with ALD process used for OLED encapsulation. Finally, lifetime tests demonstrated a similar performance for luminance decay as for control device and a diminishing of the voltage roll-off, potentially increasing the lifetime of the device.

Related Publications :
[1] K. Bouzid, T. Maindron, H. Kanaan and E. Viasnoff, Appl. Phys. Lett., submitted

Comparison between ALD-deposited Al2O3 and PVD-deposited SiOx films deposited onto green-emitting OLED as thin film barriers

T. Maindron, B. Freiburger*, T. Jullien* (*LETI/DTSI)

ABSTRACT: OLED devices encapsulated by mean of Al2O3 ALD and SiO PVD barrier films have been stored on a long term basis in laboratory conditions (21 °C/50% RH). This method allows a direct comparison, onto a functional device, of defect occurrence in the barrier films. Combination of both films have been also studied showing that Al2O3 must be passivated by the moisture-stable SiO.

The Holy Grail for encapsulation of fragile organic optoelectronic devices (OLED, OPV, OTFT) consists in the addition of vacuum deposited thin mineral barrier like oxides, nitrides or oxinitrides layers directly onto the organic circuit. This technology is so called today Thin-Film Encapsulation (TFE). The technology basics is somehow similar to the one encountered in the world of food packaging where Al, Al_xO_y or SiO_x barrier materials are vacuum-deposited onto plastic sheet surfaces as barrier layers against moisture and oxygen. The main challenge today for organic optoelectronics is to achieve TFE with Ultra High Barrier (UHB) grade in order to allow a robust encapsulation with Water Vapour Transmission Rate (WVTR) ~ 10^{-6} g/m²/day necessary for OLED devices. Such achievements will open the way to the realization of lightweight, flexible OLED based displays.
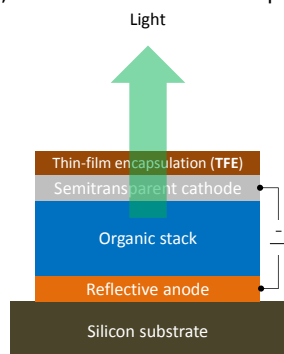

Figure 1: (left) schematic of OLED architecture developed in this work; (right) OLED emitting surface under forward bias at different storage times (21 °C/50% RH)

The ALD technology is highly suitable for making thin film barriers because it allows the deposition of pinhole-free and highly conformal, reproducible, oxide films at temperatures that are compatible with the limiting low transition temperature (100 °C typically) of organic semiconductors that compose the devices. In particular, a couple of publications have demonstrated the capability of Al2O3 ALD films to reach this severe level of WVTR requirement as well as their applicability to encapsulate OLED [E.M. Langereis & al, Appl. Phys. Lett. 89, 081915 (2006); J. Meyer, & al Appl. Phys. Lett. 94, 233305 (2009)]. While being very good barriers against moisture at initial time (fresh films), these Al2O3 films suffer however from moisture ingress, especially when they are exposed to high humidity content during storage tests. It is thus mandatory to shield Al2O3 films from moisture with additional moisture-stable passivation layers. In a recent paper, we have proposed to passivate Al2O3 ALD films by mean of an ebeam-deposited SiO2 layer [1]. Results have confirmed that the use of a SiO2 layer deposited on top of the Al2O3 barrier layer decreases drastically the level of defects into the raw Al2O3 layer (about 6 times less defect). In the meantime, we found out in the literature that SiO films should be better environmental barriers compared to SiO2 [2].

We therefore started to replace SiO2 films by thermally-sublimated SiO ones in our studies. Al2O3 films (20 nm) and SiO films (25 nm) single barriers have been deposited onto green-emitting OLED architectures made onto silicon wafers. Alternatively, hybrid barrier of the kind Al2O3/SiO or SiO/Al2O3 have been also deposited onto OLED (Fig 1). These OLED have been stored for a long period of time, up to >2000 h in laboratory conditions (21 °C/50% RH). Defects in the different barrier layers have been then easily observed as non-fluorescent dark spots that appear onto the OLED surface under a forward bias (Fig. 2).
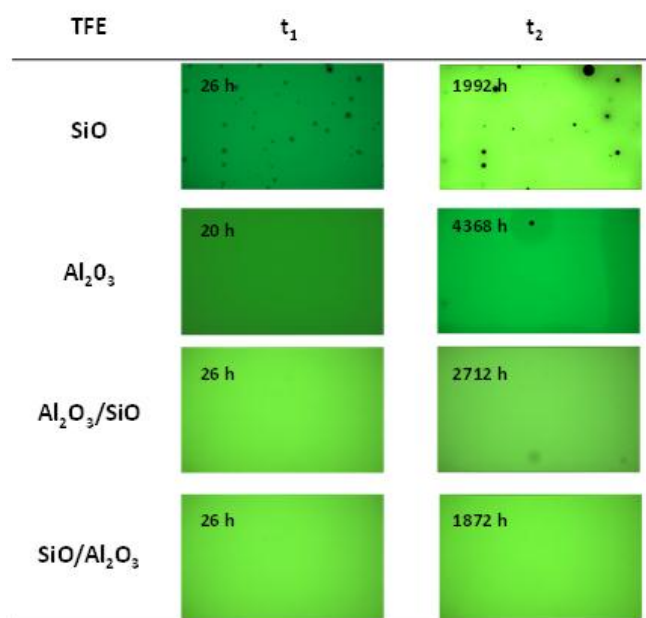

Figure 2: (left) Current density (full lines) and luminance (dashed lines) versus voltage for devices A and B - (inset) Photography of devices A and B at 4V and 5V; (right) Current efficiency versus luminance - (inset) spectra of devices A and B at 1000 cd/m²

This experiment allowed us to compare the behavior of the two different oxides Al2O3 and SiO, made by ALD and PVD deposition, respectively. It turns out that PVD-deposited SiO films show expected pinholes at initial time leading to instantaneous appearance of dark spot defects. On the contrary, ALD-deposited Al2O3 barrier films show very homogeneous emitting surface without any dark spot defects. On a long-term basis, Al2O3 films tend to degrade leading to the occurrence of dark spots. On the contrary, SiO films do not show noticeable evolution so that no new dark spot defects occur. A combination of both barrier layers is therefore a good alternative to ensure a high barrier level for the fragile organic device kept in laboratory atmosphere at 21°C/50% RH.

High-Brightness GaN LED Arrays for a new breakthrough Emissive microdisplay technology

Research topics: display, GaN, high-brightness, wearable

F. Templier, J.-M. Bethoux, F. Marion

ABSTRACT: We have developed high-brightness GaN LED arrays hybridized on Silicon interconnect at a pixel pitch of 10 μm. The GaN LED arrays has been developed and hybridized on silicon interconnect using the microtube technology. The devices provide high optical power and brightness over 1 x 10^7 Cd/m². This approach is a breakthrough in emissive microdisplay technology and is suitable for a wide range of applications from wearable devices (smart-glasses), to Head-Up Displays and compact projectors.

The growing interest for wearable devices has highlighted the need for high-performance microdisplays. Such displays are currently use liquid-crystal displays (reflective or transmissive), organic LEDs (OLEDs), MEMS-based devices like micro-mirror arrays (digital light processing) or laser-beam steering (LBS). Emissive microdisplays such as OLEDs are particularly attractive for these applications. However, for some applications such as see-through glasses, or head-up displays, a brightness of 5000 Cd/m² or more is needed, which exceeds the possibilities of OLED microdisplays. A new type of emissive display, using GaN, was proposed to provide a drastic improvement of the brightness while maintaining excellent contrast and compactness [J. Day & al Appl. Phys. Lett., 99, p031116 (2011)].

This year, we have developed very high-brightness, GaN-based LED array hybridized on a Silicon interconnect with a pixel pitch as small as 10 μm. To achieve this, a 10 μm-pitch LED array has been developed, and was hybridized on silicon interconnect using the microtube technology.
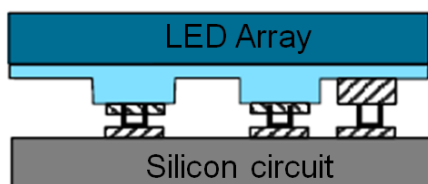

Figure 1 : Structure of hybridized LED arrays.

GaN LED array are made on sapphire substrates. Base wafers consist of 2-in. diameter sapphire with 440 nm LED Multi Quantum Well (MQW) InGaN/GaN epitaxial structure grown by metal-organic chemical vapor deposition (MOCVD). GaN array process has been developed to achieve 10 μm pixel-pitch. Finished GaN wafers have a series of LED-arrays having each 300 x 252 pixels at 10-μm pitch. A particular difficulty for hybridizing GaN LED array and CMOS active-matrix is that it should be performed at low temperature, due to the mismatch of substrate coefficient of thermal expansion (Sapphire vs. Silicon). In the meantime, a small pixel-pitch is desired for microdisplay application, namely 10 μm and less. Classical hybridization technique such as bump flip-chip technology is not compatible with pixel-pitch of 10 μm or less. In the recent years, LETI has developed the so-called microtube technology which combines low-temperature processing (→ compatible with heterogeneous substrates) [1] and pixel-pitch of 10 μm and less. Therefore this technique appears to be very suitable for LED microdisplay application, and it has been chosen for this work.

The principle of this technique is to grow microtubes on the pads of the CMOS, and align/couple the CMOS with the GaN array, the microtubes being then inserted in the GaN arrays pads (figure 1).

Hybridized GaN arrays have been tested electrically and optically. Figure 2 shows addressing of one 6.5 x 6.5 μm pixel from a hybridized 10μm-pitch array.

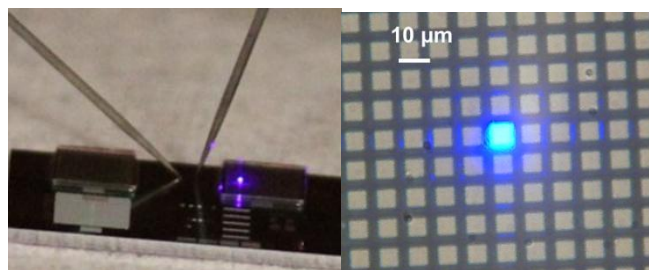Figure 2 : Addressing of a 6.5 μm microLED on hybridized matrix.

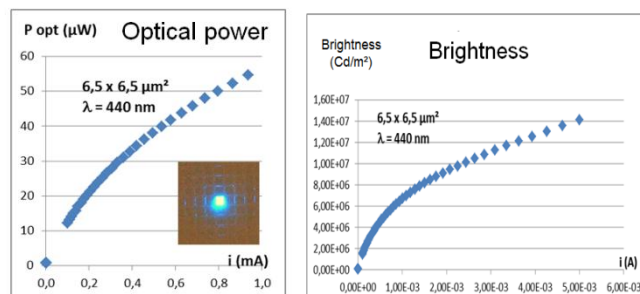Figure 3: Optical power (left) and brightness (right) of the microLEDs.

Figure 3 shows optical power and brightness as a function of driving current. It is evidenced that a brightness of more than 10^7 Cd/m² is obtained from the hybridized LED array. This outstanding luminance level is several orders of magnitude higher than those of OLED or other types of microdisplays.

The demonstrated 10 μm pitch [2] is the smallest pixel-pitch ever published for GaN LED arrays. An outstanding brightness of more than 1 x 10^7 Cd/m² is achieved on these hybridized GaN LED arrays. These results show that the developed technology is very promising for the fabrication of high resolution, small pixel-pitch, high-brightness and reliable GaN-based emissive microdisplays. A very wide field of applications can be targeted: HMD systems (including see-through glasses which represent a huge potential market), compact projectors, and compact Head-up displays.
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Related Publications:
[1] F. Marion et al., "Aluminum to Aluminum Bonding at Room Temperature", Proceedings of the 63th Electronic Components and Technology Conference, Las Vegas 2013, pp146-153 (2013)
[2] F. Templier, H. Bono, J.-M. Bethoux, F. Marion, I.-C. Robin, M.-A. di Forte-Poisson, « High-Brightness GaN LED Arrays Hybridized on Silicon Interconnect at a Pixel Pitch of 10 μm", Invited Talk, The 21st International Display Workshops in conjunction with Asia Display 2014 (IDW/AD'14), December 3-5 2014, Niigata, Japan (2014)

Holographic Display for Extended Informative Windshield

Research topics: Head Mounted Display, Holography, Augmented Reality

C. Martinez, U. Rossini, D. Sarrasin

ABSTRACT: We present the development of a windshield display system based on the use of a Head Mounted Projection Display (HMPD) and a transparent holographic screen designed to allow a light efficiency optimized visual rendering.

During their mission, aircraft pilots must remain concentrated on their trajectory by a constant warning of the scene while managing information flows coming from the aircraft sensors. In response to these needs, ergonomic improvements on information displays has been studied since the 1960s and Head Mounted Display (HMD) and Head Up Display (HUD) have been developed. In these devices, the composition of the display, the optical system and the combiner used to generate the virtual image severely limit the system performances. The field of view and the eye position limits (eye box) are especially driven by the pupil of the optical system. To deal with these constraints, sophisticated optical designs must be elaborated that increase the weight or the cost of the devices and limit its application to very specific aircraft military applications.

Recent progress in the field of Information and Communication Technologies has led to an increase of the information flow towards general users, so that HMD and HUD are now also being studied in a broad range of applications. Aware of the growing interest in these display activities, Optsys a French company specialized in vision equipment for armored vehicles has contacted CEA Leti in order to develop a smart windshield concept. We have proposed an alternative visualization solution based on a Head Mounted Projection Display (HMPD) concept.
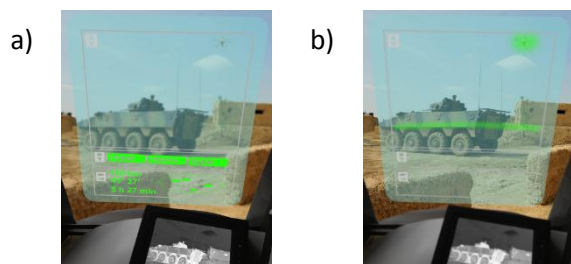

Figure 1 : .Examples of projection zones applications: a) interactive dashboard (head looking downward); b) AR functionality (head looking forward and upward)

As compared to HMD, HMPD are bounded to the user head. However the displayed data are not seen as a floating virtual image but as a real image projected on a screen. The implementation of HMPD technologies in a vehicle windshield requires a projection screen. We present in this paper a see-through HMPD system, based on a holographic display develop in collaboration with Hologram Industries Research a German company specialized in hologram design. It allows both Augmented Reality and interactive dashboard functionalities through an extended informative windshield (fig. 1).
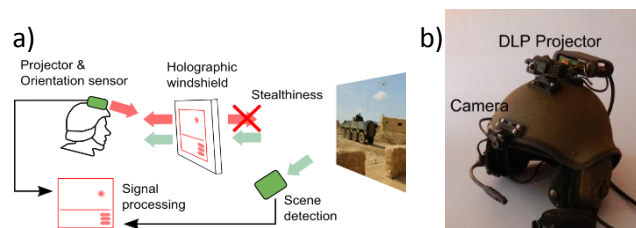

Figure 2: a) diagram of the HMPD system; b) photography of the helmet with projector and camera.

Figure 2a shows schematically the system specification with a projector and an orientation/gesture sensor mounted on the user helmet. The holographic film reflects the projected information towards the viewer in a diffuse way without disturbing the windshield transparency. Figure 2b shows the HMPD developed in CEA Leti with a DLP projector and a compact camera.

Transparent projection screen is a challenging development as the device must enable mixing of both transparency and diffusion. Holographic or particles films exist but suffer from low visual efficiency that preclude projection in ambient light [Chia Wei Hsu & al, Nat. Commun. 5 (2014)]. To overcome this problem our hologram is designed to optimize the diffused signal coming from a source point M1 into a given eye box located at point M2 (figure 3a).

Figure 3b shows the visual result of a projected checkerboard on the holographic display implemented in the windshield, as seen with the helmet camera. A uniform and bright image can be seen over the outer scenery. In usual viewing condition, measured brightness is 210 Cd/m² for the 30 Lum DLP green LED lighting.

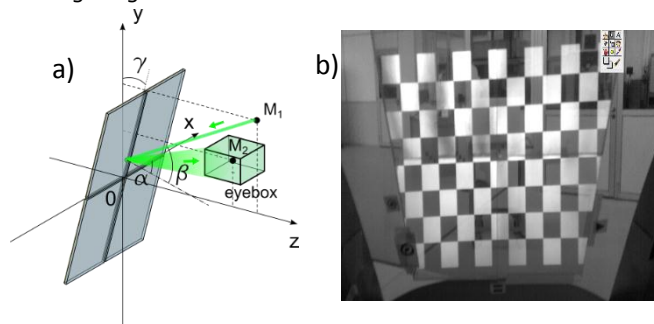*Figure 3 : a) Holographic display specification (a) end visual rendering (b)*

Research now focuses on the increase of the screen brightness for more enhanced external glaring light conditions and on the design of polychromatic display solutions.

7

Optics and nanophotonics

Topological insulator structures

Plasmonic free space optical filters

Copper-dielectric multilayer optical filters

Optics and Photonics

MBE growth and interfaces characterizations of strained HgTe/CdTe topological insulators

C. Thomas, X. Baudry, J.P. Barnes, M. Veillerot, P.H. Jouneau*, S. Pouget*, T. Meunier*, O. Crauste**, L.P. Lévy** and P. Ballet   (* CEA/ INAC, **CNRS Inst. Neel, F-Grenoble,)

ABSTRACT: Topological insulator materials like HgTe exhibit unique electronic properties at their interfaces and so, peculiar attention has to be paid concerning the growth optimization. Molecular beam epitaxy of tensile-strained HgTe/CdTe is investigated as a function of the growth temperature. Crystal quality is checked by using high resolution X-rays diffraction. By combining several material characterization techniques such as scanning transmission electronic microscopy, time-of-flight secondary ion mass spectroscopy and X-rays reflectivity, we report sharp interface morphology with nanometer-scale Hg/Cd diffusion lengths

Topological insulators (TIs) are of main interest in condensed matter research thanks to their unique electronic and spin properties that arise on their interfaces. TIs gather the graphene-like transport properties with Dirac fermions and the topological protection that prevent backscattering phenomena. These interfaces exhibit spin-momentum locking which polarizes the spin perpendicular to the momentum. Control of the spin and coherent spin transport are then easily achievable in TIs [C Brüne, & al Nat. Phys. 8 (2012).] making them very attractive for spintronic applications [V. Krueckl, K. Richter, Phys. Rev. Lett. 107 (2011)].

HgTe layers are grown by MBE on either (100) or (211)B CdTe substrates. Growth rate of 1 monolayer/s and a Hg/Te ratio in excess of 1000/1 were used. After thermal desorption of the substrate surface oxide, growth process starts with the deposition of a 200 nm-thick CdTe buffer layer with excess cadmium. The substrate is then cooled down to the growth temperature for strained HgTe layer. At the end of the growth process, a cooling down under Hg flux is performed allowing to improve roughness values lower than one nanometer [2]. High crystal quality HgTe layers have been successfully grown at temperatures up to 185°C as shown in high resolution X-rays diffraction (HRXRD) spectra of Fig. 1 where CdTe and HgTe peaks are well-defined and surrounded by Pendellösung fringes.
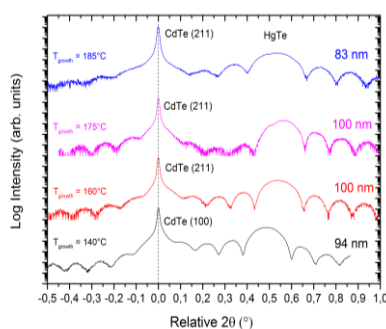

Figure 1 : HRXRD of HgTe grown on either (211)B or (100) CdTe susbtrates for different growth temperatures ranging from 140°C to 185°C.

We study the interdiffusion at the HgTe/CdTe interface for a sample of HgTe (83 nm)/CdTe (211)B grown at 185°C to check values for interdiffusion for the largest growth temperature. Three characterizations techniques are used: STEM, SIMS and XRR. Due to the resolution issue of TOF-SIMS, X-rays Reflectivity is used to obtain a more accurate estimation of the interdiffusion between HgTe and CdTe layers. Fig.2 illustrates the reflectivity curve of HgTe (83 nm)/CdTe which was grown at 185°C, as a function of grazing angle.
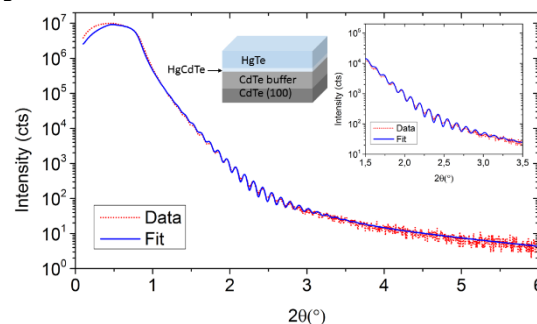

Figure 2 : XRR spectra of HgTe (83 nm)/CdTe. The model structure used for the fit includes a HgCdTe intermixed layer and is represented is the inset as well as the spectral range of main importance for the fit of the XRR spectra.

Best fitting parameters to the XRR data are obtained for a HgTe layer of thickness 79.7nm and roughness of 1.6nm. This latter value is in perfect agreement with atomic force microscopy measurement where top surface root mean square roughness was determined to a value of 1.7nm. Concerning the intermixing layer, the best fit is obtained for 3nm of $Hg_{0.5}Cd_{0.5}Te$ with a roughness of 0.8 nm. The diffusion length can then be estimated to 3.4+/-0.4nm for this structure. This value is consistent with the extrapolation of Tardot et al. [2] for growth at 180°C and has to be considered as a maximum value for interdiffusion in our structures.

In conclusion, high crystal quality HgTe/CdTe TI structures have been grown with surface roughness of 1.6nm and interfaces defined to within 3nm for the largest growth temperature used. In the case of HgTe capped layer grown at 160°C, sharp interfaces of about 1nm for the bottom interface and lower than 0.5nm for the top interface are evidenced.

Related Publications :
 [1] P Ballet, C Thomas, X Baudry, C Bouvier, O Crauste, T Meunier, G Badano, M Veillerot, J.P Barnes, P.H Jouneau, L.P Lévy, J. Electron. Mater. 43 (2014) 2955–2962.
[2] A Tardot, A Hamoudi, N Magnea, P Gentile, J.L Pautrat, J. Appl. Phys. 62 (1993) 2548.

Optics and Photonics

Angular and polarization properties of cross-holes nanostructured metallic filters

Research topics: Plasmonics, Image sensors, Surface plasmons, Nanostructures

R. Girard-Desprolet, S. Boutami, S. Lhostis* and G. Vitrant**
(*STMicroelectronics Crolles, **IMEP-LAHC)

ABSTRACT: The optical properties of cross-shaped-hole array plasmonic filters have been investigated to provide accurate design rules leading to a high angular stability and to a low sensitivity to polarization. In particular, we demonstrate that a low intercrosses distance and a low shape factor of the crosses lead to a regime where localized plasmon resonances are predominant and ensure these stability properties that make such structures appealing for wide-angle and low-color error light sensors.

Plasmonics has shown a high potential to perform optical filters. Unlike conventional organic resists, plasmonic filters do not require an external IR-cut filter (sensor's thickness reduction) and are not degraded by thermal treatments. The most widespread structures consist of hole-arrays in a metallic layer. Most of the hole designs however show a particular sensitivity to polarization and to the azimuth angle when the incidence angle θ is increased. For image sensors, such sensitivities would lead to drastic disparities in pixels sensitivity over a matrix and to distortion in color rendering. In this work we address a complete review on cross-shaped holes designs [1] and materials composition and we identify specific ranges of cross dimensions, shape factors and period array to get conditions of spectral response stability in terms of polarization and azimuth angle φ, which has never been shown so far. We have determined particular structures that would allow for the realization of image sensors and displays with extremely low color errors whatever the orientation and the polarization of the incident light.
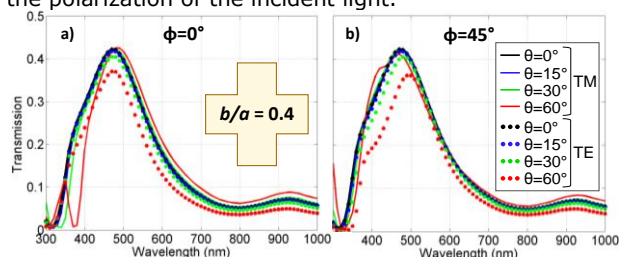

Figure 1: Spectral responses of the same filter (d=30nm, b/a=0.4) for different incidences θ, azimuths φ and under TM and TE polarizations.

Our studied structures consist of an Al layer embedded in infinite SiO2 and patterned with a square array of cruciform apertures filled with SiO2. RCWA calculations have demonstrated that the two most-impacting parameters are the intercrosses distance d and the ratio of the arm width b to the arm length a of the crosses (shape factor = b/a). We show that a ratio b/a < 0.5 and a low intercrosses distance (d < 75 nm) make the filters have a high angular stability up to 60° of incidence and a strong insensitivity to the polarization and to the azimuth of the incident light, without resonance shifts and transmission losses up to θ = 30° (Fig.1).

We attribute these properties to the competition between propagating surface modes (the surface plasmon polaritons or SPPs), and localized plasmon resonances (LSPs). While SPPs are by nature strongly dependent on the incidence conditions of the light, LSPs are characterized by a strong confinement of the electromagnetic field occurring around the apertures and are more related to the shapes and dimensions of the holes. LSPs are thereby much less impacted by the polarization state or the incidence of light.

A low d creates an important discontinuity of the metal layer and a low b/a (i.e. thin crosses) ensures a stronger

confinement of the field inside the holes (Fig. 2). These two conditions thus favor a regime where LSPs are predominant in the optical transmission mechanism, leading to a stable spectral response of the filter.
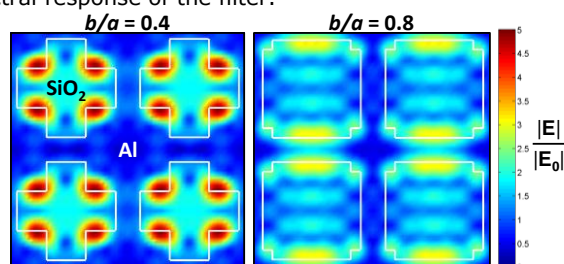

Figure 2: Electric field intensity on top of Al layer for two hole-array filters with d=30nm and b/a=0.4 or 0.8.

We apply these geometrical conditions to a set of RGB filters, and we calculate for each color filter the CIE coordinates of the spectral responses simulated for all the combinations of the following incidence conditions: TM and TE polarizations, incidences θ∈[0°,30°] and azimuths φ∈[0°,45°]. We propose in Fig. 3 the CIE diagram containing all the corresponding simulated filters. It can be seen that with the studied geometrical criteria, the color errors are extremely low even for large angles of incidence, which is an essential property for image sensors.
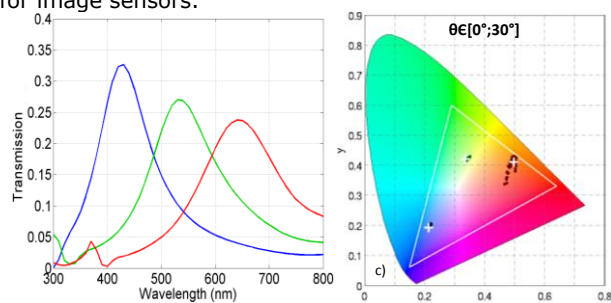

Figure 3: Color variations of a RGB filters set designed with b/a<0.5 and d=75nm under various illuminations conditions with θ ∈[0°,30°].

We thus provide in this work specific design rules demonstrating the high potential of cross-shaped-hole arrays to provide highly stable filters that can be used for wide angle light sensors [2], or for low color-error image sensors or displays with wide-angle and uniform response on each pixel on the matrix, regardless of the polarization and incidence of light. Further works have been lead to evaluate the viability of such structures with respect to process dispersions in view of an industrial wafer-level production [2].

Related Publications:
[1] S. Landis, P. Brianceau, N. Chaix, Y. Desieres, V. Reboud, and M. Argoud, "Metallic colour filtering arrays manufactured by NanoImprint Lithography," Microelectron. Eng. 111, 193–198 (2013).
[2] R. Girard-Desprolet S. Lhostis, C. Beylier, V. Farys, G. Vitrant, S. Boutami, "Impact of process factors on the performance of hole-array metallic filters," Applied Physics A 117(2), 485-490 (2014).

On-chip copper-dielectric interference filters for manufacturing of ambient light and proximity CMOS sensors

Research topics: Thin film multilayers, spectral filtering

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ABSTRACT: Filter technologies implemented on CMOS image sensors for spectrally selective applications often use a combination of on-chip organic resists and an external substrate with multilayer dielectric coatings. The photopic-like and near infrared band-pass filtering functions respectively required by ambient light sensing and user proximity detection through time-of-flight can be fully integrated on chip with multilayer metal-dielectric filters. Copper, silicon nitride and silicon oxide are the materials selected for a technological proof-of-concept on functional wafers, due to their immediate availability in front-end semiconductor fabs. Filter optical designs are optimized with respect to specific performance criteria, and the robustness of designs regarding process errors are evaluated for industrialization purposes.

Due to their sensitivity in the visible and near infrared (NIR) ranges, CMOS image sensors can be used for different applications than traditional RGB color imaging. The green channel can simply provide ambient light sensing (ALS) signals for monitoring ambient light and adjusting the brightness or the contrast of a display. Green filtering is usually realized with an organic on-chip resist but an additional interference filter with many layers is required on an external substrate to block NIR light otherwise transmitted by the resist. Time-resolved applications such as time-of-flight (TOF) for user proximity detection can also be addressed with the NIR signal provided by a CMOS Single Photon Avalanche Diode (SPAD). A highly selective NIR band-pass interference filter on external substrate, including many dielectric layers, is usually used together with a black resist on-chip to enhance the rejection.

When both ALS and NIR functions are to be implemented side by side on small pixels, a new filtering solution has to be identified, since the transmittances of the two filters on glass are incompatible. We focus here on copper-dielectric thin film multilayers which can provide both functions with the required selectivity and can be implemented fully on-chip.
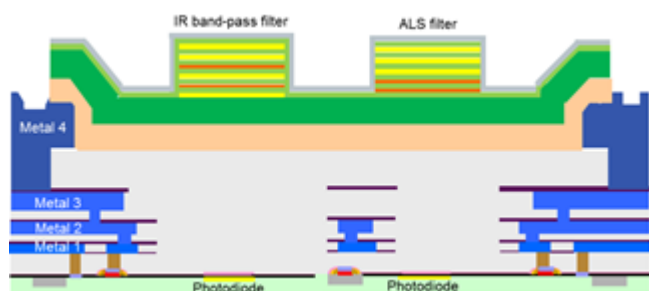

Figure 1: Integration scheme for ALS and NIR filtering on CMOS

We realized a first demonstrator of fully integrated spectral filters on CMOS separate wafers with these materials commonly used in foundries and standard patterning process. Specific developments were necessary to enhance the adherence of Cu layers over SiN layers without any optically absorbing adherence layer. Although the design was constrained by technological limitations derived from compatibility with CMOS manufacturing and cost considerations, the performances of optimized filters were close to the reference filters.

Quantitative criteria were introduced to optimize the design of ALS and IR band-pass filters in the system also including a black housing in front of the sensor, the quantum efficiency of the CMOS sensor for both filters, and the black resist in the case of the IR band-pass filter. The criteria were derived from system requirements and did not summarize to transmittance targets such as the photopic response. The high rejection of metal/dielectric filters enabled to integrate the ALS function on chip without the NIR cut-off filter on glass. The same technology was found to be particularly well suited for the NIR band-pass filtering required in TOF applications, with both high transmission and high rejection. To our knowledge, thin film multilayers have no competing solution for on chip integration in the NIR range.
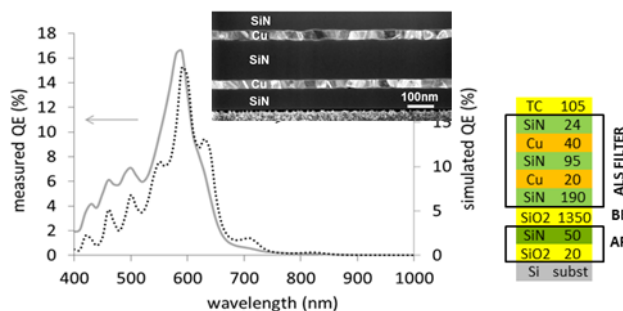

Figure 2: QE spectral response of ALS filter (simulations did not take into account the losses induced by the absence of micro-lenses), SEM cross section and filter design.

The manufacturability of this multilayer thin film technology was investigated in terms of robustness to process errors. The input thickness and refractive index were chosen within a range of ±3sigma typically considered in statistical process control. All the layers down to the Si were taken into account in the robustness evaluation. ALS filter designs were found to be robust enough with process errors typically observed in fab, provided that the dark current is reduced after the final back-end annealing. The bottleneck of the technology was the robustness to process errors for narrow IR band-pass designs. However, significant improvement may be achievable with a reduction of process errors in the deposition of only two dielectric layers in the filters.

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PhD degrees awarded in 2014

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Development of tools and methods for OLED stack design, towards predictive modeling

The work presented here revolves around electrical and optical optimization of OLEDs (Organic Light Emitting Device) through the development of simulation methods and tools. The electrical modeling of OLED is a complex field, belonging to R&D. At the beginning of this work, no state of the art OLED electrical simulation has been presented yet. The development of simulation, based on experimental data, would contribute to the establishment of predictive simulation, allowing a better understanding and faster R&D cycles. Firstly, an extraction method for organic semiconductors' transport parameters has been developed by fit procedure (reconstitution of experimental results with simulation). The extracted values, compared between the two mobility models, were used to compile a database. These sets allowed the realization of the simulation at various temperatures of the electrical behavior of a complete OLED stack. The careful analysis of the simulated intrinsic profiles gave an insight on charge accumulation at the recombination interface, harmful for the lifetime performance of the device. Secondly, we proposed to solve the problem with a bipolar blend to enlarge the recombination profile. After optimization of the blend inside the OLED, an increase of the lifetime of ca. +30% has been highlighted, as well as the stabilization of the color point dependency to voltage. To further understand the mechanisms related to the insertion of this layer, TOF-SIMS characterization of organic layers was studied. Very promising early results allowed the profiling of a full OLED stack, and determination of each layer. A second wave of results, bound to Ar beam analysis, demonstrated the possibility to detect undamaged molecule signatures, giving access to far more degradation related information than before. Finally, an alternative cathode made of $WO_3/Ag/WO_3$ (WAW) has been optimized for white OLED microdisplays to enhance the light outcoupling coefficient. The fabrication of the devices demonstrated a +40% increase in luminance and current efficiency, in perfect agreement with simulation. The transfer of the process onto an industrial class deposition cluster tool resulted in the fabrication of OLEDs with WAW cathodes demonstrating a +75% increase of the lifetime at half luminance.

Bertrand CHAMBION
University of Bordeaux

Reliability investigation of high power white LEDs multichip modules for automotive applications

With rapid development of Lighting Emitting Diode (LED) market, LED performances are now suitable for automotive high beam / low beam lighting applications. Due to the need of Ultra High Brightness (UHB-LEDs), LEDs are packaged on high thermal conductivity materials to obtain multichip module (4 chips in series), which deliver up to 1000 lumens at 1A. Currently, several LED technologies are commercially offered for the same performances, and different packaging strategies have been implemented in terms of chip configuration, bonding, down conversion phosphor layer and mechanical protection to optimize performances. This study addresses a dedicated methodology for reliability analysis, applied on two LED chip packaging technologies: On the one hand, a Vertical Thin Film (VTF) technology; on the other hand a Thin Film Flip Chip (TFFC). Our methodology is based on 3 main items:

- Packaging technology structure, materials analysis and electro-optical and thermal multichip models for both technologies to understand and extract the key parameters to monitor during ageing tests.
- Robustness assessment tests to define operating margins, adjust accelerated life-testing conditions, and identify failures signatures.
- Reliability study through a 6 000 hours High Temperature Operating Life (HTOL) accelerated tests, to predict the Mean Time To Failure (MTTF) of these new light source technologies regarding the automotive mission profile. Linked to failure analysis, convincing failure mechanisms are proposed.

Based on these results, parametric variations are compared to failure analysis results to propose failure mechanisms. The HTOL tests reveal that both LED technologies have their specific reliability behavior and failure modes: catastrophic failure and gradual failure. Predictive lifetime estimations (L70B50) of these multichip modules give a factor 6 between both technologies.

Beyond these reliability results, the multichip architecture brings new issues for Solid State Lighting (SSL) sources in automotive, as well as partial failure or unbalanced behavior after stress. These new issues are discussed through the behavior modeling of a 10 LED modules batch for both failure modes. Modeling results demonstrate that the predictive lifetime of a LED multichip architecture is directly related with the LED technology failure mode.

Antoine DESCOS
University: Ecole Central of Lyon

Hybrid III-V on Silicon Lasers and Devices

With the development of the Internet and the new cloud services, the amount of data processed by data-centers is increasing. Though, if the paralleling of multiple server answer to this growing quantity, a structural problem arises. As in super calculators between nodes calculations, data are not transmitted quickly enough between servers on classical electric cables. This bottleneck can be overcome thanks to the optic which can access greater data rates. If existing active cables allow a quick resolution, silicon photonic has a clear benefit. The integration of the optical components closer to the electronic chips reduces substantially the path of interconnections and their energetic costs.

An optical transmitter and receptor need different components. If modulators, multiplexers, fiber coupler, multiplexer and photo-detectors are already achieved, laser sources used are still outside the photonic chip. This is the missing link for a complete optical integration thanks to the silicon photonic. Several architectures have been proposed but this thesis relies on hybrid integration of III-V material on silicon.

The work of this thesis consisted on the conception, the fabrication and the characterization of hybrid III-V on Silicon laser sources and was completely done at the CEA/LETI. The LETI architecture composed by a III-V waveguide coupled to a silicon waveguide was improved thanks to a adiabatic criterion to obtain an efficient and robust active area of the laser. This architecture was declined in different kinds of lasers (Fabry-Pérot, DBR, Racetrack and DFB). The fabrication required technological development for the structuration of the reported III-V material on silicon at the laboratories of the CEA/LETI.

The first results validates the proposed architectures. The DBR lasers have threshold of less than 20mA and maximal optical power of more than 20mW inside the silicon waveguide. Those lasers are monomode with a SMSR of more than 50dB. The DFB Lasers have threshold of 30mA and maximal optical power of more than 40mW inside the silicon waveguide. They are monomode with SMSR more than 40dB. Those results are world state-of-the-art for hybrids laser sources in silicon photonic
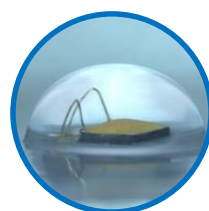
Benoit HAMON
University: Institut National Polytechnique of Grenoble

LED reliability, mechanisms and modelling

In the past years, white light emitting diodes (LEDs) have faced an increase of their performances combined with a decrease of their cost. In the present situation, LEDs are considered to be the light source of the future. As well as their low energy consumption, their long lifetime is one argument for a massive adoption of this technology. However, due to their long lifetime and the multitude of existing failure mechanisms (at die and package levels), the study of their reliability still remains challenging. This thesis proposes a wild range study of LED reliability, from early life failures to end of life failures. First, a new qualification test has been implemented in production to characterize and detect early failures of LED. Second, the cross study of electrical and optical variations during accelerated lifetime has been conducted. Results allowed modeling those variations and using this model for more precise lifetime estimations. Finally, failure analyses of aged samples have been conducted highlighting the failures mechanisms responsible for the measured degradations.

The obtain results allow a better understanding of LED reliability through the modeling of their behavior during time and the analysis of the most critical failure mechanisms. Because lighting device reliability is a key factor, these results are useful for the LED industry.

Wala HASSIS
University of Grenoble

Study of advanced structures for high operating temperature quantum IR detection

The detection principle of cooled detectors is based on photovoltaic conversion. However, small gaps involved in IR detection require the association of the detectors to a cryogenic system to reduce the dark current and the 1/f noise. The measurement of dark current shows that this one, limited by the diffusion, increases considerably with the warming of the detector and thus makes it impossible to use at higher temperatures. Several pioneers in the field have focused on the study and understanding of the different mechanisms of 1/f noise in different ranges of temperature but the origin of this noise is not yet clear in the case of photo-detectors.

The different behavior of noise observed in the literature led us during this thesis to conduct a major measurement campaign on different variants of structures: implanted photodiodes characterized by mature technology and nBn structures or bariodes that are still in the experimental stage. Various configurations of photodiodes have been investigated in order to correlate the noise with the tested parameters. The nBn being less mature structures were in this thesis characterized in terms of dark current and unfortunately did not have allowed further in terms of 1/f noise study. Indeed, the noise study investigated in this thesis has focused on MCT photodiodes.

Trends observed in the low frequency noise in the different detection structures has as main goal of restricting the search field to isolate the different mechanisms of 1/f noise and determine the key parameters to be considered in structural design of high temperature detection structures.

Wiyao KPOBIE
University: Institut National Polytechnique de Lorraine

3D modeling of flip chip assemblies for the reliability of high value electronic components of the "More than Moore" group

Flip chip technology is increasingly prevalent in electronics assembly [threedimensional (3D) system in package] and is mainly used at fine pitch for manufacture of megapixel large focalplane detector arrays. To estimate the reliability of these assemblies, numerical simulations based on finite-element methods appear to be the cheapest approach. However, very large assemblies contain more than one million solder bumps, and the optimization process of such structures through numerical simulations turns out to be a very time-consuming task.

In many applications, the interconnection layer of such flip chip assemblies consists of solder bumps embedded in epoxy filler. For such configurations, we propose an alternative approach, which consists in replacing this heterogeneous interconnection layer by a homogeneous equivalent material (HEM). A micromechanical model for the estimation of its equivalent thermoelastic properties has been developed. The constitutive law of the HEM obtained was then implemented in finite-element software (Abaqus®). Elastic properties of materials that compose the assembly were found in literature and by using mechanical characterization method especially nano-indentation. Thermomechanical responses of tested assemblies submitted to loads corresponding to manufacturing conditions have been analyzed. The homogenization-localization process allowed estimation of the mean values of stresses and strains in each phase of the interconnection layer. To access more precisely to the stress and strain fields in these phases, two models of structural zoom (model coupling and submodeling), taking into account the real solder bump geometry, have been tested. The local stress and strain fields obtained corroborate the experimentally damage initiation of the solder bumps observed.

Clément LOBRE
University: Institut National Polytechnique of Grenoble

Arsenic doping of HgCdTe by Ion Implantation

This thesis addresses the incorporation of arsenic in HgCdTe but also its activation and the related diffusion during high temperature annealing. For each item, a large panel of characterization tools was used in order to obtain a better understanding of p-type doping of HgCdTe by arsenic implantation.

Irradiation induced annealing during ion implantation has been demonstrated with a saturation fluence of about 2.10^{14} at.cm-2. A simple model enabled us to evaluate the diffusion coefficient of arsenic and to evidence the major role of mercury in the diffusion process. The solubility limit of arsenic in the HgCdTe alloy was determined for the three most common compositions used for infrared applications. For arsenic concentration over this limit, the formation of arsenic-rich nanocrystals was demonstrated by transmission electron microscopy coupled with nano-scale chemical mapping. This first experimental evidence of arsenic clustering explains why some of the arsenic does not participate in the diffusion process. However, the exact chemical and crystallographic nature of these nanocrystals remains unknown. The measurement of the depth profile of carrier density allows us to demonstrate the electrical inactivity of arsenic-rich nanocrystals. On the other hand, almost 100 % of the mobile arsenic is found to be activated as an acceptor. The formation of AsHg8 complexes was proposed to explain the activation and the diffusivity of arsenic in HgCdTe.

Ion implantation of nitrogen, phosphorus and antimony was studied and its behavior compared to that of arsenic. For nitrogen and phosphorus, a trapping effect that blocks the dopant diffusion was observed. Therefore, a good quality doping cannot be achieved under these conditions. Antimony exhibits a faster diffusion than arsenic and the activation as an acceptor of more than 21 % of mobile antimony was demonstrated. Even if the antimony behavior seems interesting, arsenic exhibits the most promising properties for HgCdTe doping among all studied elements. As well as restoring a good crystal quality, our annealing conditions allow the activation of most of arsenic as an acceptor.

Thi Thu Thuy NGUYEN
University: Institut National Polytechnique of Grenoble

Study of thin film transistors based on Indium Gallium Zinc Oxide for their applications in active matrix flat panel LCD and OLED display

This thesis aims to study thin-film transistors (TFTs) based on Indium Gallium Zinc Oxide (IGZO) in the framework of applications in active matrix flat panel LCD and OLED display. The TFT fabrication process and the characterization of IGZO deposited film are two key studies in this thesis in order to obtain TFT electrical characteristics close to the state-of-the-art. We have also studied the passivation which is identified as crucial for stabilizing the TFT and achieving good performance.

The deposition of the active layer and the fabrication process of TFT are firstly studied. Smooth surface of deposited films is demonstrated by AFM and the absence of the crystalline peak of the material is shown by X-ray diffraction. The density of charge carriers decreases with the increase of oxygen flow rate. The active layer deposited at 200°C and at 4 sccm of oxygen flow has a carrier density in the order of 10^{17} cm-3 which is suitable for TFT operation. This condition is chosen to fabricate IGZO-based TFT in this thesis.

In a second step, we have evaluated the influence of annealing condition on TFTs' electrical characteristics. Annealing in oxygen leads to operational TFTs while doing the same under nitrogen or the absence of annealing suppresses field-effect behavior. Our studies have also shown that annealing temperature of 300°C is suitable to obtain good performance of the transistors. From this study, we have obtained TFTs with high mobility (between 5 and 15 cm2/Vs), high ION/IOFF ratios (about 107), and reasonable sub threshold slope (about 0.3 V/decade). The threshold voltage (VT) however remains low (between -4 and -2 V) and needs to be improved.

Finally, we have investigated the impact of a passivation layer on the performance of IGZO TFTs. SiO2 film (deposited by PECVD) and Al2O3 film (formed by ALD) were studied. We have observed that such passivation can degrade the TFTs rather than protecting them. Concretely, VT shifts in negative direction when increasing the Al2O3 layer thickness or the silane flow during SiO2 deposition. Principal reason for this shift is the presence of hydrogen which is generated during passivation. We have evaluated some solutions to reduce the degradation during deposition and ensure a good protection of the TFTs.

Optics and Photonics

Léopold VIROT
University of Paris Sud

Development of Ge on Si avalanche photodiodes for low signal and high speed detection

To address the issue related to the limitations of metallic interconnects especially in terms of bitrate, Si photonics has become the technology of choice. One of the basic components of photonic circuits is the photodetector: It allows to convert an optical signal into an electrical signal. Photodetectors based on Ge on Si have shown their potential and offer the best alternative to III-V photodetectors, for integration into Si photonic circuits.

In this context, the Ge on Si photodiodes have been studied. The optimization of pin photodiodes enabled the achievement of state of the art results. A new approach using a double lateral Si/Ge/Si heterojunction was proposed to increase the responsivity but also to provide a better integration solution, especially with Si modulators. To further increase the sensitivity of the receivers, the use of avalanche photodiodes, is however necessary. SACM (Separate Absorption Charge Multiplication) structure, combining Si low multiplication noise and Ge absorption at telecom wavelengths was first studied. Models have been developed to optimize the devices, and the photodiodes have been fabricated and characterized. The results obtained on the surface illuminated photodiodes (Gain-bandwidth product of 560GHz only -11V) are very encouraging for waveguide integration. On the other hand, Ge on Si pin photodiodes have been studied in avalanche. The small width of the intrinsic region contributed to the multiplication noise reduction thanks to "dead space" effect, and operation at 10Gbps for a gain of 20 and an optical power of -26dBm at only-7V, without using amplifier (TIA), have been demonstrated. These developments open the way to fast, low power consumption and high sensitivity receivers.

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Optics and Photonics

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