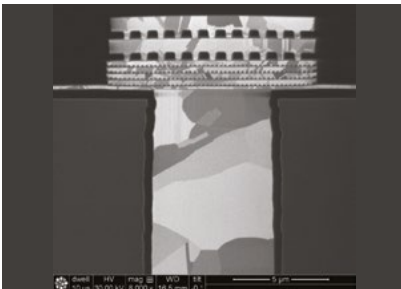
# 3D technology bricks

CEA-Leti offers state-of-the-art technology bricks using 200 & 300mm industrial tools to enable 3D high performance applications: from computing, telecommunication to heterogeneous technologies



## High aspect ratio TSVs

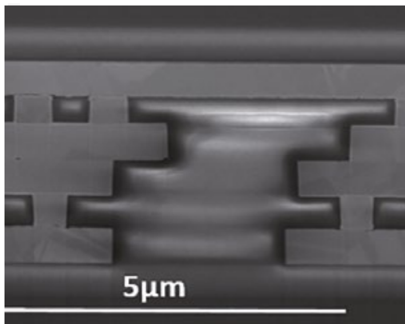
CEA-Leti's offers strong expertise in high aspect ratios TSVs, including:

- via-mid TSVs with a diameter in the range of 10-12µm for a height between 80 and 120µm with excellent electrical performances and filling demonstration
- new gen. of high density TSVs with diameter 1-2µm as well as high aspect ratio TSV last (AR>5)

## Fine pitch copper pillars & assembly

Fine pitch interconnection is key to support 3D silicon stacking roadmaps. CEA-Leti offers:

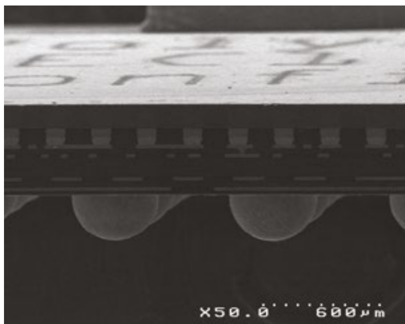
- 20µm diameter (40µm pitch) µbumps and µpillars, including R&D to stabilize lower diameter interconnection process
- strong knowledge in thermocompression die-to-wafer stacking and related underfill technologies, including fine pitch interconnection




## Fine pitch and beyond hybrid bonding

From design to fabrication and electrical characterization, CEA-Leti offers various hybrid bonding solutions using full 300&200mm fabrication lines including Known Good Dies:

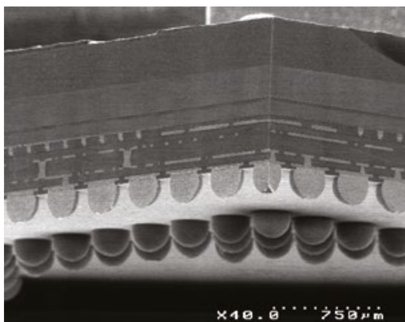
- wafer-to-wafer and die-to-wafer bonding technologies
- multi-layer hybrid bonding techniques with fine connection pitches (<1µm) to support various technologies with high bandwidth
- emerging bonding techniques and modules for next gen. of ultra-fine die alignment (<200nm)



## Temporary bonding & wafer-level planarization

Thin interposer technologies require the control of thin wafer handling and temporary bonding technologies. CEA-Leti offers:

- two major 300mm thin wafer handling technologies
- a process flow diversification, including stress-free wafer-level planarization materials with excellent RF applications behaviors



## Interposer stress management strategy

CEA-Leti offers extensive expertise in the evaluation of stress issues within interposers:

- TSVs induced stress
- warpage control of large interposers
- chip/package Interaction

All topics are studied through comparison of realistic 3D models with in-situ measurements on real 3D demonstrators. In parallel, a large panel of materials have been qualified in order to offer complete Wafer-Level compensation strategy.

*Work performed in the frame of the IRT Nanoelec consortium.*

## Interested in this technology?

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