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DNEURO, DNN* IP FOR FPGA
For high performing DNN running standalone on FPGA

* DNN: Deep Neural Network

TECHNOLOGY

- DNEURO is a complete and independent RTL Hardware Library for DNN integration on FPGA
- Based on dataflow computation, DNEURO has been designed to optimize the use of the DSP available on FPGA
- Thanks to N2D2, the IP can be generated in a few clicks from the DNN description and weights

INNOVATION

- Data flow architecture requiring few memory Potentially without external DDR
- Very high use rate of the DSP per cycle More than 90%
- Configurable precision Integers from 4 to 16 bits, typically 8 bits
- Up to 4 MAC/DSP operations per cycle

PERFORMANCE PROJECTION (AlexNet)

Inference Engine	N2D2 / TensorRT	N2D2 / DNEURO
Board Reference	NVIDIA Tegra X2 (1300 MHz)	Xilinx ZCU102 (200MHz)
Performance	**330 FPS***	**1200 FPS***
Compute Precision	Floating Point 16	Integer 8 + Acc Integer 18
	* FPS = Frame Per Second	

- DNEURO allows DNN Integration on FPGA with extremely high image / second / watt efficiency
- The objective is to meet industrial or strategic requirements, with high constraints in energy, latency, size ...

APPLICATIONS

- Safety/defense Detections in harsh and constrained environment, sovereignty
- Manufacturing Quality and high speed control
- Transportation autonomous vehicles, drones

OUR OFFER

- Expertise in Deep Neural Network Accelerators
- N2D2, CEA Deep learning Platform to generate automatically DNEURO Code

N2D2

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