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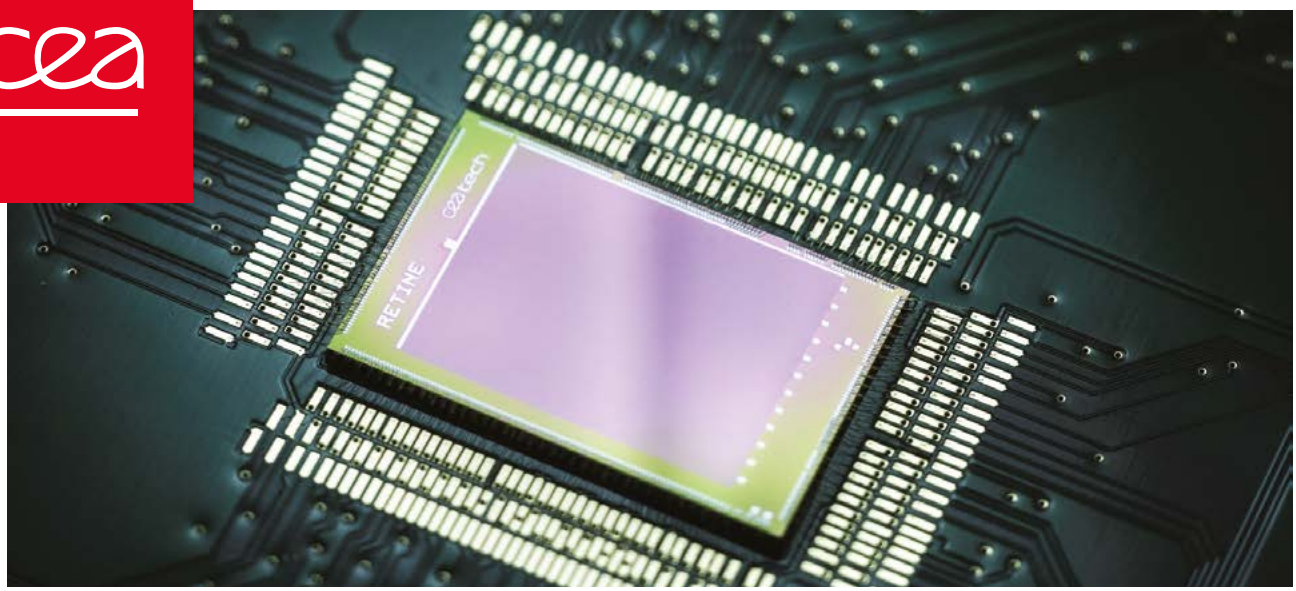


Retine

PATENTS 5 PATENTS

Programmable vision chip enabling high frame rate and low latency image analysis

What is Retine?

In collaboration with CEA-List for embedded imaging processing, CEA-Leti has developped Retine. Thanks to 3D IC stacking technology, it combines an image sensor and a parallel array of processors to form a single vision circuit. Retine can hence acquire upto 5500 fps while featuring flexible scene analysis capabilities. It results in downto millseconds latency between acquisition and computation outputs and the resulting data stream can be reduced to the minimal relevant amount.

Retine's processing capabilities allow to implement pixel based local processing very well, from low-level image processing such as image transformation or filtering to medium-level image processing such as feature detection and extraction at high speed. These types of algorithms benefit directly from the fine-grained parallelism and the local communication mechanisms provided by the Retine chip. The design of this circuit is really scalable as it is built by replicating a 3D elementary brick composed of a matrix of pixels and an elementary processor. Thus, by increasing the resolution, the associated computing power increases in an equivalent way.

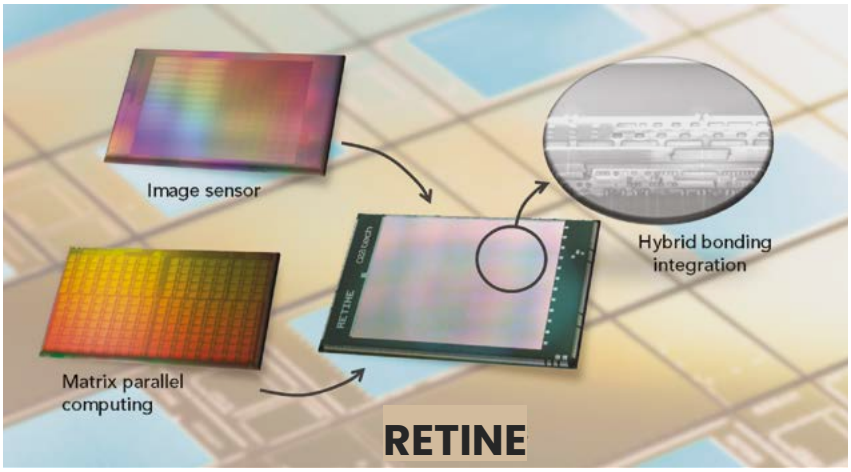
Applications

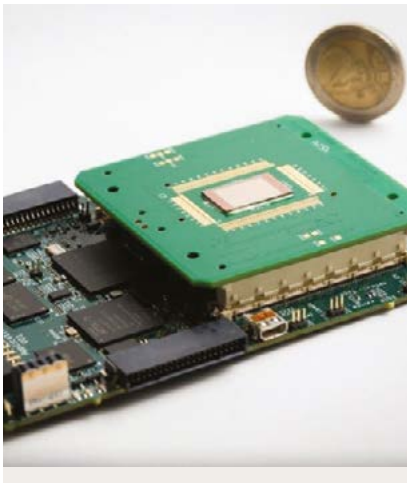
Retine helps improve:

- **Robotics**: compact solution for positioning or tracking control
- **Quality inspection** in manufacturing leveraging on the fly optical monitoring
- High-speed **optical monitoring**
- **Safety** with rapid presence detection to trigger safety devices or promptly cut off engines
- **Drones**: vision chips are helpful for flight assistance through ground positioning and speed estimation, field analysis or ground modeling.
- Implement **machine learning** algorithm inside the sensor to enhance image with semantic informations

What's new?

Retine vision chip is built around a scalable array parallel structure.
The 3D stacked implementation brings a high data bandwidth from the sensor to the processing elements, allowing high speed, minimum latency, image analysis. The 192 multi-core processors enable the execution of differentiated code based on a specific area of the image, allowing multi-processing in the same focal plane array.
Depending on the processing architecture, the chip allows different local feedback on pixel acquisition (integration time, power on/off, etc.).
As a result the chip can be seen as a flexible system able to significantly reduce the need of communication to a main external driver element.





Interested in this technology?

CEA-Leti contact:
Antoine Dupret
antoine.dupret@cea.fr
+ 33 169 080 735
www.cea-leti.com

CEA-List contact:
Magaly Gouttebroze
magaly.gouttebroze@cea.fr
+33 169 089 372
www-list.cea.fr

What's next?

Retine provides a major breakthrough in terms of flexible computing with low latency. It will address the growing needs for image analysis in various industries. In close collaboration between CEA-Leti and CEA-List institutes, the next generation of Retine is under development to reduce pixel size and integrate more processing power into the sensor.

Research for industrial innovation