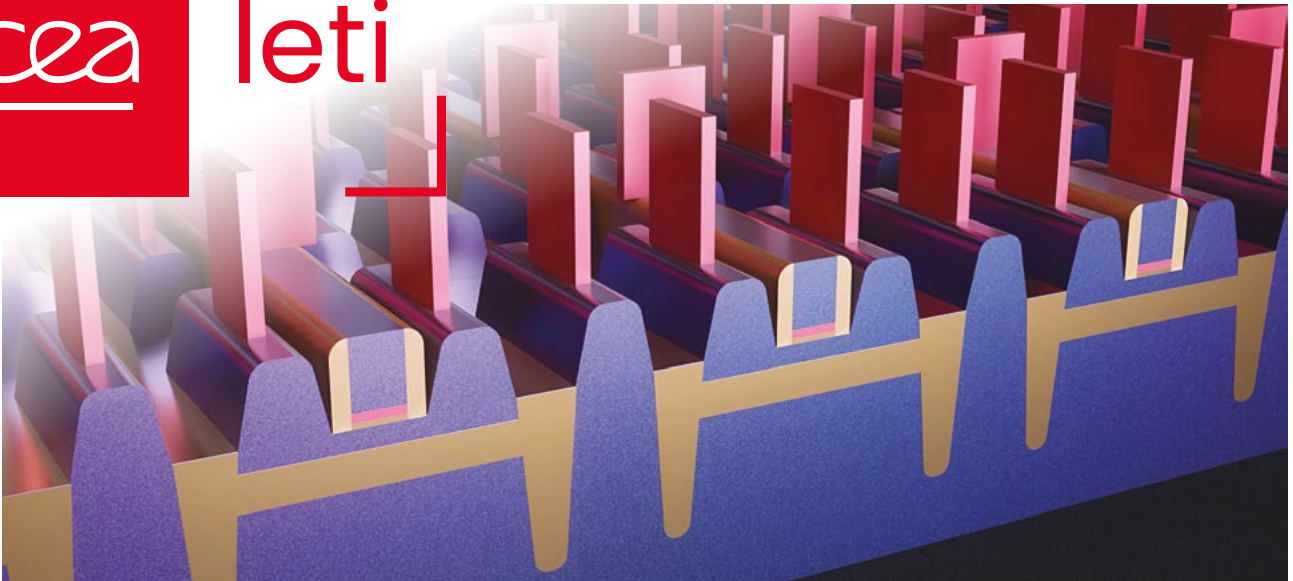




FD-SOI Next Generation 10–7 nm

An innovative generation of chips for the best balance in Power, Performance, Area, Cost and Environmental Impact (PPAC-E) for highly energy efficient applications

What it is

Already used in mobile electronics, automobiles and the Internet of Things, 28–22 nm FD-SOI transistors are currently being produced in volume by STMicroelectronics, Samsung and GlobalFoundries. The transition to the 10 nm node will enable very significant gains in terms of:

- transistor density
- high-performance/low-power trade-off: circuit performance and power consumption will be modulated by back-biasing according to application needs
- reduced current leakage
- costs

What it can do

FD-SOI technology can be found in the world's three major markets:

- **Communications:** 5G and sub-6 GHz smartphones, network infrastructures, components for cybersecurity
- **Automotive industry:** radar and lidar, automotive microcontrollers
- **Smart Devices:** Internet of Things, watches and ultra-low-power connected devices, components for embedded artificial intelligence

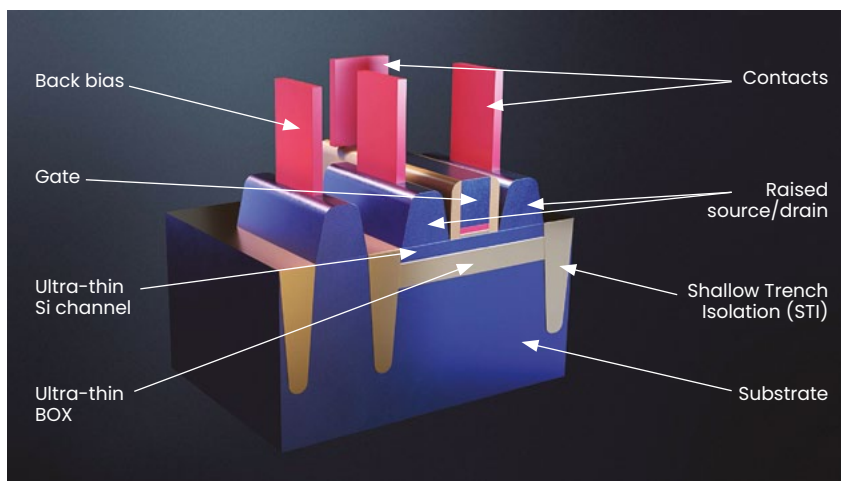
And also in components for the space industry.

What makes it unique

The development of 10 nm FD-SOI involves major advances in terms of substrates, the application of mechanical constraints on materials and devices, miniaturization, advanced lithography and etching processes, polarization flexibility on the back of components (back-biasing), etc.

Improving the performance/consumption trade-off is of particular interest to the communication market in order to improve autonomy and/or enhance functionality.

For automotive applications, the integration of several types of embedded non-volatile memories in the microcontroller back end of line (BEOL) will improve reliability, storage, density, performance and enhanced functionality of FD-SOI technology.



What's next?

Initiated with national NextGen* project and extended today with FAMES Pilot Line**, CEA-Leti is investing heavily in equipment, buildings and human resources to develop 10 nm FD-SOI, while anticipating the specific needs of European semiconductor players. The FAMES Pilot Line will develop five new sets of technologies: FD-SOI 10 and 7 nm process technologies, embedded non-volatile memories, 3D integration, RF components and power management integrated circuit solutions.

This initiative is in line with the EU Chips Act's ambition to strengthen the EU's semiconductor capabilities and ensure technological sovereignty.

The booming FD-SOI market is therefore anticipating the 10nm and 7nm next-generation nodes.

Key figures

- Metal pitch: Minimum distance between the center of two interconnection lines is 48 nm (90 nm in FD-SOI 28 nm)
- CPP (Contacted Poly Pitch): Minimum distance between the center of two gates is 68 nm (114 nm in FD-SOI 28 nm)

Benefits as compared to FD-SOI 28 nm:

- Fourfold increase in transistor density
- At equal speeds, operating power consumption reduced by a factor of five
- At equal power, twice as fast

Key facts

- Forty years ago, the FD-SOI adventure was born at CEA-Leti laboratories in Grenoble, the heart of the French Alps.
- Over 150 patents have been filed in relation to FD-SOI.

Interested in this technology?

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* <https://anr.fr/ProjetIA-22-NEXG-0001>

** <https://fames-pilot-line.eu>

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