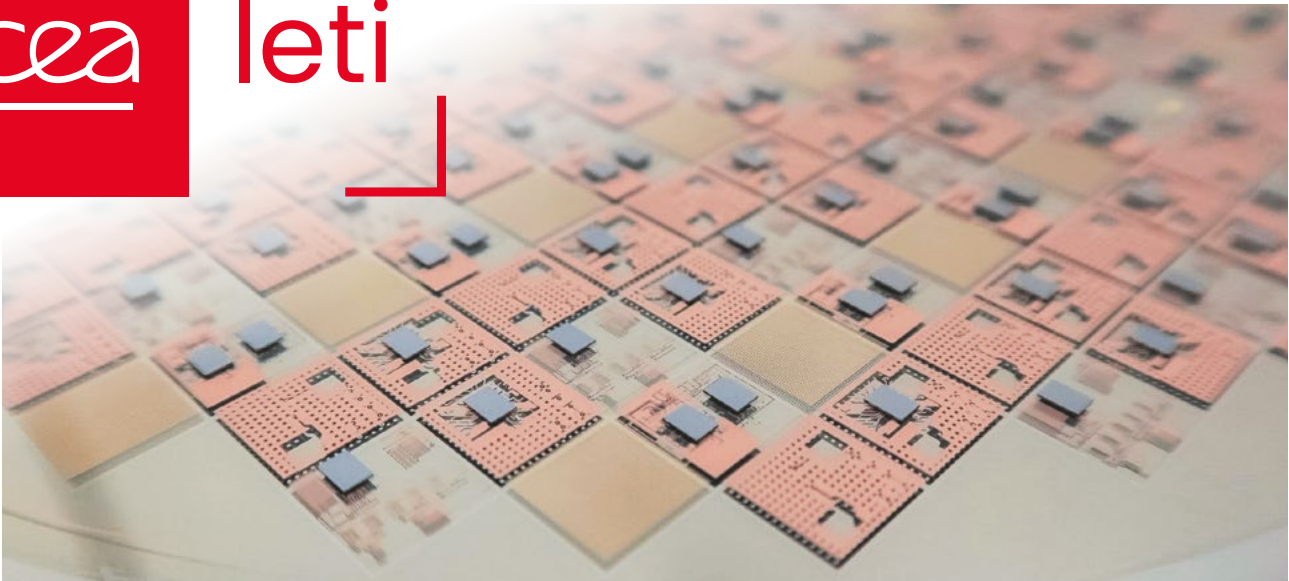
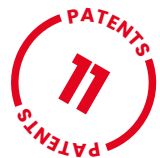




Fan-Out Wafer-Level Packaging



Advanced packaging technology for heterogeneous System-in-Package (SiP)

What is it

CEA-Leti offers a competitive Fan-Out Wafer-Level Packaging technology using 8" wafers. Based on the reconstruction of substrates around individual chips, this technology has become an iconic part of any "More than Moore" strategy. This advanced technology has enabled high-potential, multi-chip system-in-packages since the mid-2000s.

Eliminating the need for intermediate, laminated substrates has enabled the integration of high performance systems with a reduced cost and footprint. It has also paved the way for applications that would have been difficult to address using conventional packaging.

What it can do

RF front-end modules for wireless communications and radar sensing

- Heterogeneous modules combining silicon and III-V technologies
- Integration of antenna in package and passive components

High-speed optical transceivers and sensing systems

- VCSEL, PIN photodiodes and silicon CMOS drivers

Sensing systems

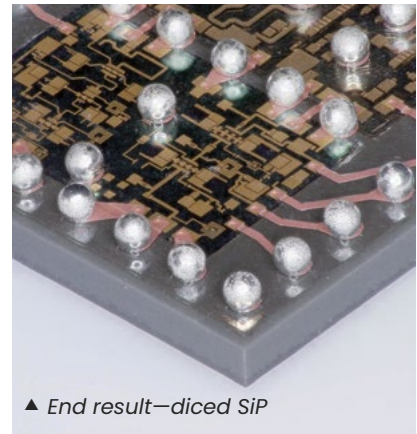
- Integration of various sensors such as MEMS with IC

What makes it unique

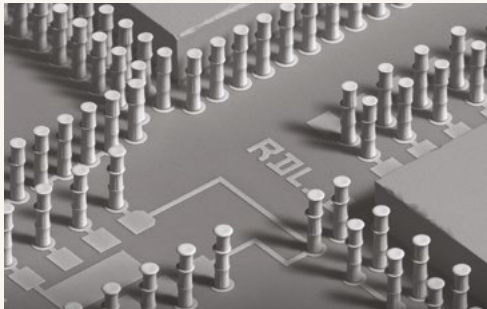
CEA Leti is developing Fan-Out Wafer Level Packaging technology with a focus on the RDL 1st process, with multiple RDL levels depending on customer application and architecture.

By taking advantage of a wide range of possible materials, dimensions and topologies, and thanks to an unprecedented through mold interconnection pitch, we enable the realization of new high-performance 3D architectures.

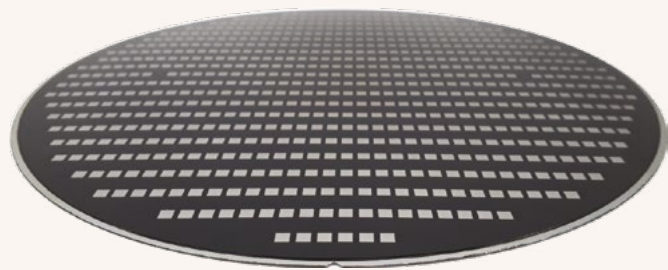
Our 20-year track record, bolstered by numerous patents ranging from technology to final system architecture, enables us to deliver customized solutions.



▲ End result—diced SiP



▲ High aspect ratio through mold interconnect



▲ Fully populated wafer with Si dice

What's next

- Redistribution lines (RDL) with width/space down to 5/5 μm
- Developments for increased frequency in telecom applications ($> 140 \text{ GHz}$)
- Innovative wafer level thermal management approach

Interested in this technology?

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Publications

- **Outstanding Interactive Presentation Paper:** A. Plihon et al., Scalable Through Molding Interconnection realization for advanced Fan-Out Wafer-Level Packaging applications, 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 2122–2127, doi: 10.1109/ECTC51906.2022.00335
- **Best Interactive Presentation Paper:** A. Garnier et al., System in package embedding III-V chips by fan-out wafer-level packaging for RF applications, 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 2016–2023, doi: 10.1109/ECTC32696.2021.00318.
- **Early pioneering work:** Wafer level processing of 3D system in package for RF and data application, Proceedings Electronic Components and Technology, ECTC 2005, pp. 356–361 Vol. 1

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