



leti



# Silicon PIC Platform

Photonics technologies convergence  
on silicon CMOS platform

## What is CEA-Leti's Si PIC platform?

**CEA-Leti's fabrication platform for silicon photonic integrated circuits (PIC) enables large-scale integration of active and passive devices in a flexible CMOS-compatible process.**

Beyond silicon, the platform also offers integration of SiN and III-V bonded epi layers on the same wafer, providing the advantages of each material. The convergence of various photonic platforms combined with CEA-Leti's multi-material process helps address numerous applications with the same technology.

## Applications

Several applications come with this photonics-technologies convergence on a Si CMOS platform, including:

- **Communication:** telecom, datacom, 5G infrastructures, quantum cryptography for cybersecurity
- **Computing:** computer communication for high performance computing (HPC), quantum computing and neuromorphic computing for AI
- **Sensing:** optical gas sensing, structural health monitoring and 3D sensing such as LIDAR

*Work performed in the frame  
of the IRT Nanoelec consortium*

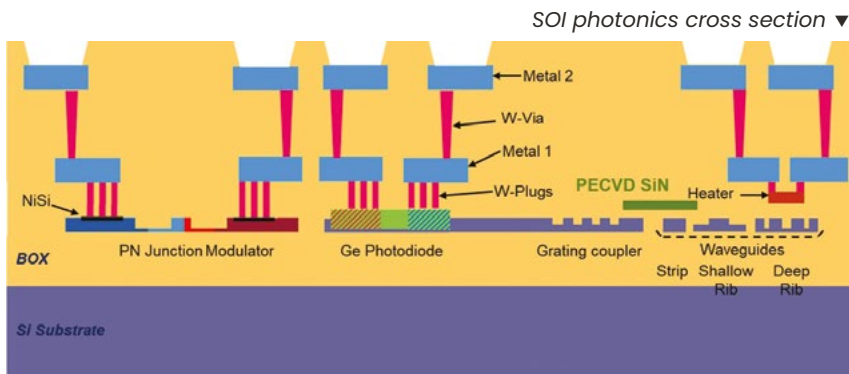


## What's new?

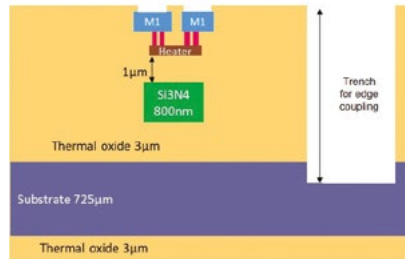
Benefits of this convergence offer CEA-Leti's partners a greater number of functions on photonic integrated circuits (PIC), fabricated on an advanced CMOS-compatible platform.

### CEA-Leti's key achievements:

- Mature device library for O-band and C-band in a process design kit (PDK), compatible with conventional CAD tools
- Small feature size and low sidewall roughness
- III-V integration on CMOS-compatible process through collective die bonding
- Multilayer Si/Si or SiN/Si for 3D photonics
- 2D beam steering based on SiN OPA
- Tunable DBR, DFB, racetrack lasers



ULL-SiN cross section ►



CEA-Leti's also offers a state-of-the-art platform for ultra-low loss silicon nitride (ULL-SiN) on 200 mm wafers, based on 800 nm Si<sub>3</sub>N<sub>4</sub> LPCVD film on 3 µm insulation oxide.

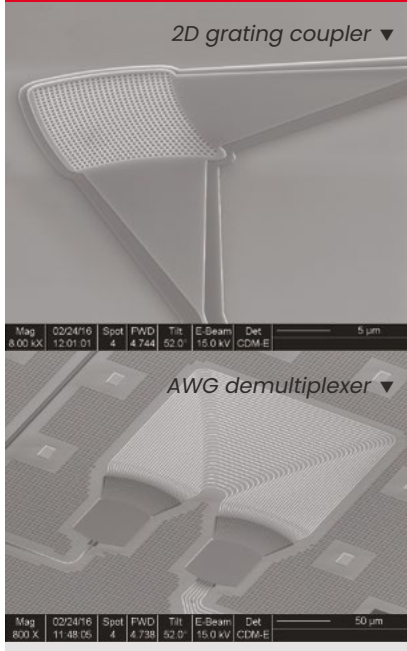
## What's next?

CEA-Leti's Optics and Photonics Division is working on:

- Focus on ultra low insertion loss and high efficiency Si & SiN devices
- Develop high efficiency NbN Superconducting single photon detector (SSPD)
- Introduce new materials
- Keep on the improvement of wafer scale heterogeneous integration

## Key features

- 300 mm SOI substrate with 310 nm Si, other thicknesses available
- Multilevel silicon patterning for silicon heights of 0, 65, 165 and 310 nm
- Selective Ge epitaxy
- SiN layer (optional)
- Ti/TiN heater
- 6 implant levels for p-type and n-type for electro-optic modulators and silicon doped heaters
- Silicide tungsten contact
- III-V collective die bonding



## Interested in this technology?

Contact:

**Eleonore Hardy**

[eleonore.hardy@cea.fr](mailto:eleonore.hardy@cea.fr)

+33 438 782 639

**CEA-Leti, technology research institute**

17 avenue des Martyrs, 38054 Grenoble Cedex 9, France

[cea-leti.com](http://cea-leti.com)

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