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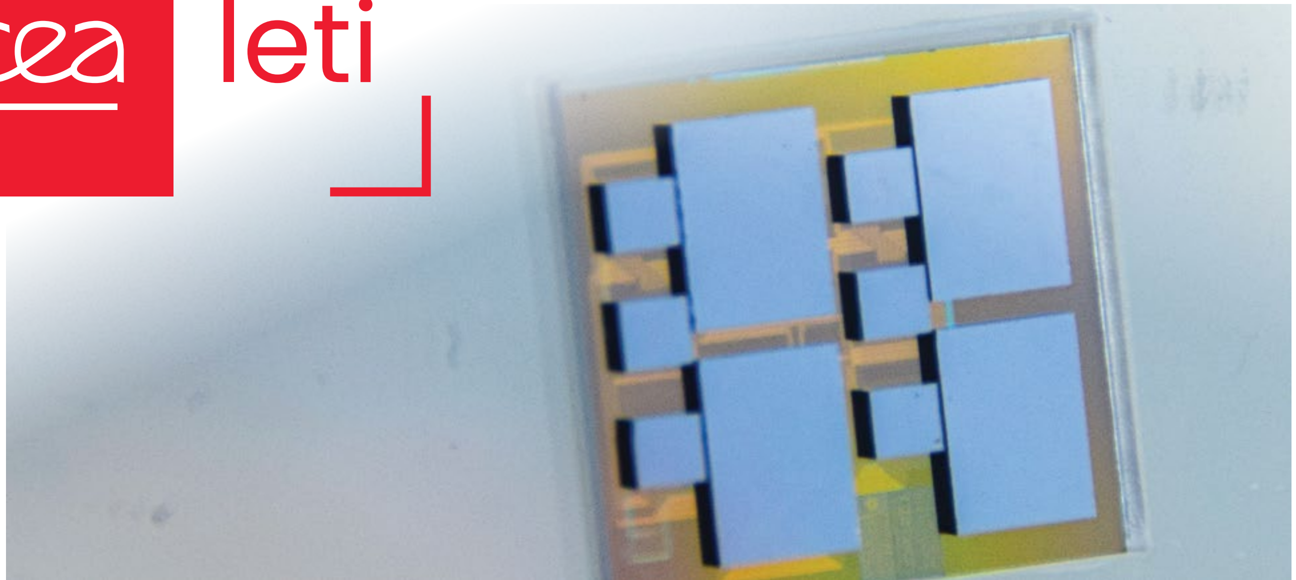

3D Chiplet Integration

10+ PATENTS

Optimizing power, performance, area, cost, and environmental impact with heterogeneous 3D integration

What it is

CEA-Leti possesses a comprehensive set of heterogeneous 3D chiplet integration tools and technologies:

- **Fine-pitch, precision-aligned wafer-to-wafer and die-to-wafer interconnects**, copper bumps, and hybrid bonding.
- **Vertical interconnects** using small-diameter, high-density through silicon vias (TSV HD), through different substrates—silicon, glass, organic.
- **Chiplet-to-chiplet communications** using passive, active, photonic interposers, enabling co-packaged optics.
- **Fan-out wafer-level packaging (FOWLP)**, which entails reconstituting the substrate around individual dies, enables multi-chip systems and the integration of higher-performance, more compact, lower-cost systems.

What it can do

CEA-Leti's 3D integration technologies respond to tomorrow's challenges in a wide range of applications, including **high-performance computing (HPC), AI, co-package optics, RF integration, quantum computing, power delivery, and also imagers and displays**.

For HPC and AI, for example, each chiplet can be optimized according to its function (processor, accelerator, memory, serializer/deserializer, etc.). The number of computing and memory chiplets can be increased as needed, and chiplets with other functions (RF communication, microcontrollers, power management, sensors, imagers, etc.) can also be integrated.

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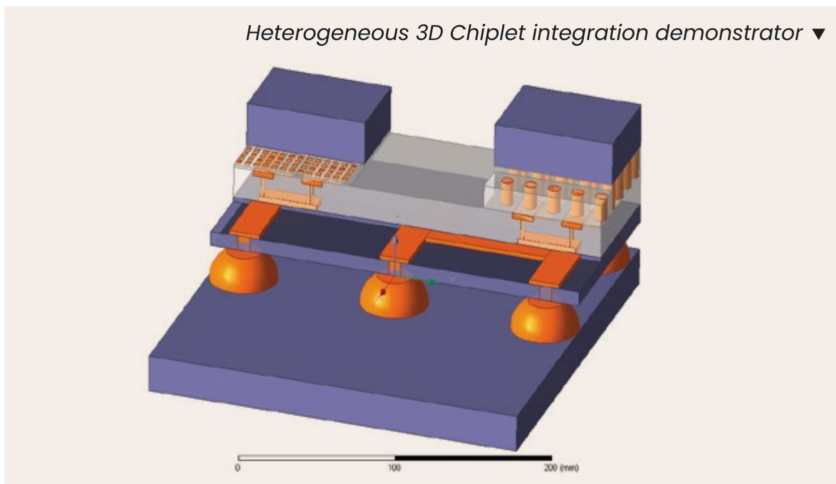
What makes it unique

Heterogeneous 3D chiplet integration offers unprecedented flexibility. Each chiplet, depending on its function and the requirements of the target application, can be optimized separately and manufactured using the most appropriate technology node, resulting in the best possible PPACE tradeoff. Substrates of different sizes and materials from different foundries can be assembled with agressive interconnect pitches using standard semiconductor industry processes.

CEA-Leti offers advanced hybrid bonding, with aggressive pitches, in different flavors : wafer-to-wafer and die-to-wafer assembly, including capability of handling Know-Good-Dies (KGD) to support industry test requirements, and with different materials allowing heterogeneous integration (the widely used copper but also Ti, GaN, InP, Nb, glass substrate, low temperature annealing, etc).

Heterogeneous 3D Chiplet integration demonstrator ▼



What's next?

CEA-Leti possesses unrivaled expertise in the design and architecture of the most advanced 3D chips. Using holistic models in a design-technology co-optimization/system-technology co-optimization (DTCO/STCO) approach, CEA-Leti can speed up the development of complex 3D chips by measuring the positive impacts of different configurations on the overall architecture. And, with its own semi-industrial cleanrooms, CEA-Leti can support foundries, fabless companies, and end-product manufacturers right through to the prototyping and transfer of specific integrations for manufacturing.

Key figures

Interconnect pitches:

- Hybrid bonding wafer-to-wafer : minimum pitch = 400 nm
- Hybrid bonding Die-to-wafer: minimum pitch = 1 µm
- Copper pillar: minimum pitch = 10µm

Through Silicon Via (TSV) pitches:

- 100,000 high density TSV per mm²: 3-10 µm, Ø <2 µm
- 1,000 TSV middle per mm²: 20 µm-100 µm, Ø 2-15 µm
- Low-density TSV last (V/mm²: low I/O): 100 µm-500 µm, Ø 40 µm-100 µm

Scientific publications

- Thonnat, Y., et al. (2026). *A 3.19pJ/bit Electro-Optical Router with 18ns Setup Frame-Level Routing and 1-6 Wavelength Flexible Link Capacity for Photonic Interposers.* ISSCC.
- Najem, M., et al. (2026). *Die-To-Wafer Hybrid Bonding Technology Down to 1 µm Pitch for Multi-Die Stacking Integration.* ECTC.

Interested in this technology?

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