

## **OWLY-EYED**

# **SUB-ELECTRON READOUT NOISE** FOR LOW-LIGHT IMAGING

#### **WHAT IS OWLY-EYED?**

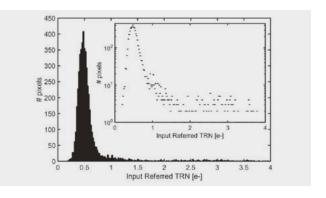
A sub-0.5e-rms temporal read noise VGA (640H $\times$ 480V) CMOS image sensor has been integrated in a standard 0.18  $\mu$ m 4PM CMOS process.

The low noise performance is achieved exclusively through circuit optimization without any process refinements. The presented imager relies on a 4T pixel of 6.5 µm pitch with a properly sized and biased thin oxide PMOS source follower.

Process	180 nm CIS
Active array size	640(H)×480(V)
Pixel size [µm <sup>2</sup> ]	6.5×6.5
Fill factor [%]	40
Conversion gain $[\mu V/e^-]$	160
Full well capacity [e <sup>-</sup> ]	6400
Column-level gain	$\times 1 \times 64$
Pixel readout time [µ s]	25
Read noise (peak) [e <sub>rms</sub> ]	0.48 @ room T
Dark current [e <sup>-</sup> /s]	$5.6$ @ room $T^{\circ}$
PRNU [%]	0.77
Imager lag [%]	0.1

### **APPLICATIONS**

Today, markets such as medical, security, industrial vision, defence, scientific imaging and space are expected to grow and increase the demand for more sensitive CIS operating in low-light conditions.



### **WHAT'S NEW?**

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To further reduce the TRN in a standard CIS technology, without any process refinements, a new circuit-optimization technique has been developed. A detailed noise analysis of a classic CIS readout chain shows that the input referred 1/f noise can be reduced using three techniques that can be combined with each other:

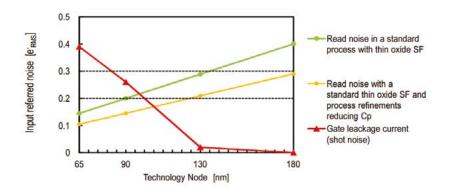
- the **first** one consists of the reduction of the transistor 1/f noise process parameter (K factor). By minimizing the contribution of all parasitic capacitances to the sense node
- the **second** one is, including overlap, wiring and junction's capacitance (Cp, Ce)
- the **third** technique consists of optimally sizing the in-pixel source follower (SF) transistor by using a minimum gate width (W), an optimum gate length (L) and the best available oxide thickness (Cox).

$$\overline{Q_{n,1/f}^2} = \alpha_{CMS} \frac{K \left(C_P + 2C_e \cdot W + \frac{2}{3}C_{ox} \cdot W \cdot L\right)^2}{C_{ox}^2 \cdot W \cdot L}$$

The first and second approaches often have been addressed using only process modifications. In this technique, we apply the third technique by making only design choices (W, L and Cox).

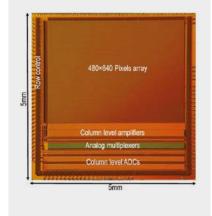
### **WHAT'S NEXT?**

Besides the read noise originating from the 1/f and thermal noise, the gate-leakage current shot noise, up to now, has been neglected due to the extremely low levels of the leakage currents achieved thanks to the used technology. The figure below also shows how the input-referred noise is expected to decrease, only by taking advantage of the technology downscaling.



#### **KEY FACTS:**

- 3 publications in leading journals (JSSCC; Sensors, IISW)
- Filed patents
- Industrial partnerships (innovation transfer)



## INTERESTED IN THIS TECHNOLOGY?

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