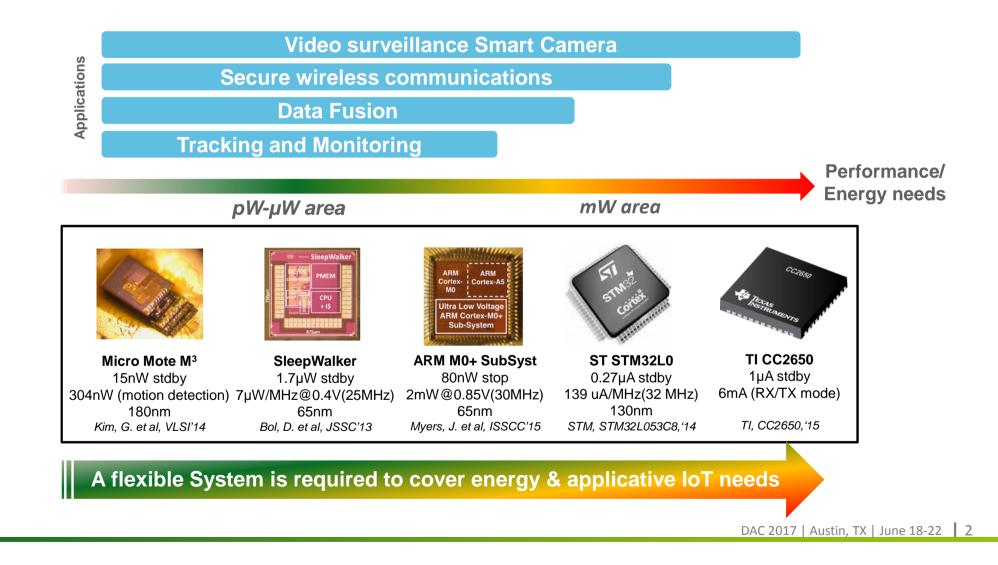
Ceatech

L-IOT: a Flexible Energy Efficient Platform Targeting Wide Range IoT Applications

E. Beigné, <u>I. Miro-Panades</u>, A. Valentian, J.F. Christmann,
S. Bacles-Min, A. Verdant, G. Sicard, C. Jany, B. Martineau,
D. Morche, C. Bernier, A. Molnos, D. Couroussé, S. Lesecq,
G. Pillonnet, A. Quelen, F. Badets

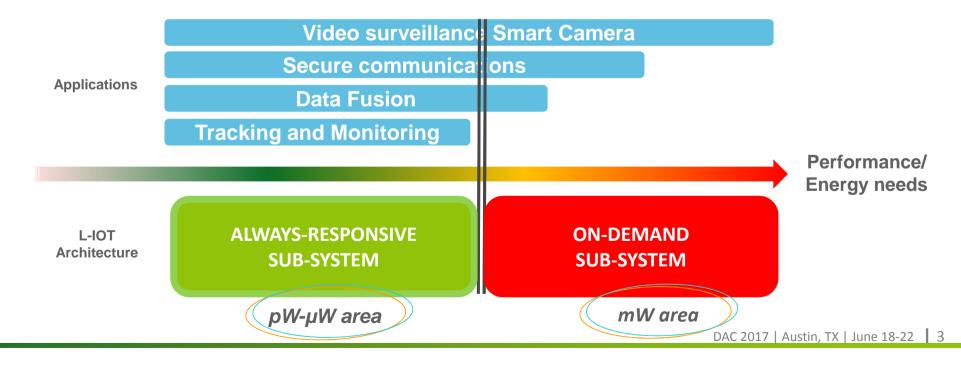
CEA, LETI, MINATEC Campus, F-38054 Grenoble, France

IoT applications: a wide range of performance and energy needs

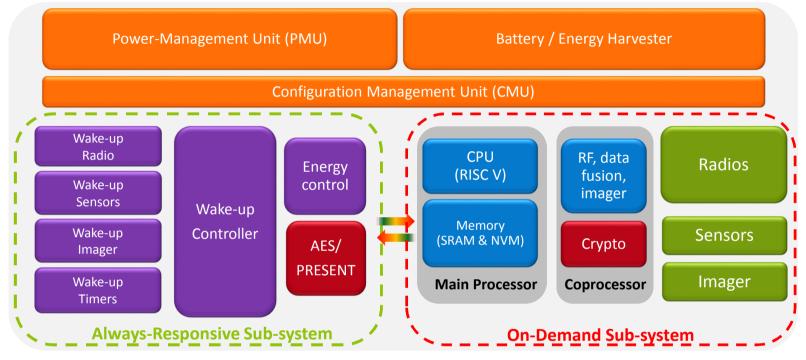


L-IoT : a flexible platform targeting high energy efficiency

- A flexible and <u>fully integrated platform covering a wide range of performance</u> and energy needs required by IoT applications
- Architecture : Always-Responsive/On-Demand partitioning
- Design : Ultra low power and adaptive IP blocks (analog/digital)
- Technology : FDSOI 28 nm technology brings more flexibility (V_{BB})

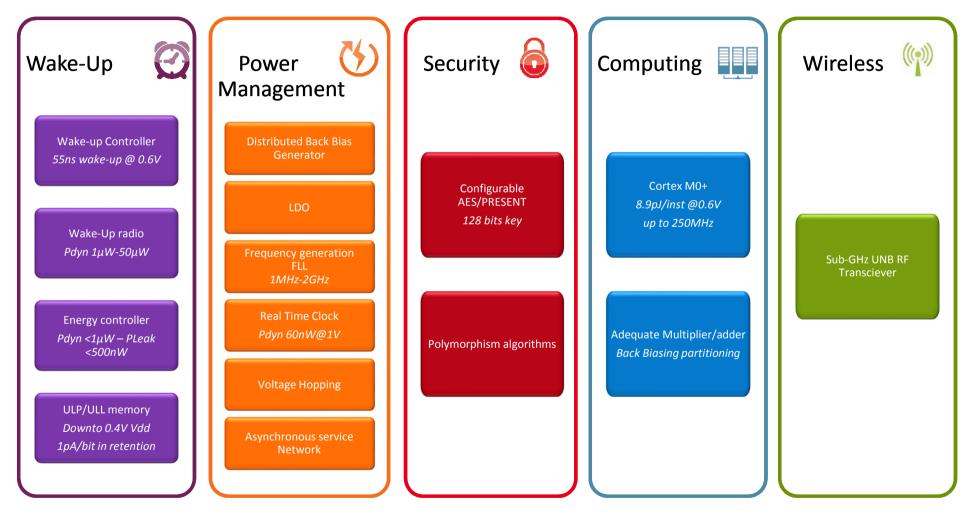


L-IoT : Detailed architecture and main characteristics



- Advanced Wake-up features : radio, imager, sensors, timers controlled by an asynchronous Wake-up processor
- Advanced co-processing for image and radio digital Base Band
- Adaptive security features for authentication, identification and cryptography
- Efficient Power and Configuration units asynch energy controller

L-IoT : available HW and SW IPs



Summary

- A flexible platform suitable for a fragmented IoT market and variable performance/energy needs
 - Architecture partionned into wake-up and on-demand sub-systems
 - Ultra fast wake-up features
 - Ultra low power and adaptive mixed-signal IPs available
- Ultra low energy and adaptivity are key technologies provided by L-IoT
- Mixed-signal circuit integration and global optimization in FDSOI 28nm technology

Acknowledgements & references

Acknowledgments

- THINGS2DO project (JTI Contract Number 621221), co-funded by grants from France and the ECSEL Joint Undertaking.
- BENEFIC project (CA505), co-funded by the framework of CATRENE, the EUREKA cluster for Application and Technology Research in Europe on NanoElectronics, and National Funding Agencies of France, the Netherlands and Portugal
- ST Microelectronics

References

- D. J. Pagliari et al., "A methodology for the design of dynamic accuracy operators by runtime back bias," DATE, 2017
- E. Beigne et al., "Asynchronous Circuit Designs for the Internet of Everything: A Methodology for Ultralow-Power Circuits with GALS Architecture," in IEEE Solid-State Circuits Magazine, 2016
- _ D. H. Bui et al., "Ultra low-power and low-energy 32-bit datapath AES architecture for IoT applications," ICICDT, 2016
- T. Mesquida et al., "Impact of the AER-induced timing distortion on Spiking Neural Networks implementing DSP," PRIME, 2016
- B. Martineau et al., "Towards fully integrated 28nm UTBB FD-SOI IoT node: The sub-50μW RF receiver," S3S, 2016
- S. Chairat et al., "Ultra low energy FDSOI asynchronous reconfiguration network for an IoT wireless sensor network node," S3S, 2016
- _ D. Couroussé et al., "Runtime code polymorphism as a protection against side channel attacks," WISTP, 2016
- S. Chairat et al., "Dedicated network for distributed configuration in a mixed-signal Wireless Sensor Node circuit," PATMOS, 2015
- E. Beigne et al., "UTBB FDSOI technology flexibility for ultra low power internet-of-things applications," ESSDERC, 2015
- E. Beigne et al., "Ultra-low power volatile and non-volatile asynchronous circuits using back-biasing," ECCTD, 2015
- F. Berthier et al., "Power gain estimation of an event-driven wake-up controller dedicated to WSN's microcontroller," NEWCAS 2015
- Y. Akgul et al., "Power management through DVFS and dynamic body biasing in FD-SOI circuits," DAC, 2014
- D. Couroussé et al., "COGITO: Code polymorphism to secure devices," SECRYPT, 2014
- I. Miro-Panades et al., "A Fine-Grain Variation-Aware Dynamic Vdd-Hopping AVFS Architecture on a 32 nm GALS MPSoC," JSSC, 2014.
- J. F. Christmann et al., "Event-driven asynchronous voltage monitoring in energy harvesting platforms," NEWCAS, 2012
- _ J. F. Christmann et al., "Energy harvesting and power management for autonomous sensor nodes," DAC, 2012
- C. Albea et al., "Architecture and Robust Control of a DFLL for Fine-Grain DVFS in GALS Structures," JOLP, 2011

DAC 2017 | Austin, TX | June 18-22 7