DENSITY AND EFFICIENCY: TECHNOLOGIES AND DEVICES TO ADDRESS COMPUTING CHALLENGES

Carlo Reita - Director Technical Marketing Strategy, Nanoelectronics

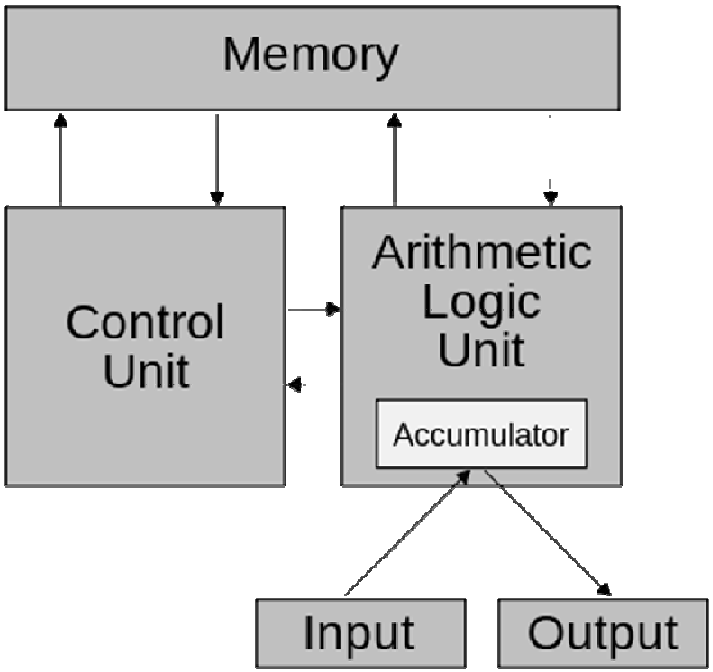
RC21

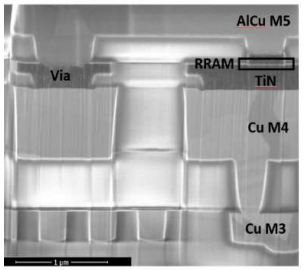
ANSWER THE CHALLENGES OF ADVANCED COMPUTING

Memory Bottleneck

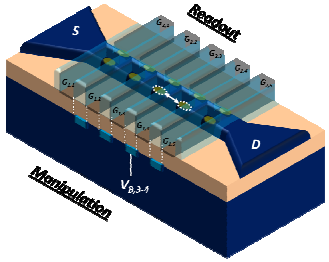
Limit of Shrinking

Limit of Power Dissipation

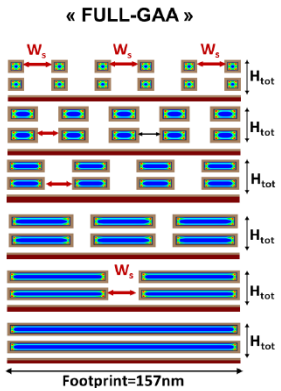




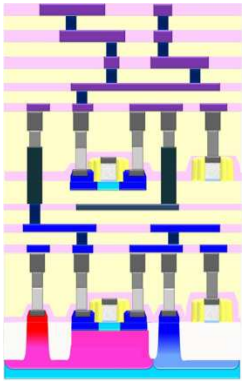
New Memories



New Architectures



Ultimate Scaling



3D

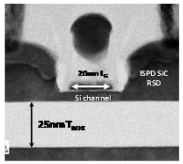
Diapositive 2

RC21 Pourriez vous refaire le chemin à gauche de façon graphiquement plus "jolie" là c'est un chemin fait de fçon trés schematique
REITA Carlo 211212; 07/07/2017

DEVELOPING THE BUILDING BLOCKS FOR DATA PROCESSING

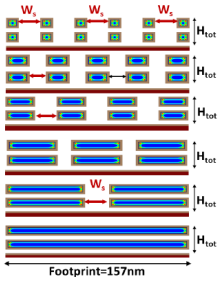
Power Efficient FDSOI

22FD



12FD

« FULL-GAA »



Non Planar / Stacked NW

Mainstream FinFET

14nm	2017	7nm	2023	3nm
2014	10nm	2020	5nm	2026

New Memories in Logic

Cryo CMOS

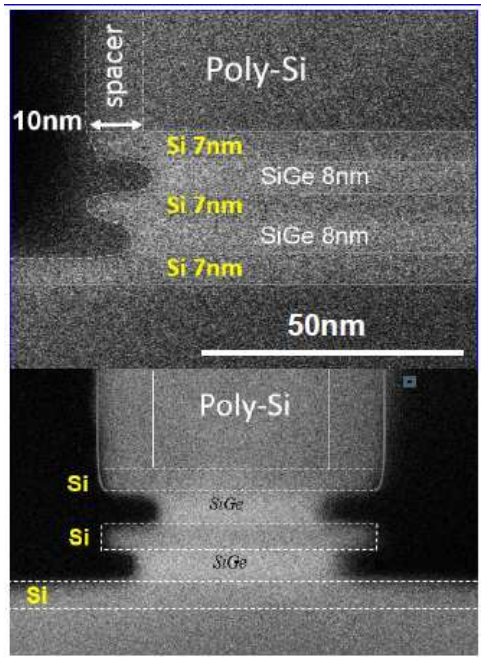
Si Quantum Bits

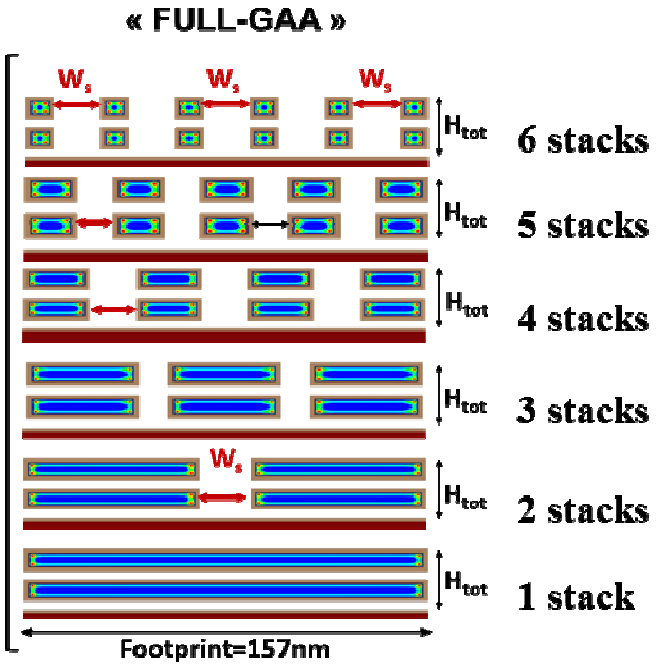
CoolCube™ for 3D VLSI

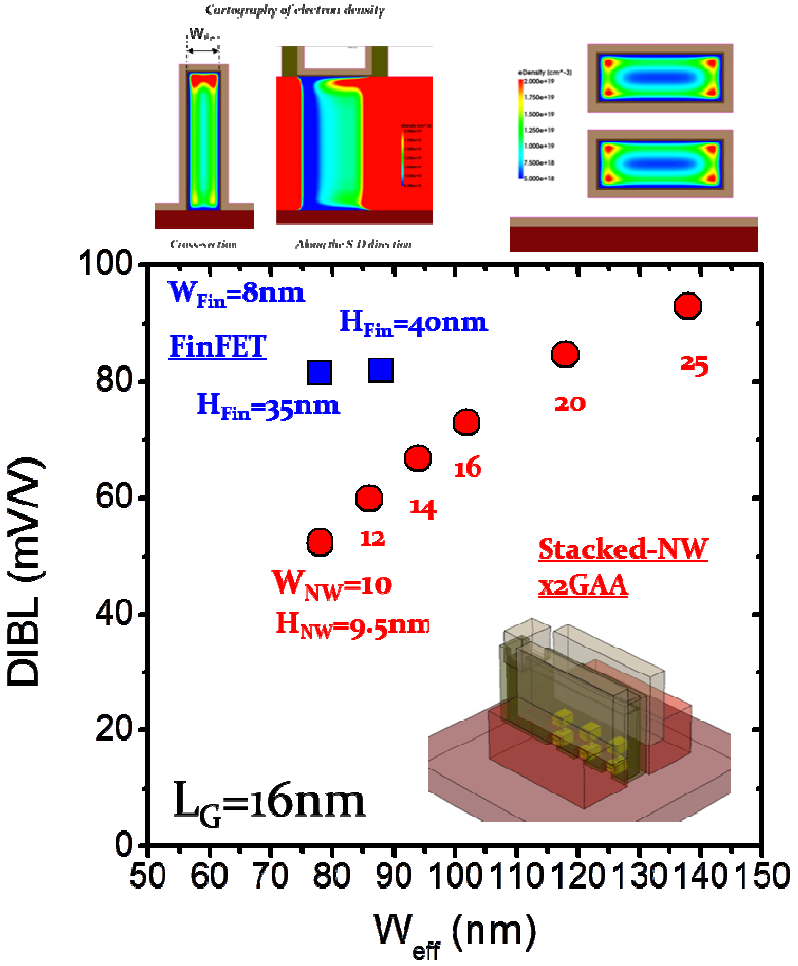
PDKs for Benchmarking Each Approach

STACKED NANOWIRES FOR 7NM AND BEYOND

How to Design Stacked-NW?







PDKs Validated with 10nm Silicon Device Data

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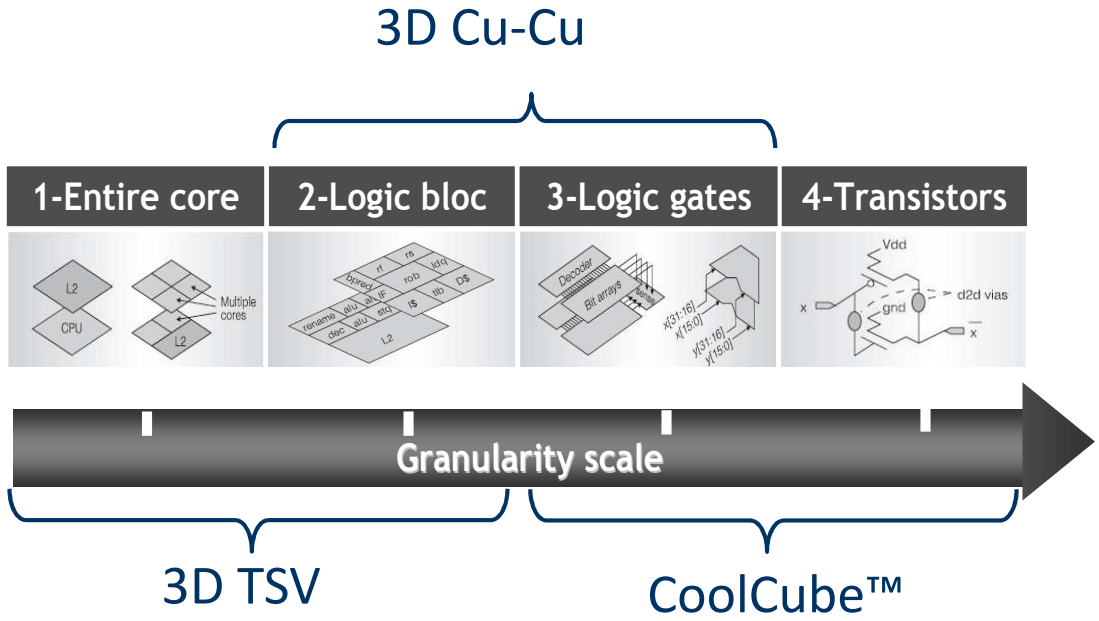
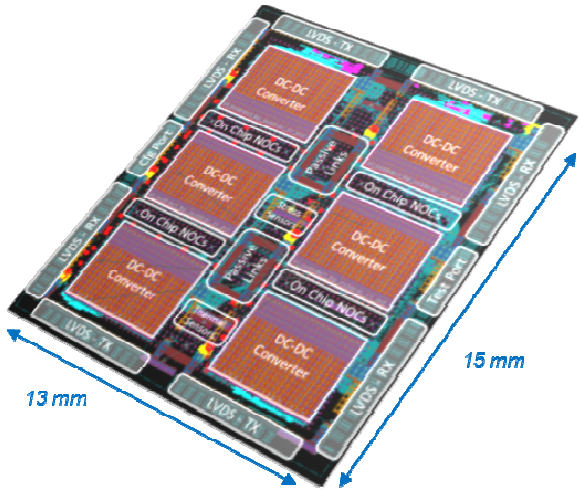
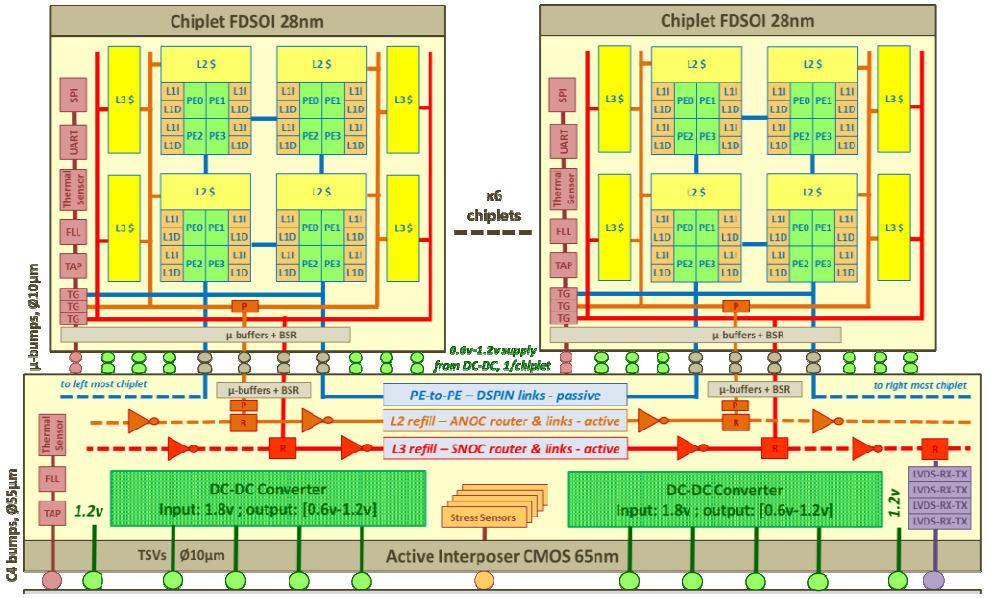
3D FOR OPTIMIZING THE SYSTEMS



➔ Gain obtained by shortening interconnection, optimizing function and cost by partitioning and reducing latency





Diapositive 5

RC22 L'images de gauche aussi a besoin de etre refaite. Elle n'est pas à nous et pas tres attraiante non plus

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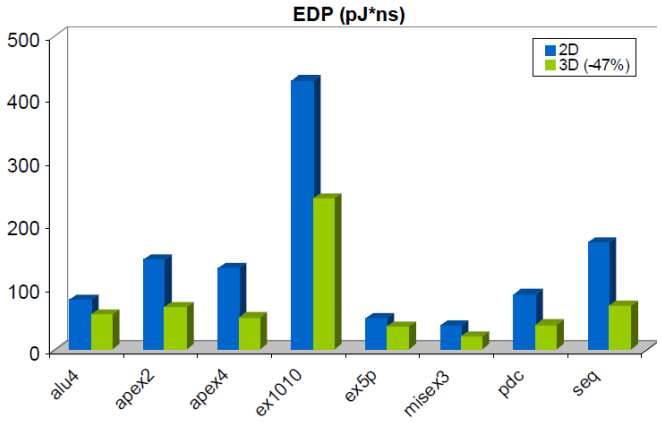
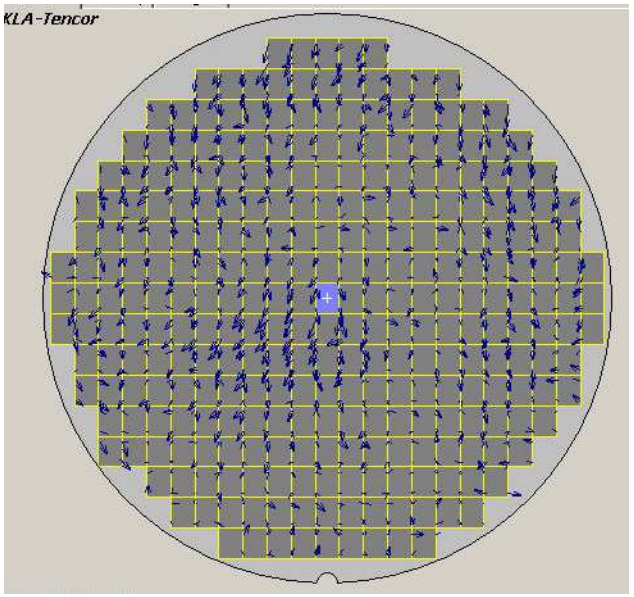
COOLCUBE™

Design tools and 2D vs 3D benchmark

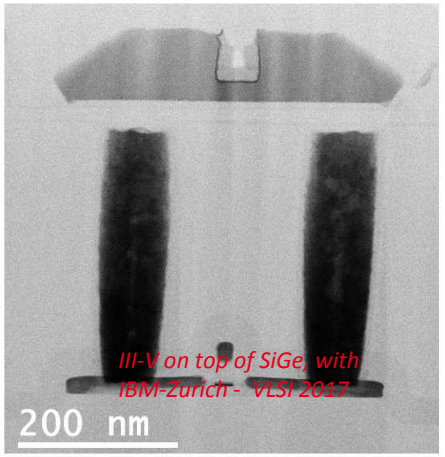
Average gain benchmark 2D vs 3D

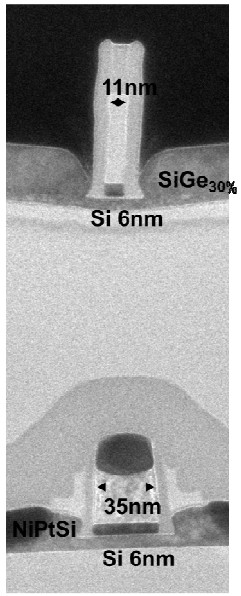
- Area gain=55%
- Perf gain = 23%
- Power gain = 12%



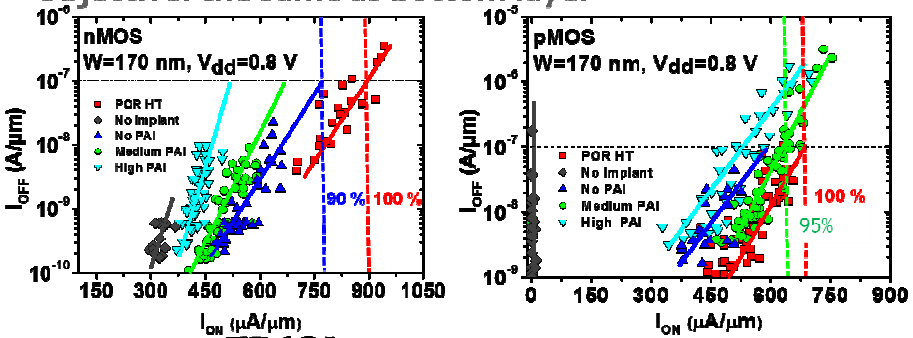


Planar over planar
Lg = 50 over Lg = 25





Objective: the same as bottom layer



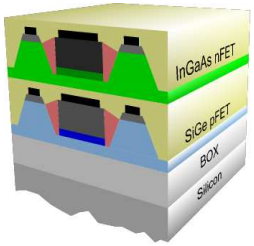
14 FDSOI low thermal budget electrical characteristics

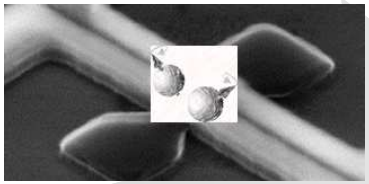
RC23

FUTURE OF 3D DEVELOPMENTS

RF

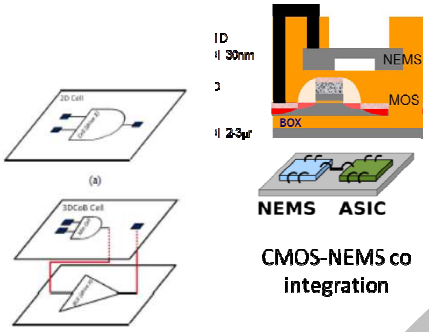
Heterogeneous CMOS



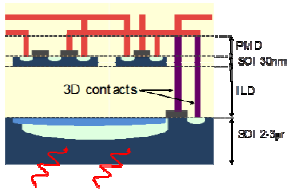


IoT

NEMS co-integration



CMOS-NEMS co integration



2016

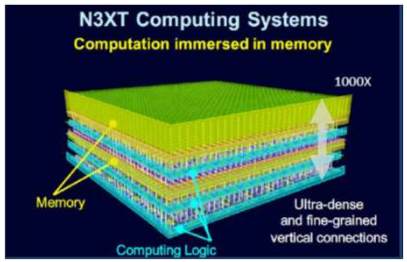
Low-Power Applications

Relaxed technology for top layer 3D image pixel for image sensors

2020

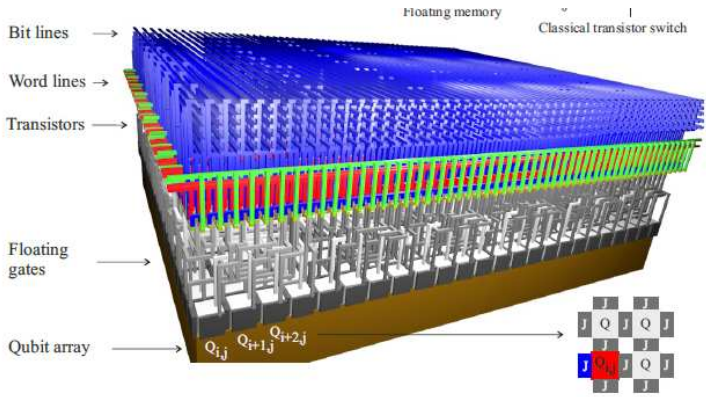
Computing

Advanced nodes



2025

Neuromophic and Quantum Computing



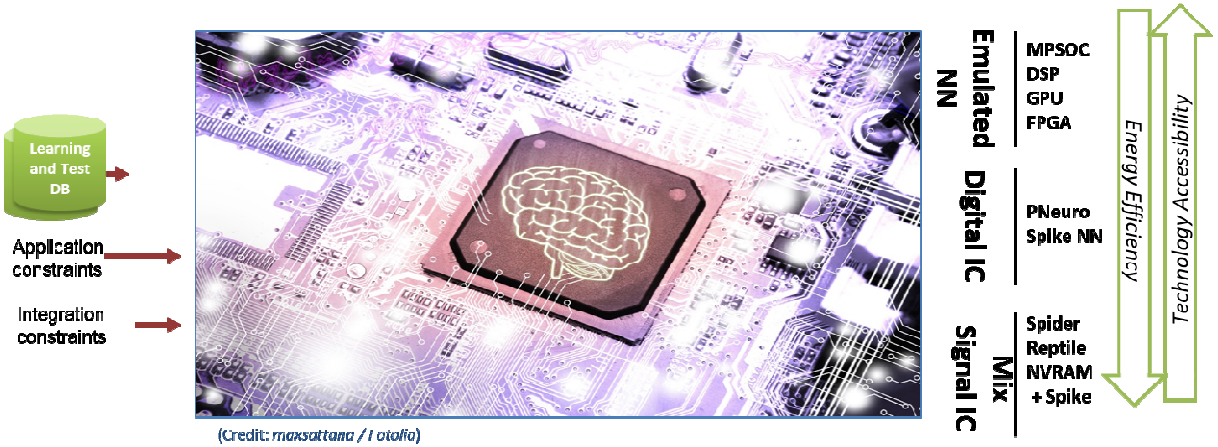
Diapositive 7

RC23 Ici aussi les concepts sont ceux que on veut pousser ma la veste graphique est tres brouillon, pouvez vous faire mieux avec vos competences et moyens?

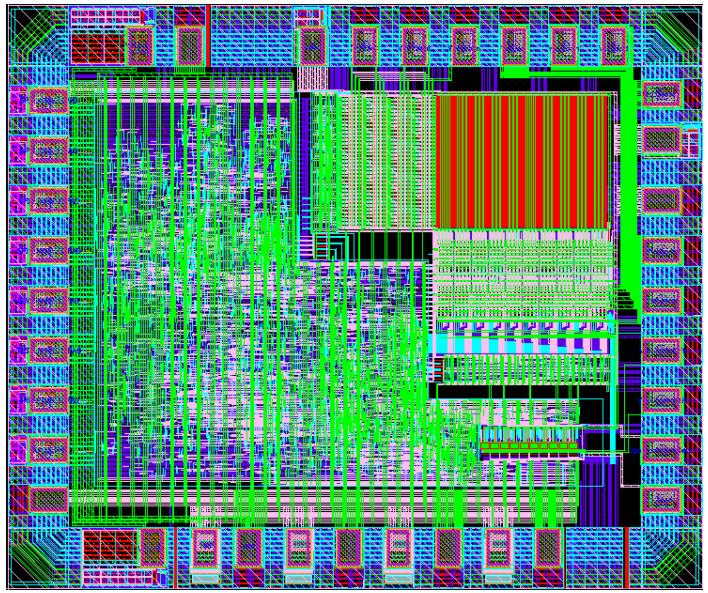
REITA Carlo 211212; 07/07/2017

NEW ARCHITECTURE DEVELOPMENT: NEURAL NETWORK DESIGN

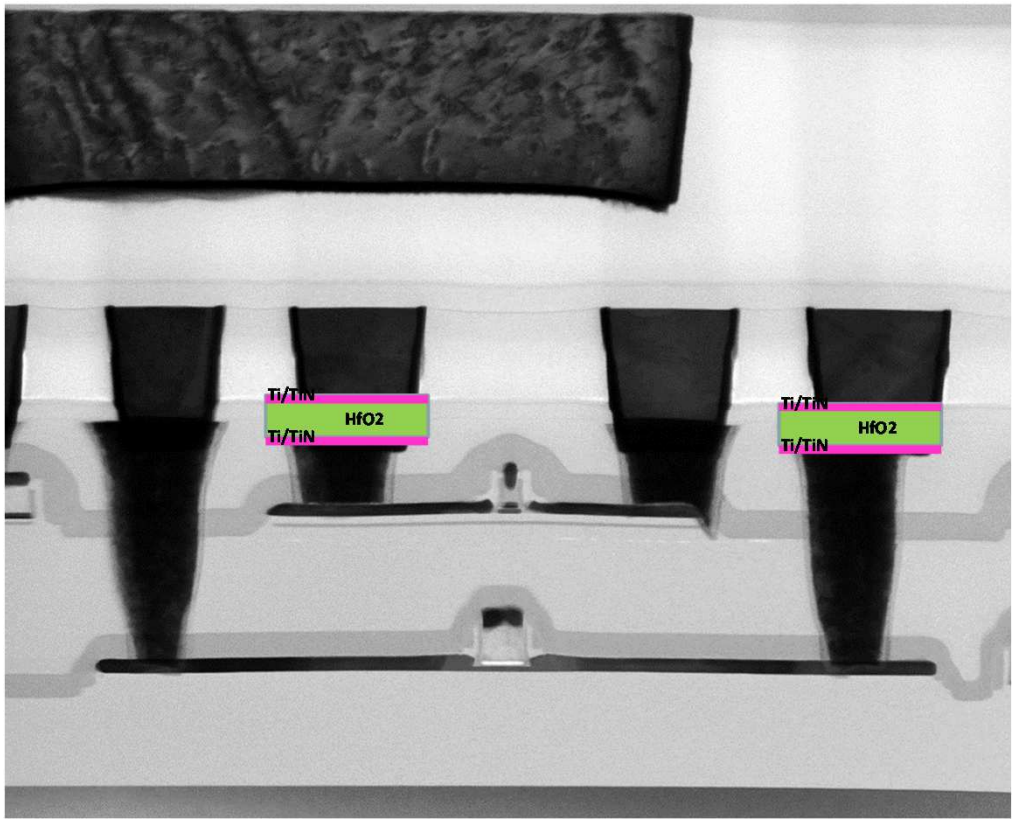
N2D2: Full architecture and design environment to get to a mission optimized implementation



- Fully integrated CMOS+OXRAM Neural Network core



3D INTEGRATION COUPLED WITH RRAM

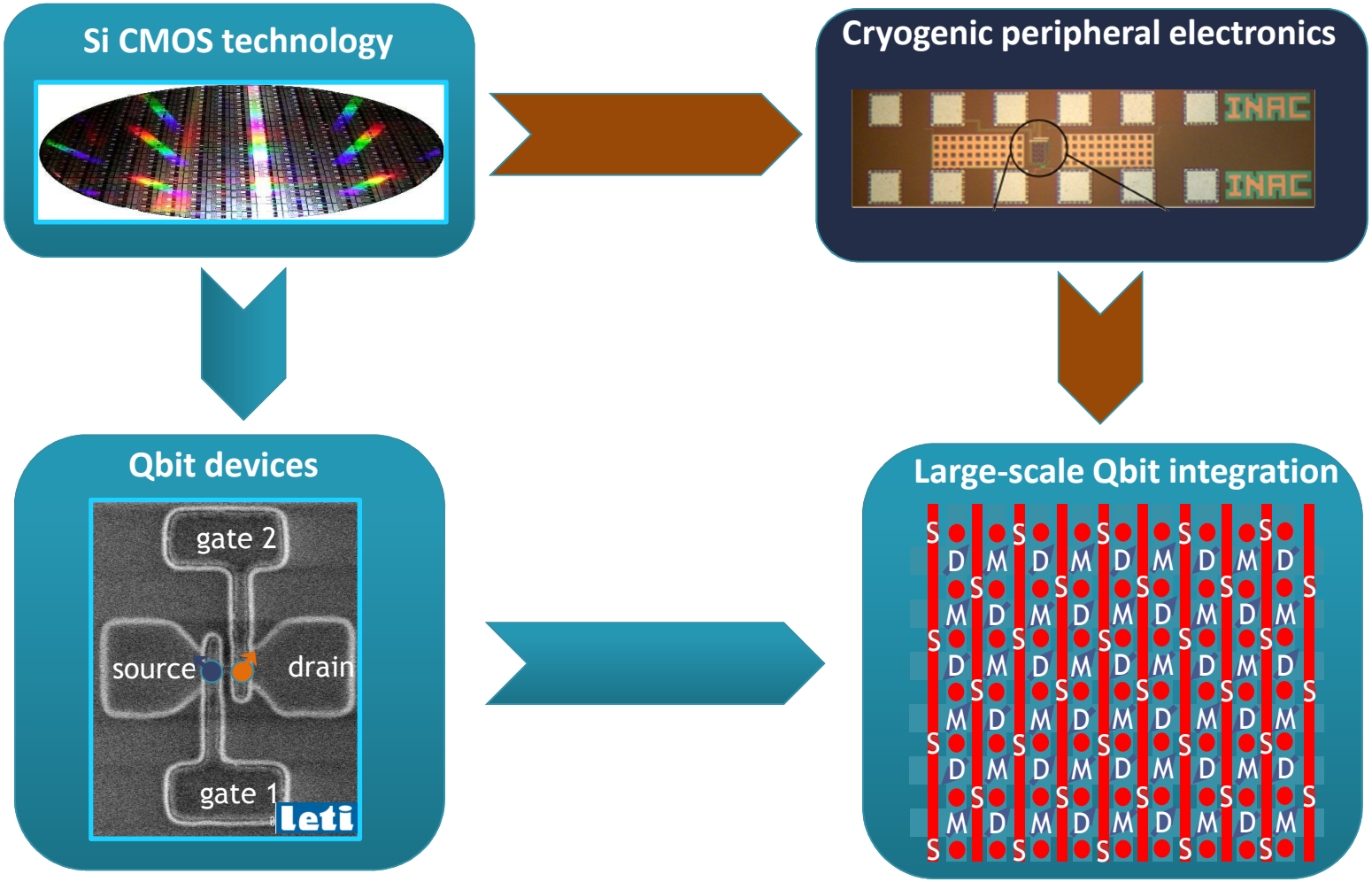


NeuRAM3

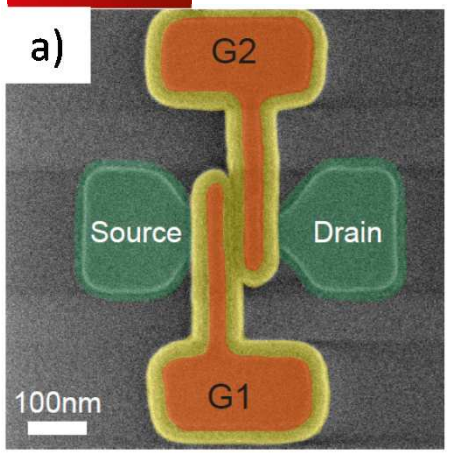
HORIZON 2020

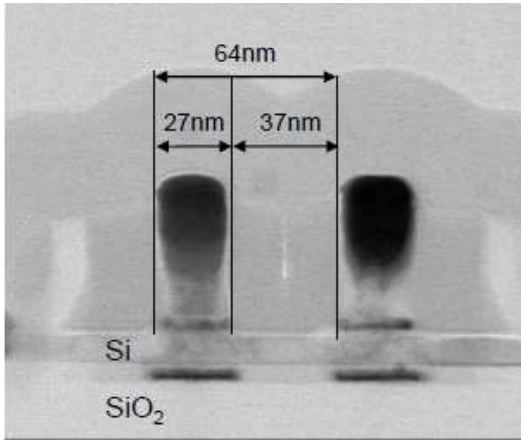
- Using CoolCube for highly-dense integrated neural networks with RRAMs
- Mixed analog/digital spiking architecture for distributed AI

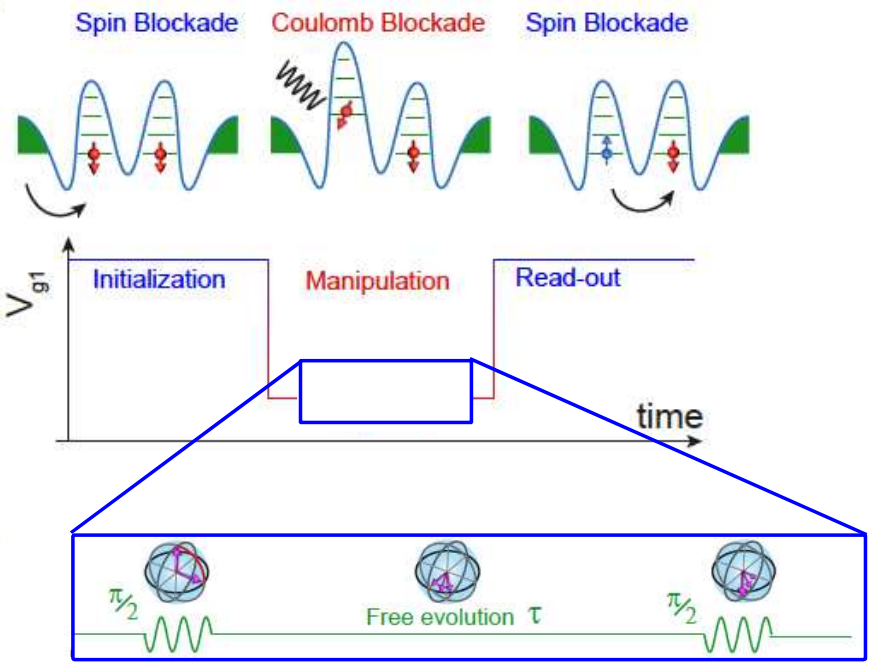
SI QUANTUM ELECTRONICS

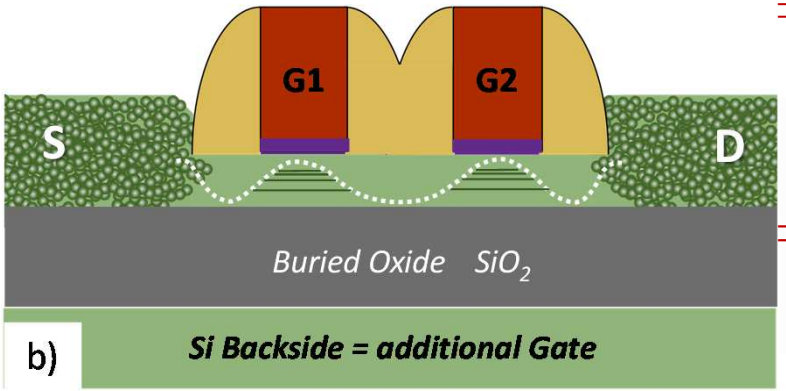


FIRST QUBIT ON SI ON 300MM; BASED ON FDSOI 28NM FLOW



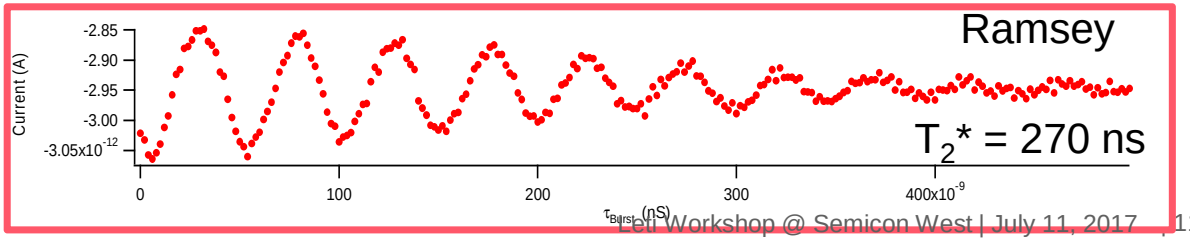






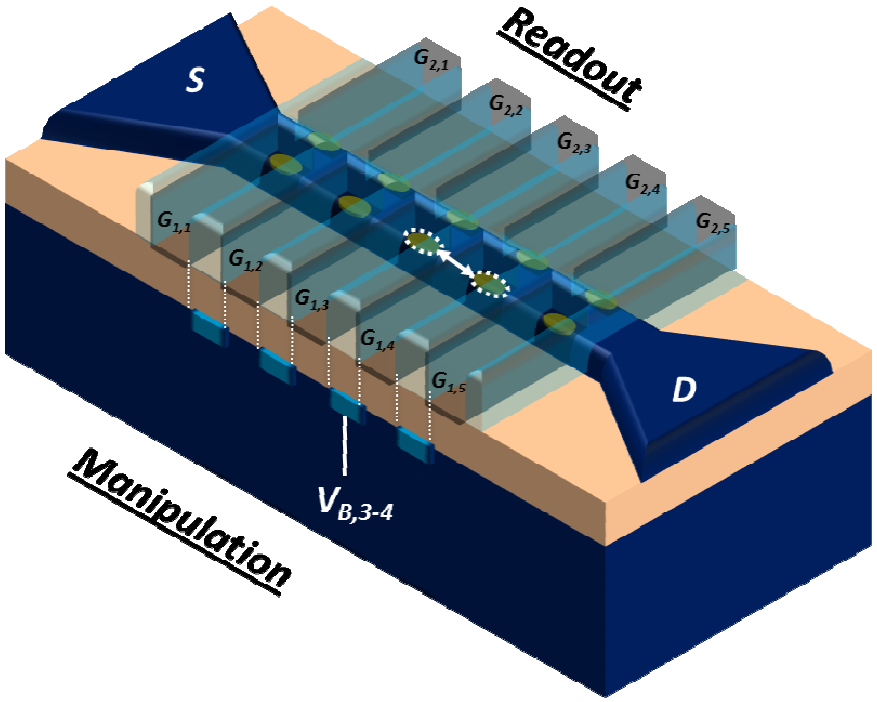
⇒ **Two QDs in series** coupled by tunnel junction

⇒ **Quantization** of the energy levels at low T



TOWARDS A REAL MULTI-QUANTUM BIT SYSTEM ON SI

Near-term:



- Pairs of **split-gates over a single Si Nanowire**
- **Spacing 40nm** or lower
- One side for data Qubits, other side for **readout via reflectometry**
- **Tunable nearest neighbor coupling** via (local) ground plane defined under the BOx

CONCLUSIONS

- Identifying the core challenges to break the barriers
- Combine technologies and architectures to improve systems
- Leti is continuing its disruptive approach looking for new paths to construct the computing roadmap future