

A decorative pattern of small, light gray dots arranged in a wavy, horizontal line across the middle of the slide. Some dots are highlighted in green and red.

## NON VOLATILE MEMORY : A WIDE SPECTRUM OF POTENTIAL SOLUTIONS

Etienne NOWAK, Head of Advanced Memory Lab  
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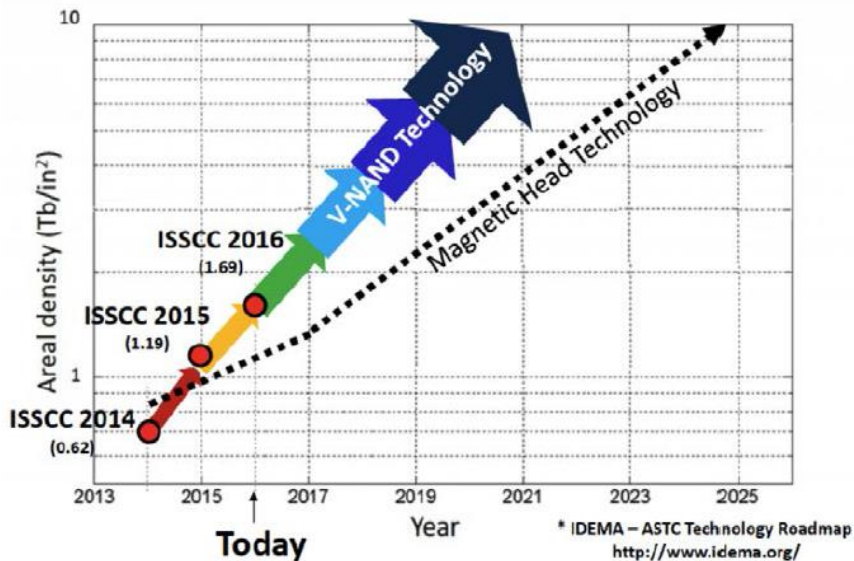
## 3D in Memory Product

What about Emerging Non Volatile Memory ?

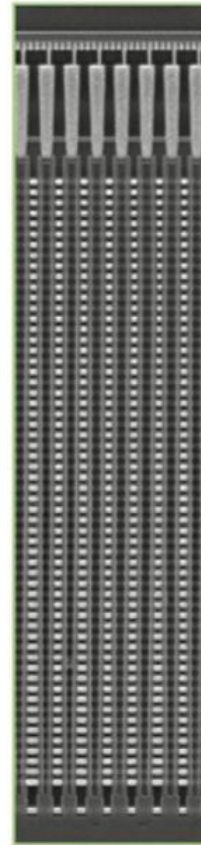
Emerging Non Volatile Memory at Leti

# NAND FLASH IS A 3D TECHNOLOGY

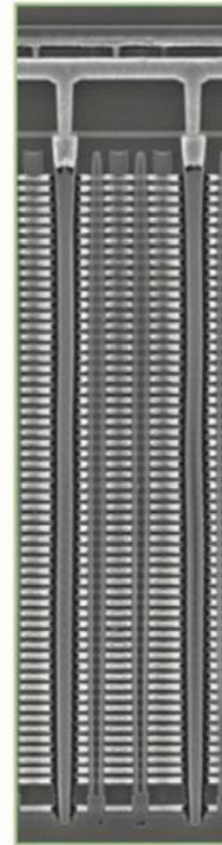
- All NAND memory players have 3D memory product
- NAND Product transition from 1Ynm to 3D (48-64 layers)
- NAND density has surpassed HDD density



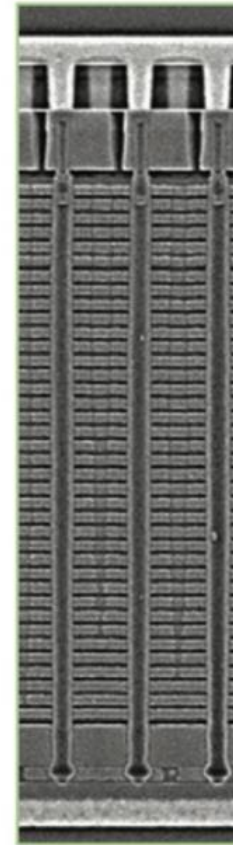
[H. Meinhard, 2016 ECFA Workshop]



Toshiba/SanDisk  
48L 3D NAND



Samsung  
48L 3D V-NAND



Micron/Intel  
32L 3D FG NAND



SK Hynix  
36L 3D U-NAND

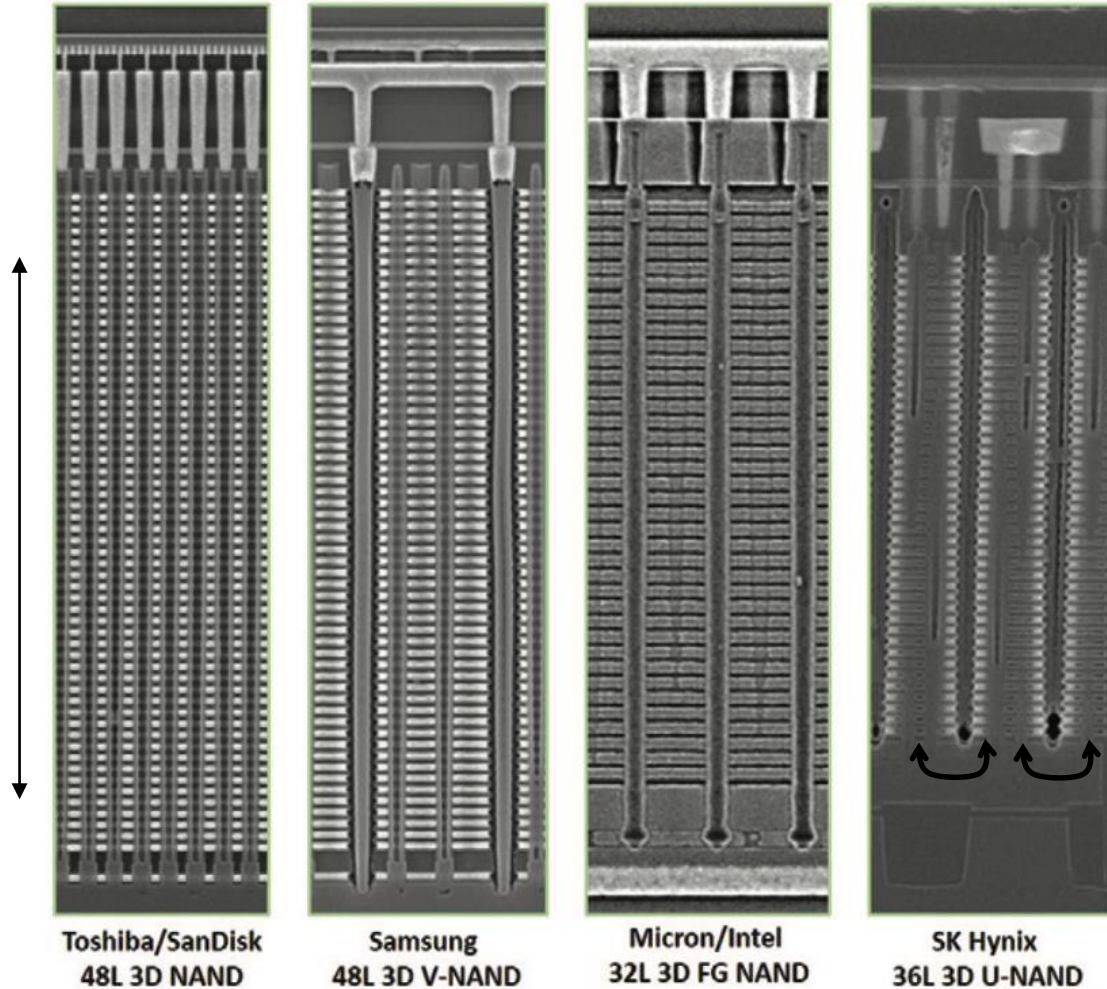
[Techinsight]

Images not at same scale

# NAND FLASH IS A 3D TECHNOLOGY

- Ultimate 3D architecture ?
- Layers are composed of
  - Transistor
  - Memory layers
  - Interconnection

3-4um



[Techinsight]

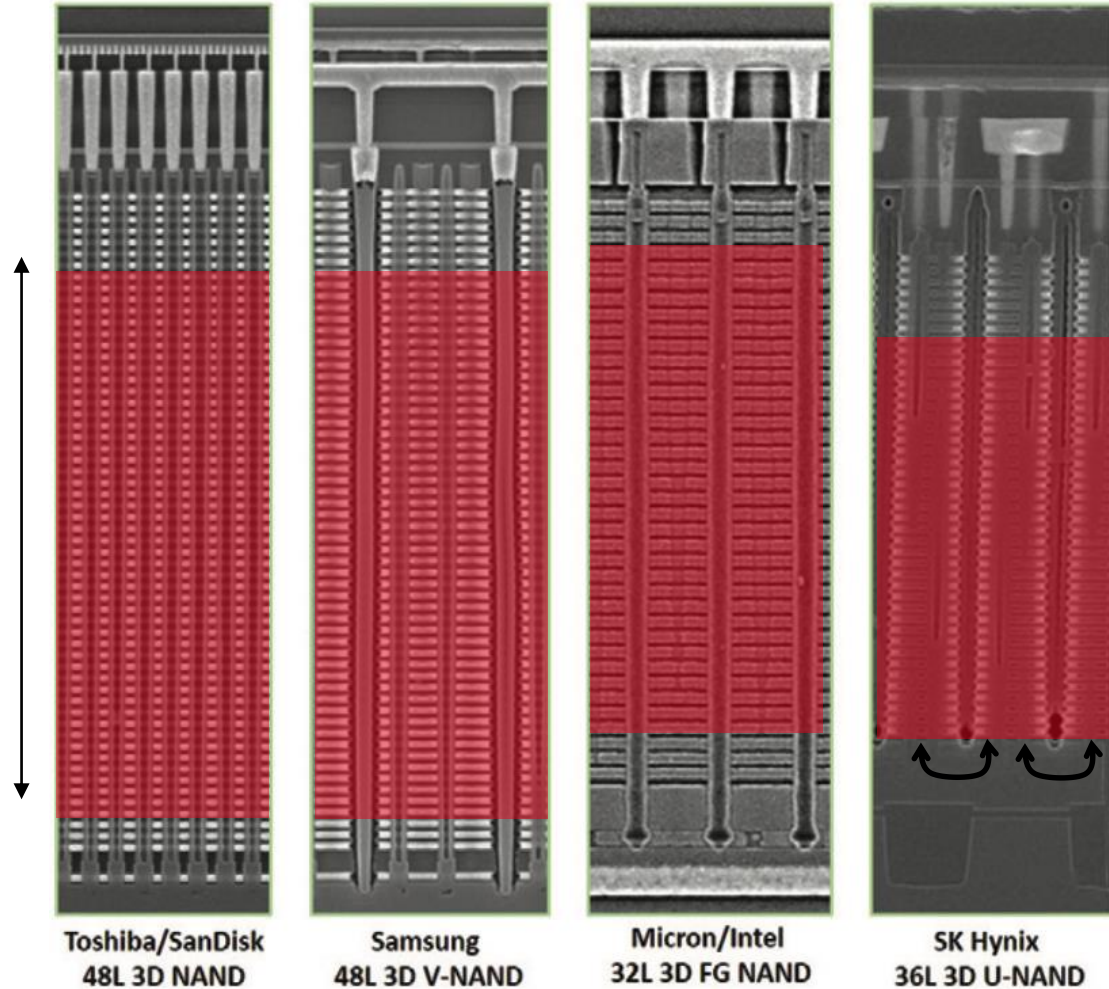
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[Techinsight]

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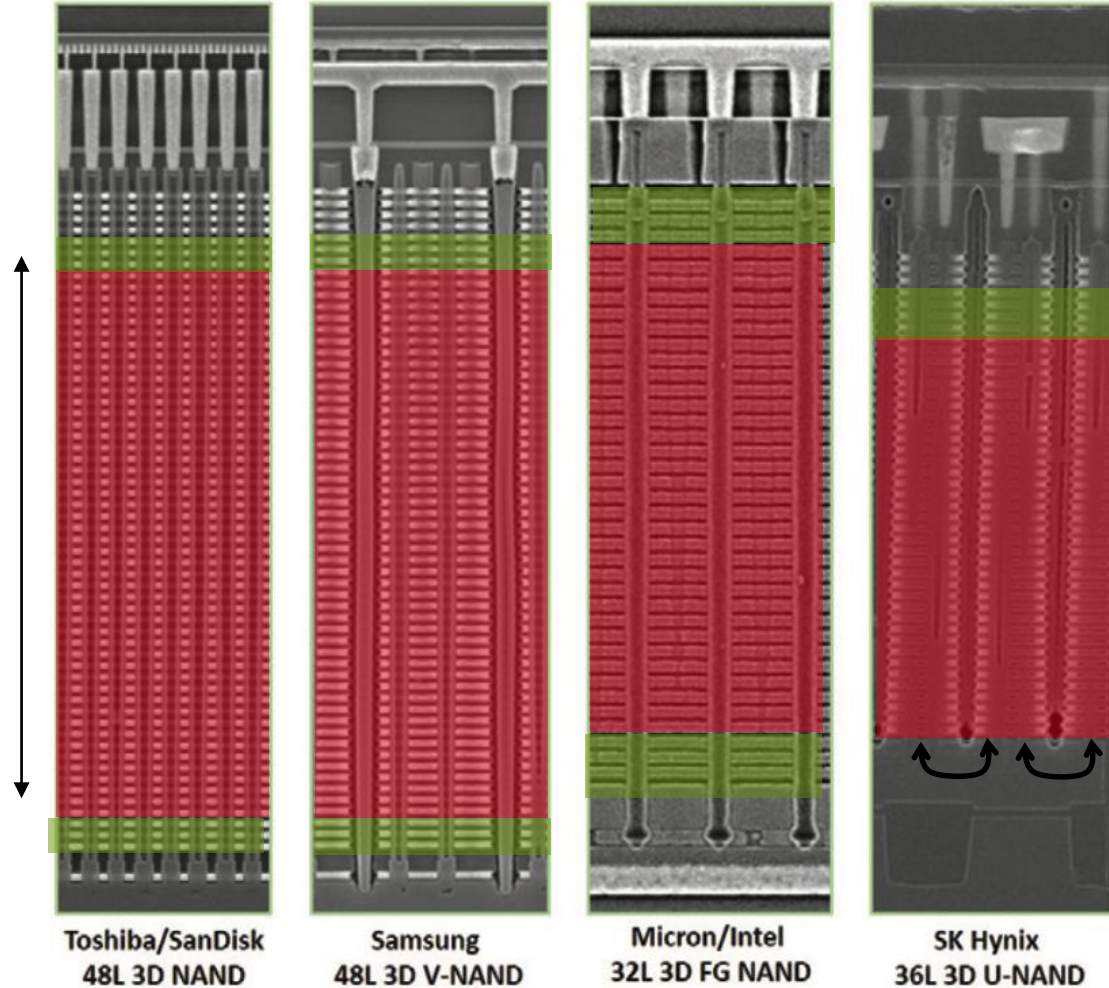
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Memory

Dummies memory

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[Techinsight]

Images not at same scale

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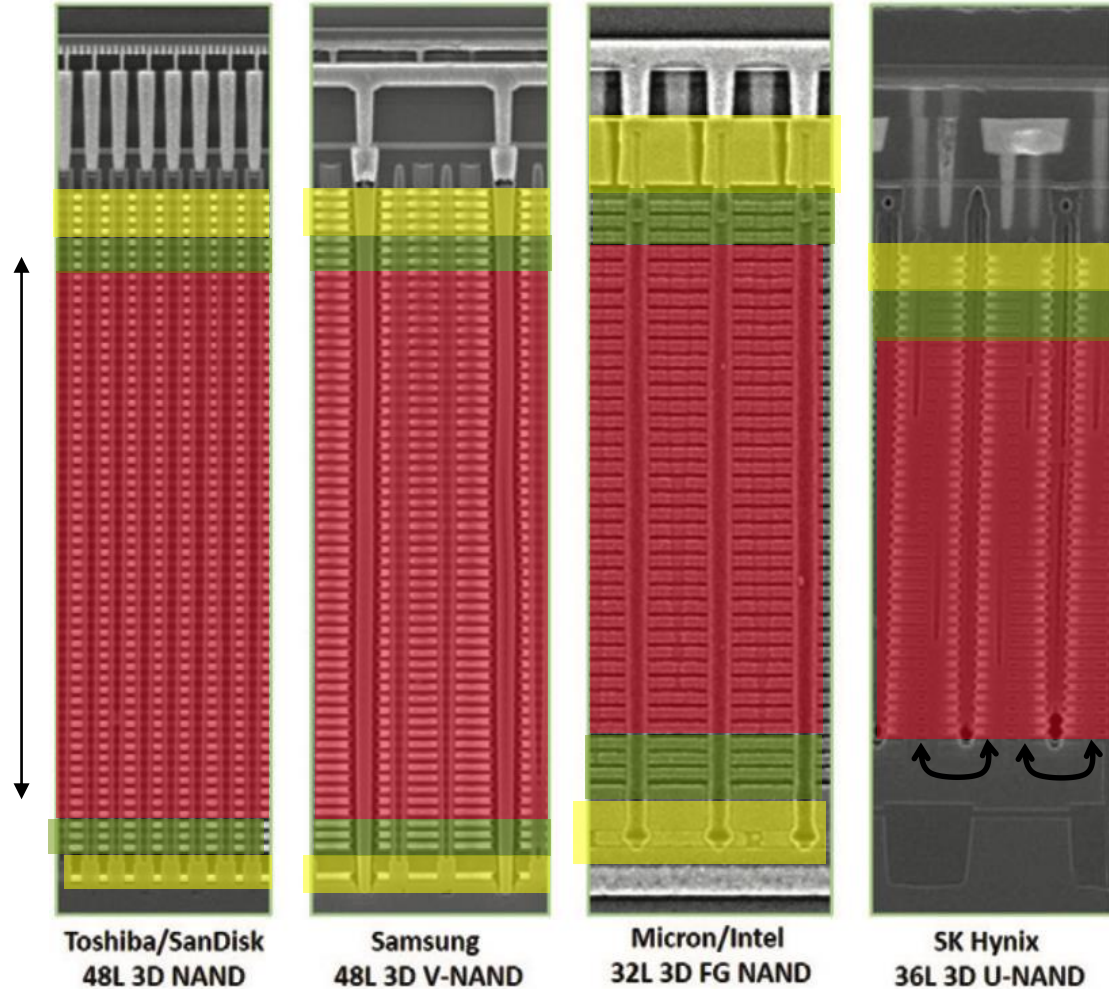
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[Techinsight]

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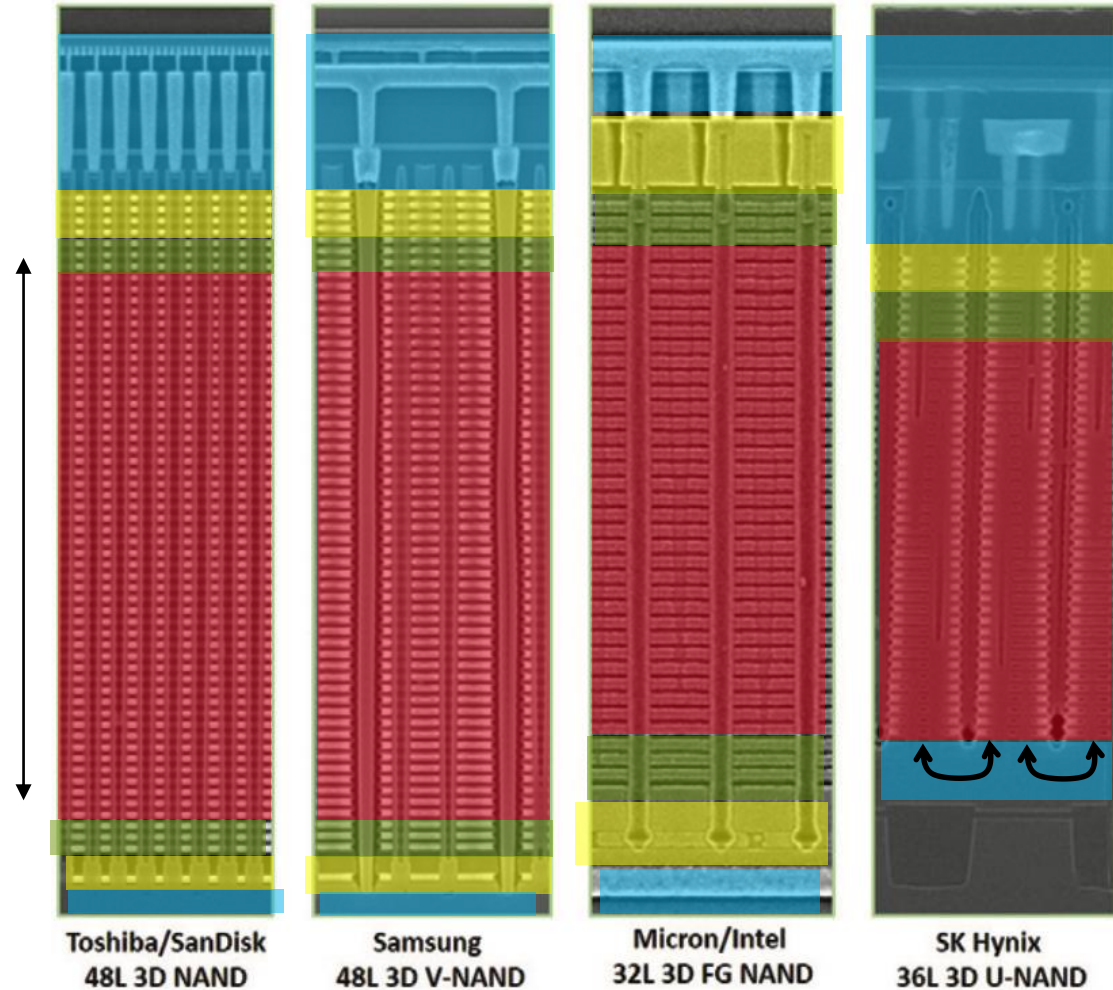
Memory

Dummies memory

Transistors

Interconnection

3-4um



[Techinsight]

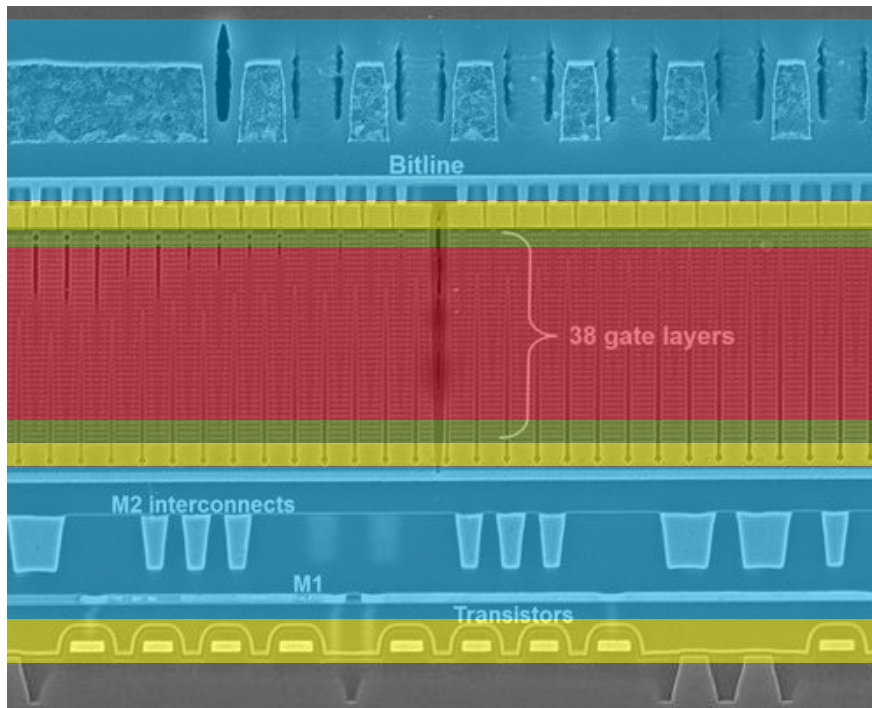
Images not at same scale



## 3D NAND FLASH PERIPHERY

- NAND memory = Periphery + Memory array
- « Periphery under CMOS » improve array efficiency from 70% to 85%

Memory Transistors  
Dummies memory Interconnection



[TechInsights]

Toshiba/SanDisk 128Gb  
Array efficiency ~70%



[Toshiba]

Micron Intel 256Gb  
Array efficiency = 85%

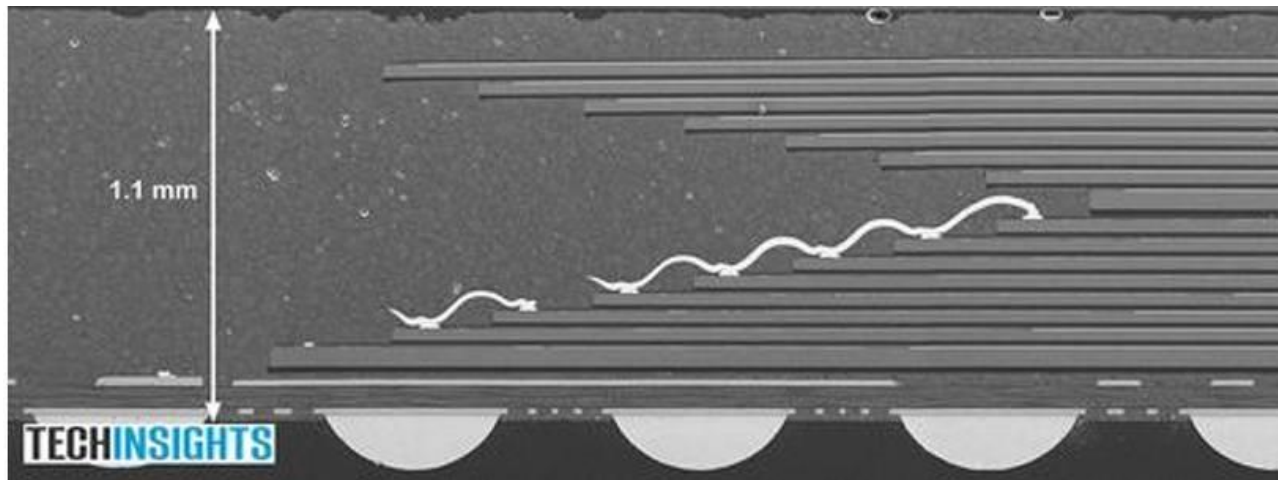


[Micron]

## TYPICAL NAND PACKAGE

- Thinned die that are wire bonded
- Flash has high latency (10's of us)

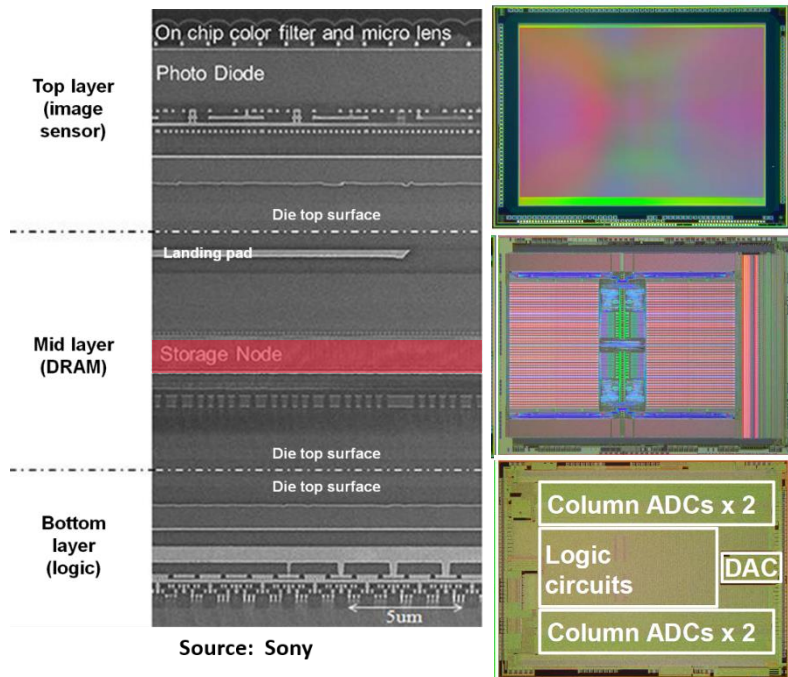
16 Stacked Samsung 48L V-NAND Dies



[TechInsights]

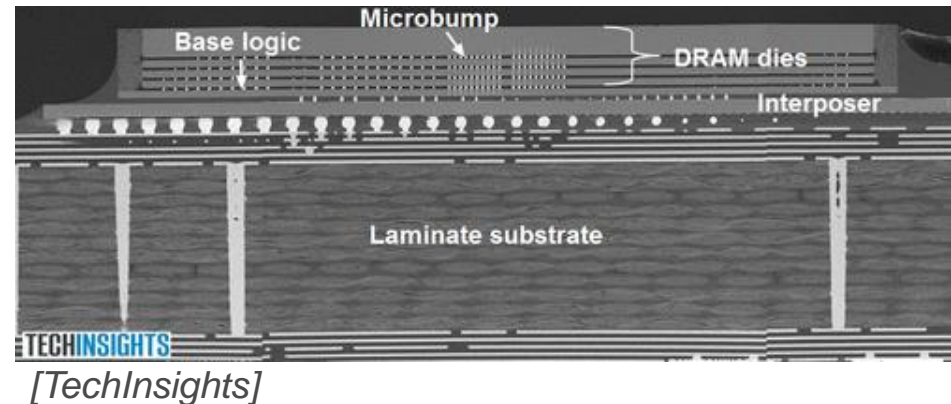
## DRAM AS A COMPLEMENTARY APPROACH OF 3D

- DRAM continue « classical scaling » but used advanced packaging (TSV/ Micro bump)
- DRAM has a low latency (< 100's ns)



[T. Haruta, ISSCC 2017]

[AMD/Hynix] HBM assembly  
Radeon Fury X



3D in Standalone memory

 **What about Emerging Non Volatile Memory ?**

**Emerging Non Volatile Memory at Leti**

## GENERAL MARKET TREND FOR EMERGING NVM

- **Scaling at constant performances**
  - Density
  - Latency
- ➔ **Higher Density or Speed**



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**NAND**  
**DRAM**



## GENERAL MARKET TREND FOR EMERGING NVM

- **Scaling at constant performances**
  - Density
  - Latency
- ➔ **Higher Density or Speed**
- **Low/No energy consumption**
  - Cost of Si ownership due to power (Server)
  - Battery based system (IoT/VR/AR)
- ➔ **Deeper integration of Non Volatile Memory in computing**
- **New Market forces**
  - Deep Learning / Artificial Intelligence
- ➔ **Blurred Computation/Memory frontier**

**NAND**  
**DRAM**



## 2016 MEMORY MARKET DIRECTION

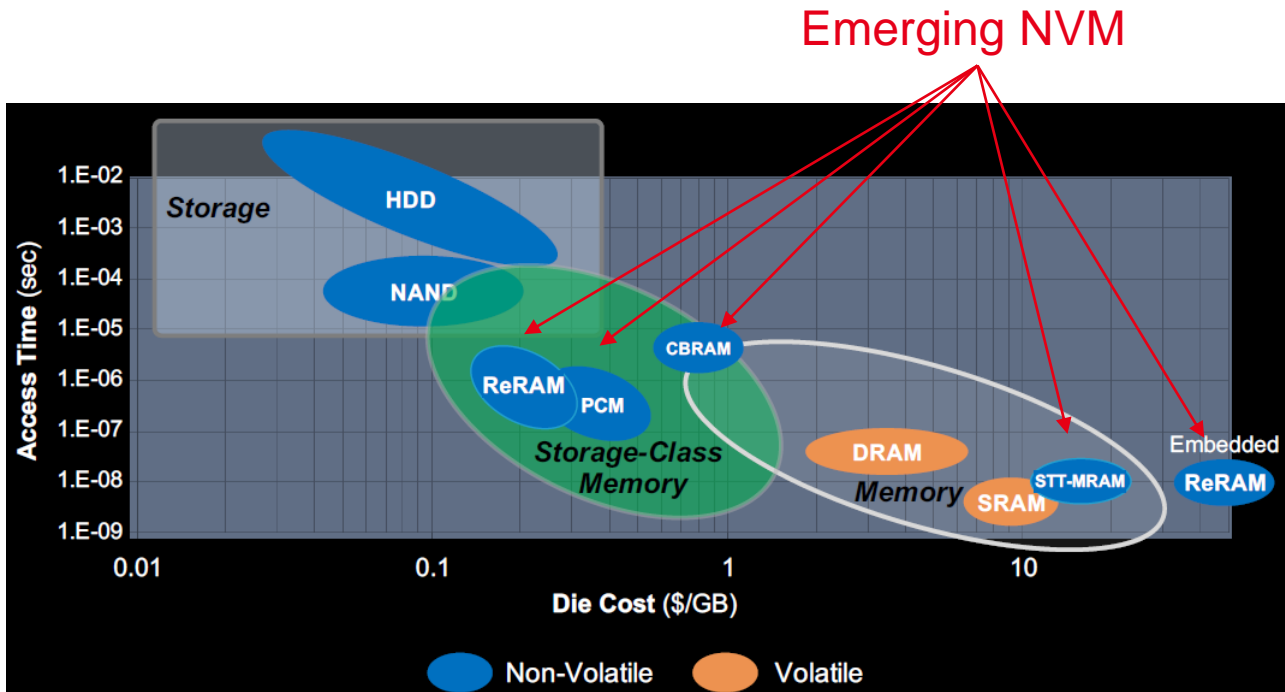
- **PCM revival**
  - Intel/Micron : 3D XPoint 128Gb product
  - ST : 28nm announced
- **MRAM confirmation**
  - Everspin : 256Mb product (1Gb announced)
  - GF : embedded on 22nm
  - Samsung : embedded on 28nm
- **OxRAM/CBRAM continue**
  - Panasonic 0,18um product
  - UMC : 40nm announced
  - Adesto: 512kb product
  - Crossbar/SMIC : 40nm announced
- **FeRAM**
- **Mott memory, ...**

→ All emerging memories are **going to market**

→ Emerging memories are **complementary, no clear winner**

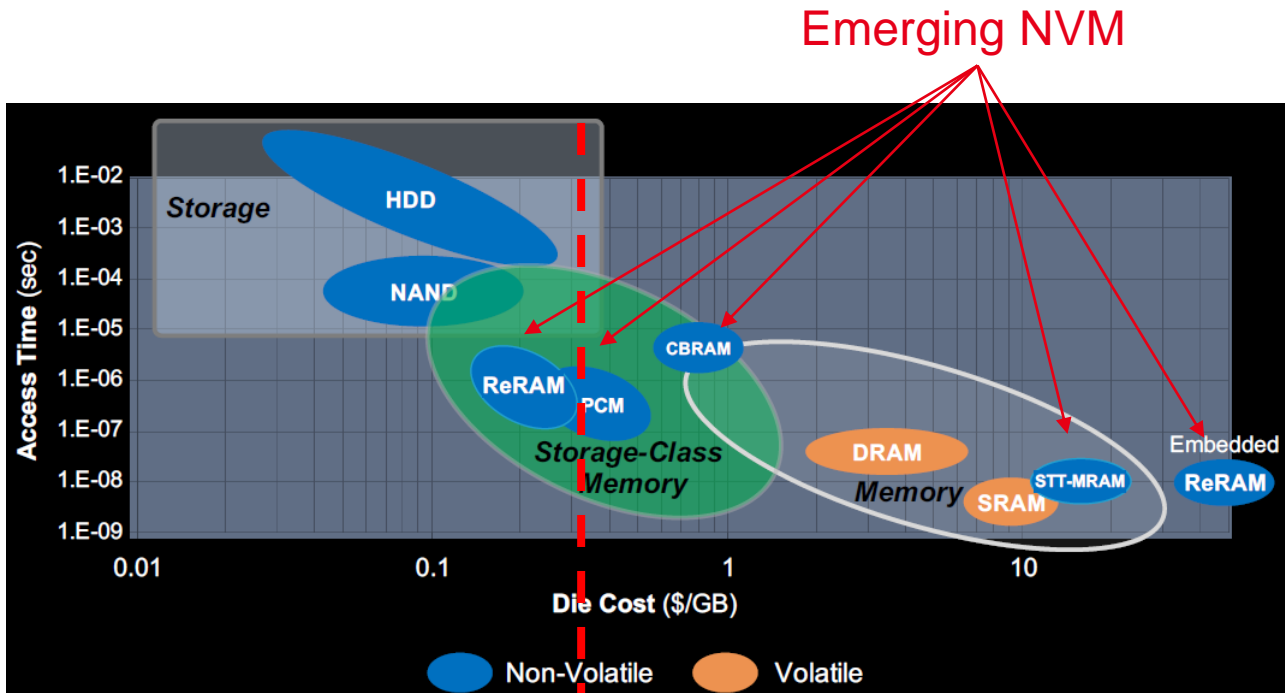


# 2016 MEMORY HIERARCHY



[Siva Sivaram, Western Digital, Flash memory summit 2016]

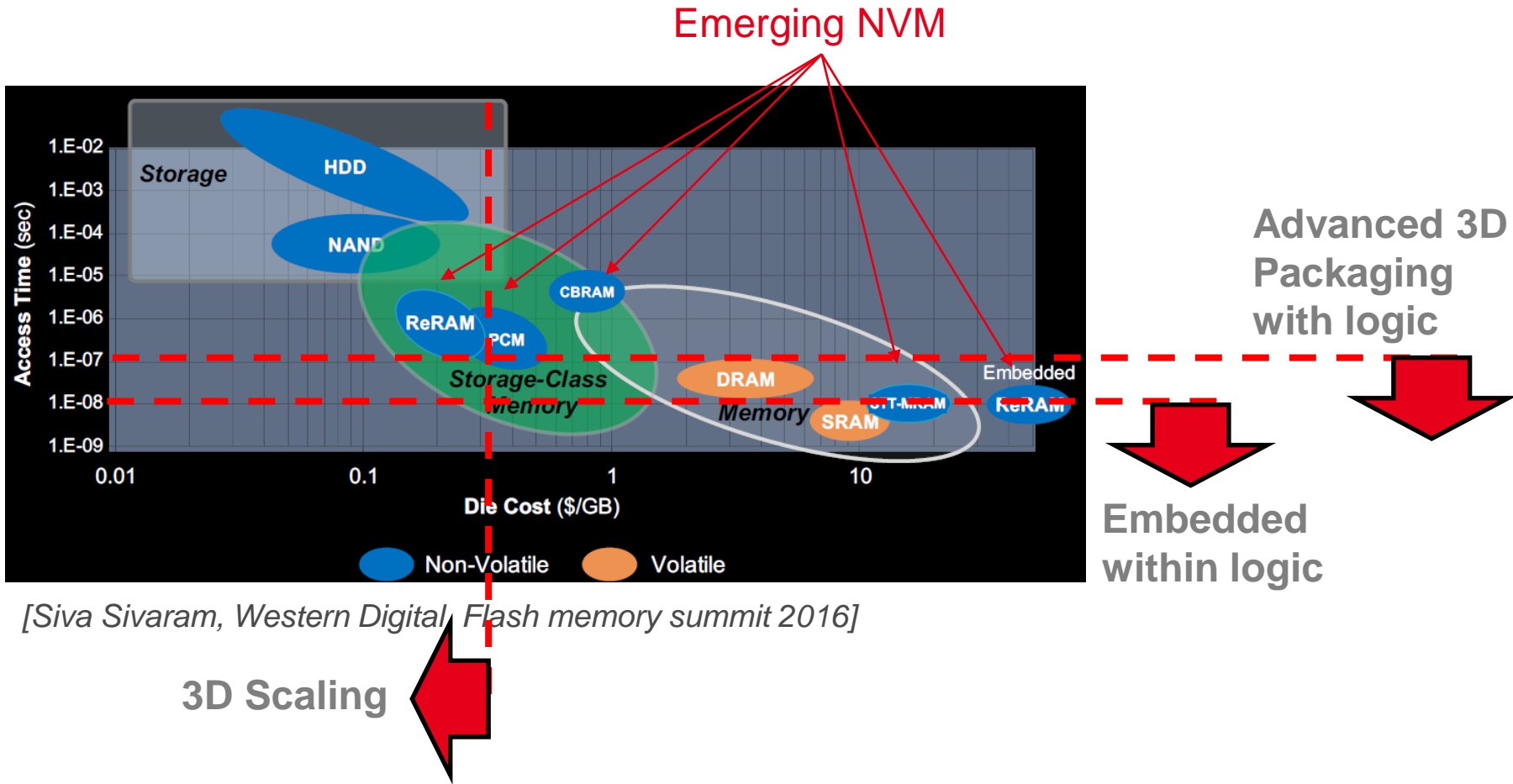
# 2016 MEMORY HIERARCHY



[Siva Sivaram, Western Digital Flash memory summit 2016]

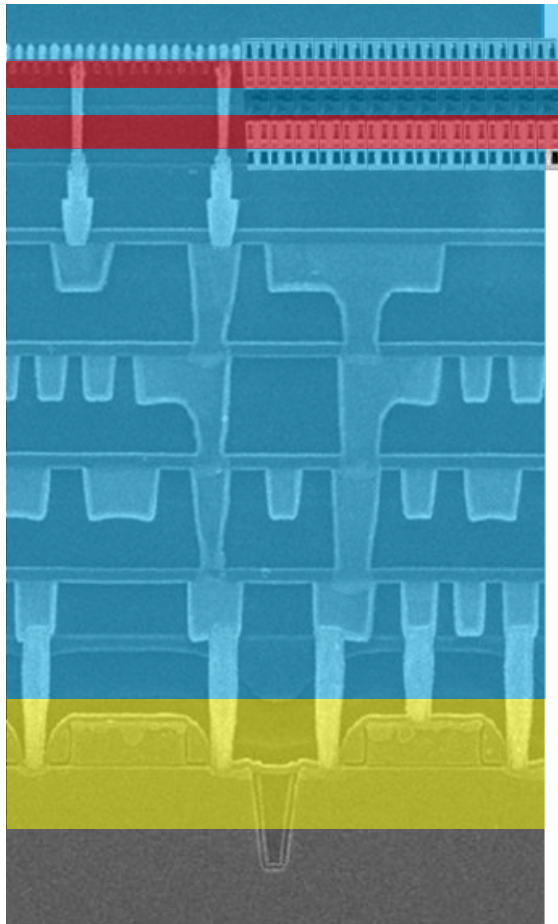
3D Scaling

# 2016 MEMORY HIERARCHY



## « EMERGING NVM » IN PRODUCTION INTEL/MICRON 3DXPOINT

- 2 memory layers above CMOS
- NVM Memory layers above CMOS (91% Array efficiency)

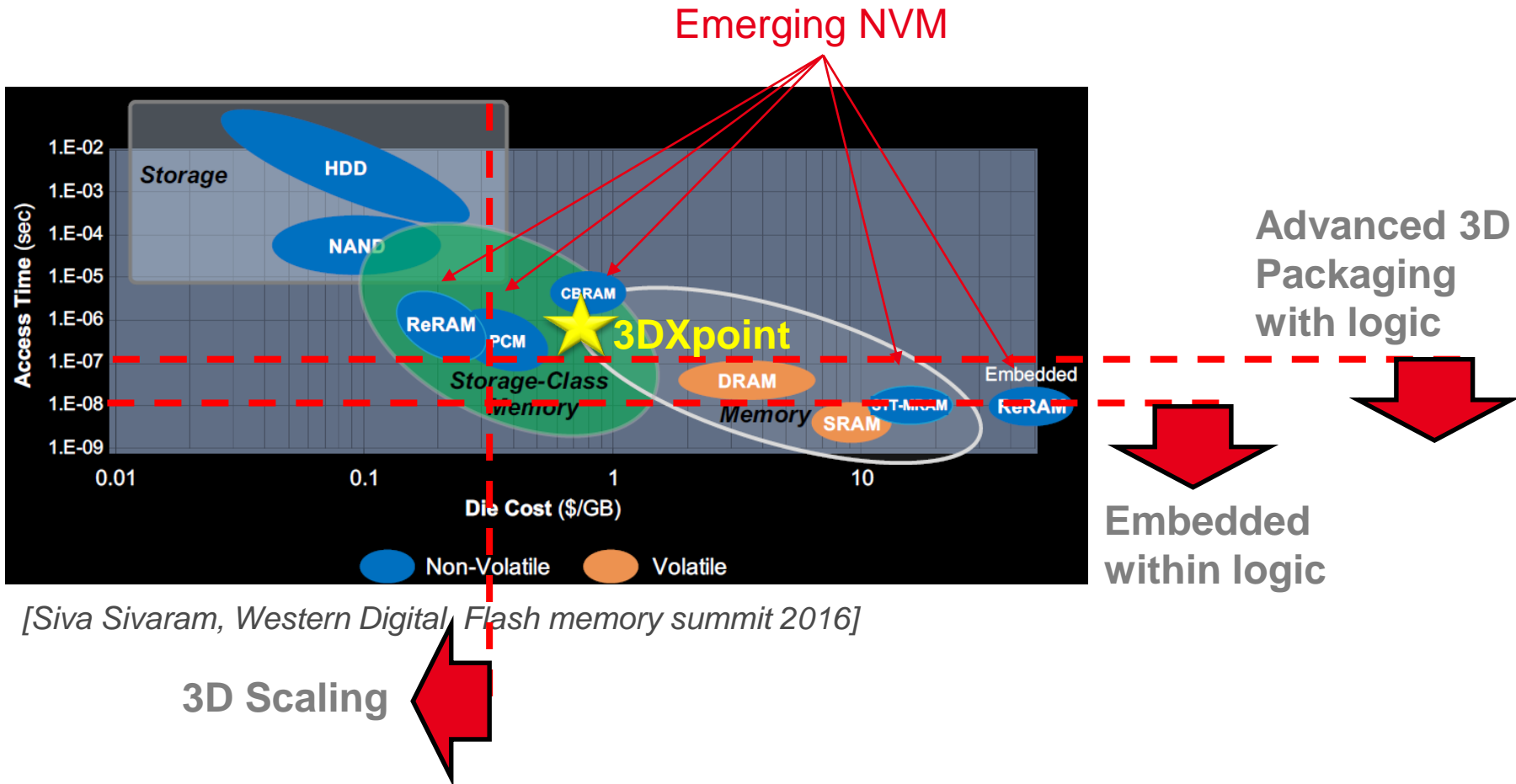


[composed from TechInsights images]

Memory  
Transistors  
Interconnection



# 2016 MEMORY HIERARCHY



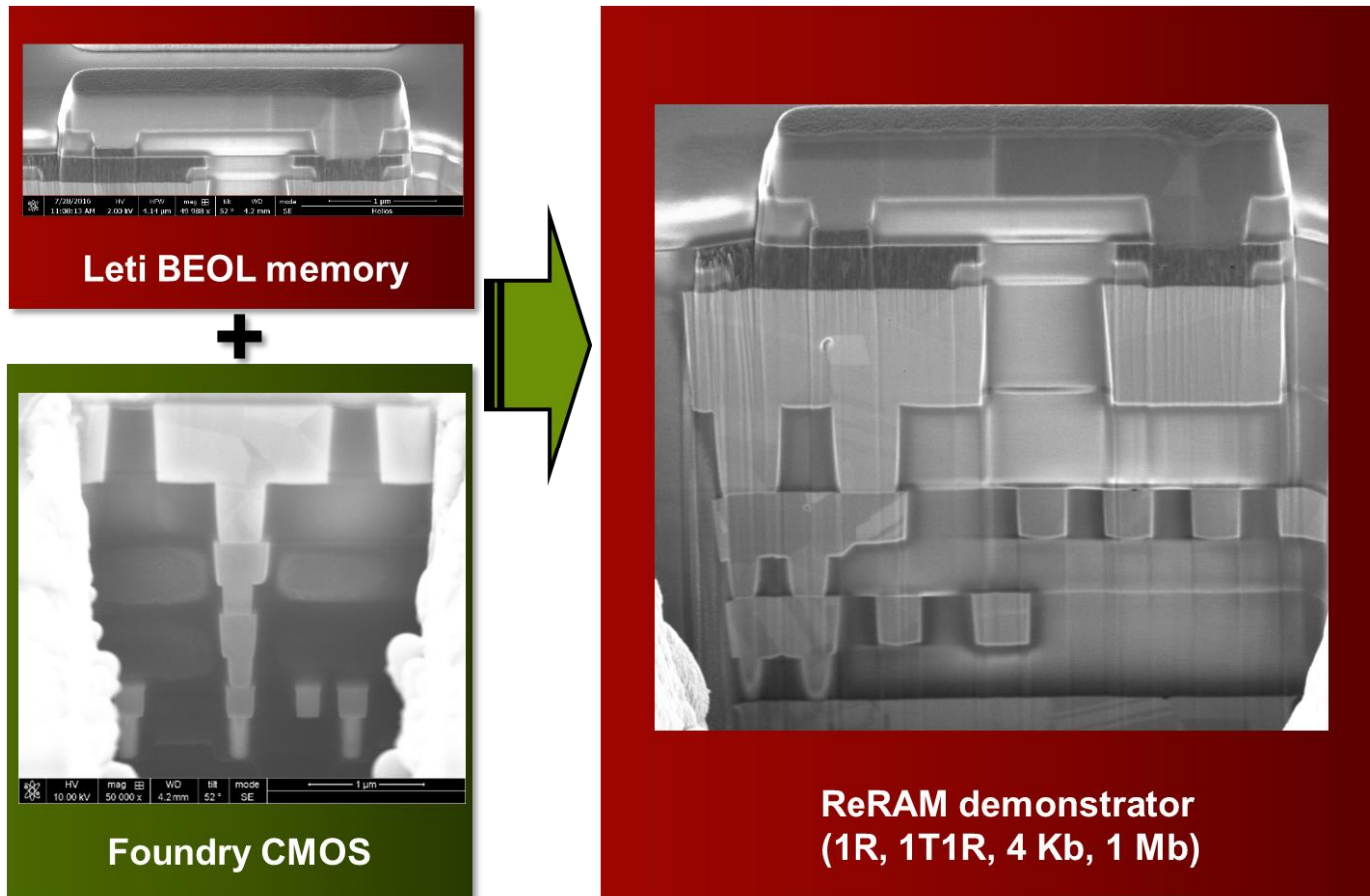
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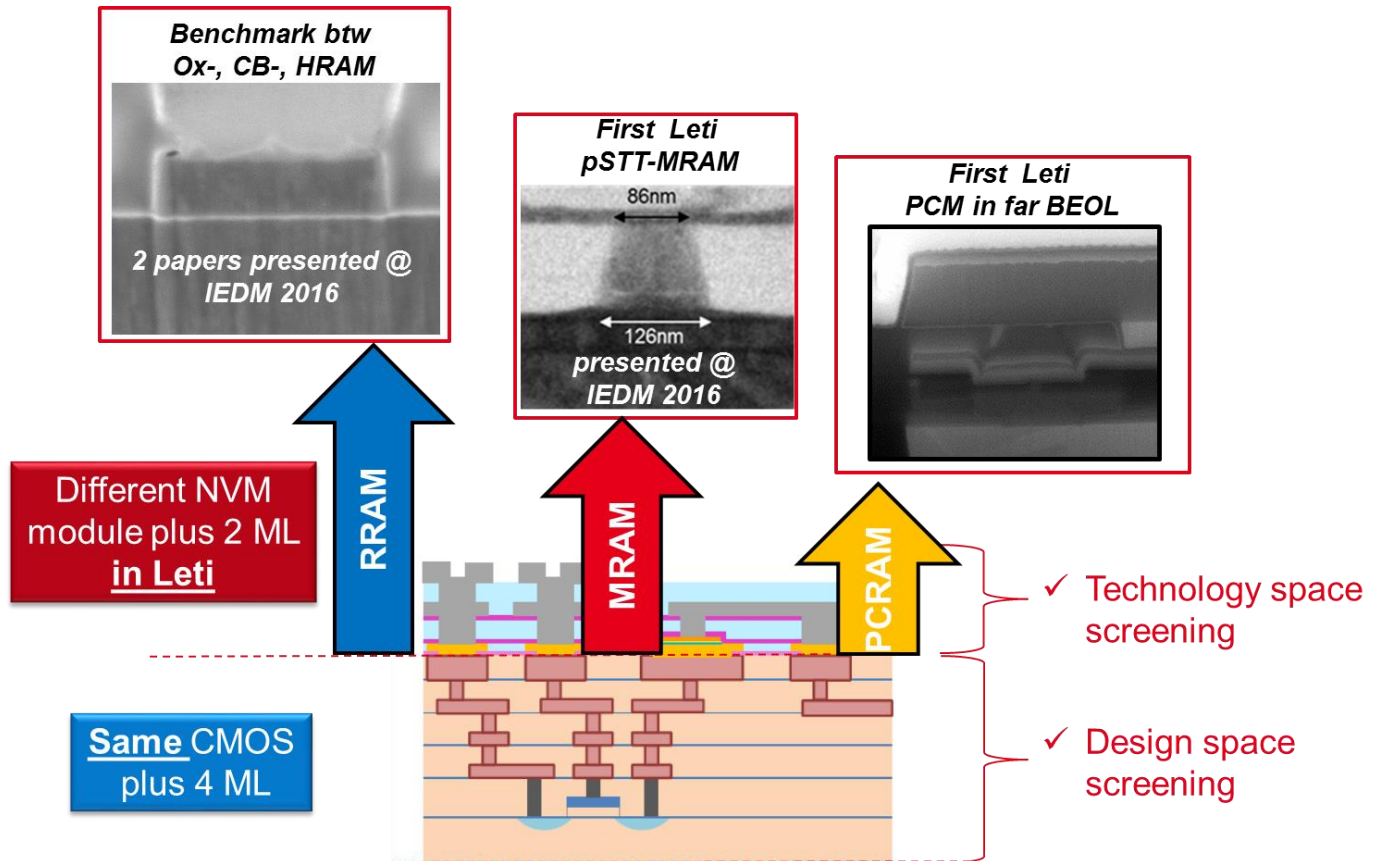
# LETI TECHNOLOGY SOLUTION FOR NVM ASSESS TECHNOLOGY ON THE SAME PLATFORM

- MAD (Memory Advanced Demonstrators) test vehicle allowed to compare different technology on the same demonstrator



## 2016 LETI NVM ACHIEVEMENTS

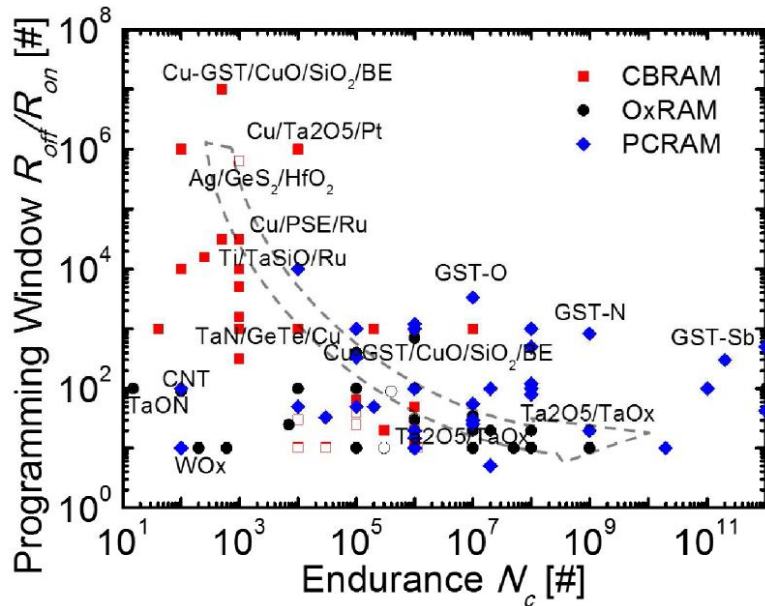
- Test Vehicle MAD operational with most emerging memory integrated
- ➔ Leti knowledge upgraded from single cell to matrix and complex design while continuing integration of new materials





# LETI NVM PERFORMANCES ASSESSMENT

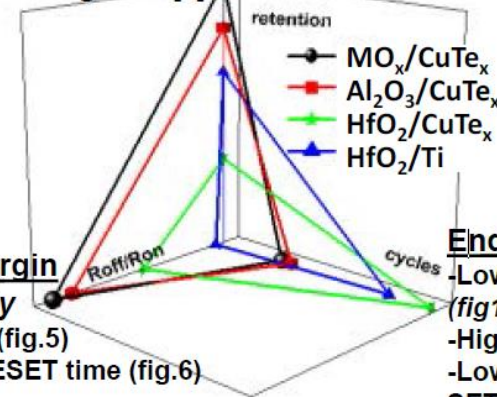
- General tradeoff between endurance, retention and window margin trade-off is observed
- Emerging memories are complementary with no clear winner



[L. Perniola, IMW 2016]

## Retention - Embedded

- High ion migration barrier  $E_a$  (fig.18)
- Large WM [5]



## Window Margin

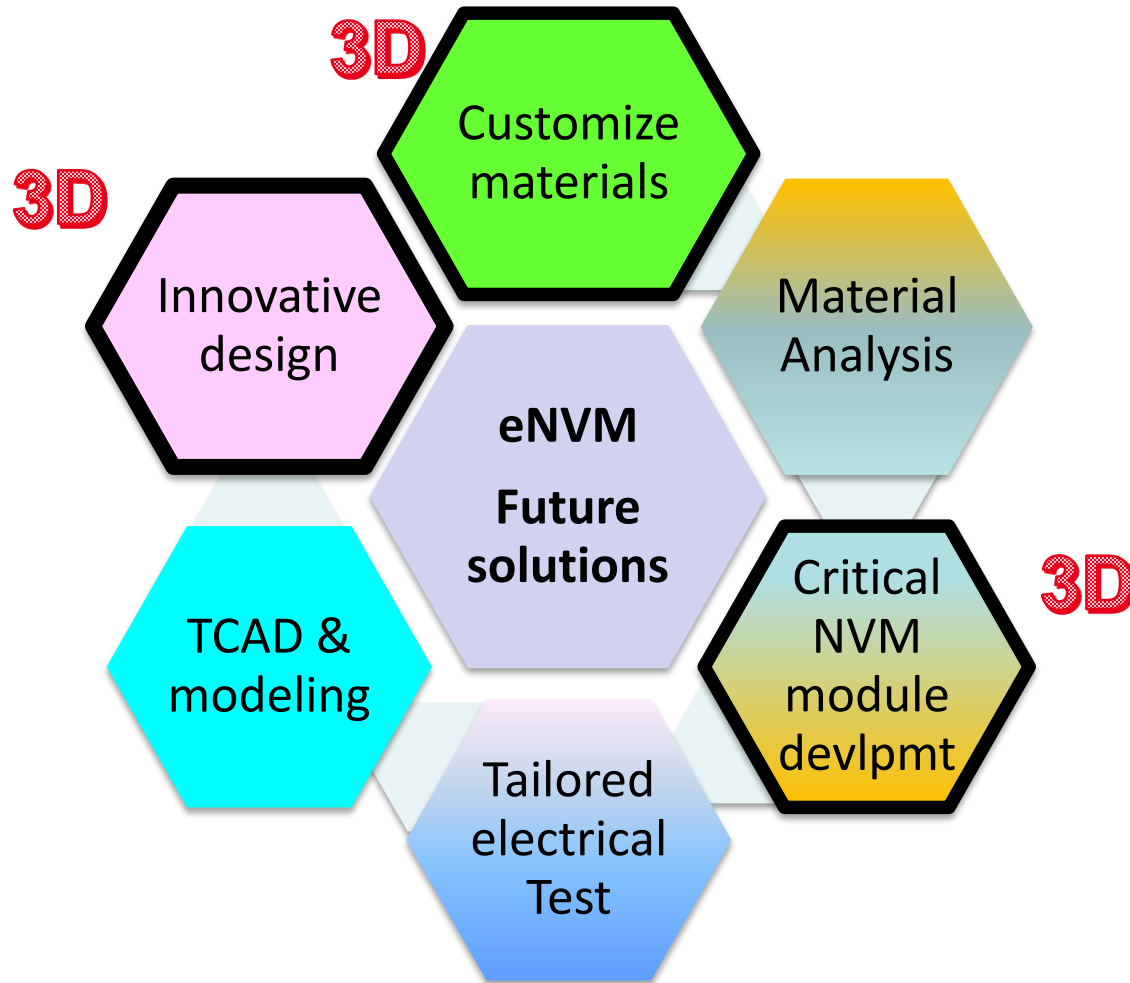
- High density
- Optimized  $I_c$  (fig.5)
- Long SET RESET time (fig.6)

## Endurance - Storage class

- Low ion migration barrier  $E_a$  (fig.18)
- High hopping distance  $d_h$
- Low Window margin (slight SET RESET conditions) (fig.8)

[C. Nail, IEDM 2016]

## What does 3D change for NVM in Leti



- A wide toolbox enables **customized** research with **our partners** and a **benchmark** between different technological solutions

# Conclusion

## Conclusion

- **Memories are 3D**
  - **3D technologies are used in Flash for Cost (Highest Density)**
  - **3D packaging are used in DRAM for Performance (Latency)**
- **Emerging NVM performance spaces are at the limits between 3D technology and 3D packaging**
- **Emerging NVM are complementary with no clear winner**
- **NVM consist of “Memory + CMOS+ interconnect” layers at state of the art lithographic pitch**
- **Leti technology able to assess most emerging NVM technology in order to choose the right “3D” that associated with it**

Thank you for your attention



**LETI MEMORY WORKSHOP**

**MEMORY OF THE FUTURE  
FROM CONCEPT TO MARKET**

TUESDAY, JUNE 27, 2017  
MINATEC, GRENoble

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