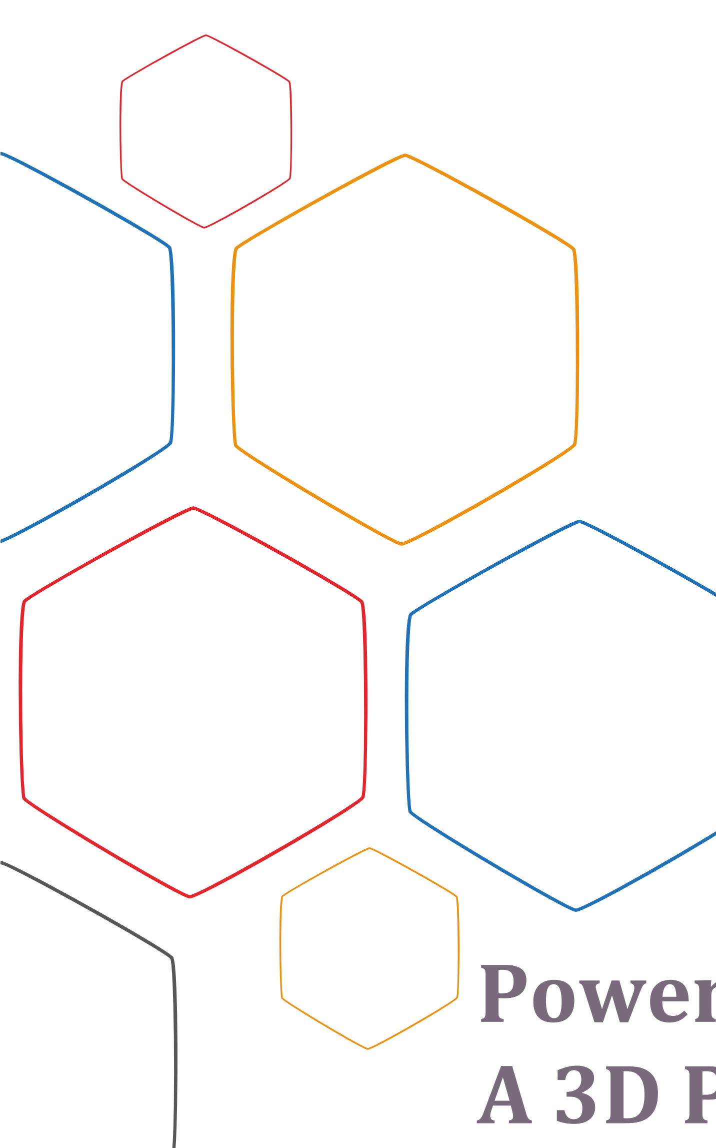
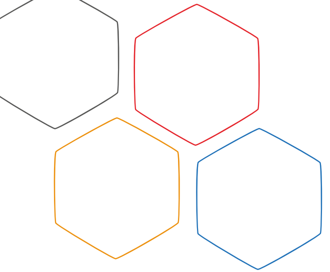


Power, Heat, Reliability: A 3D Physical Design Perspective

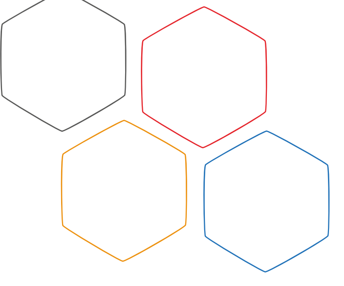
Dr. Aida Todri-Sanial
CNRS-LIRMM/University of Montpellier



Introduction

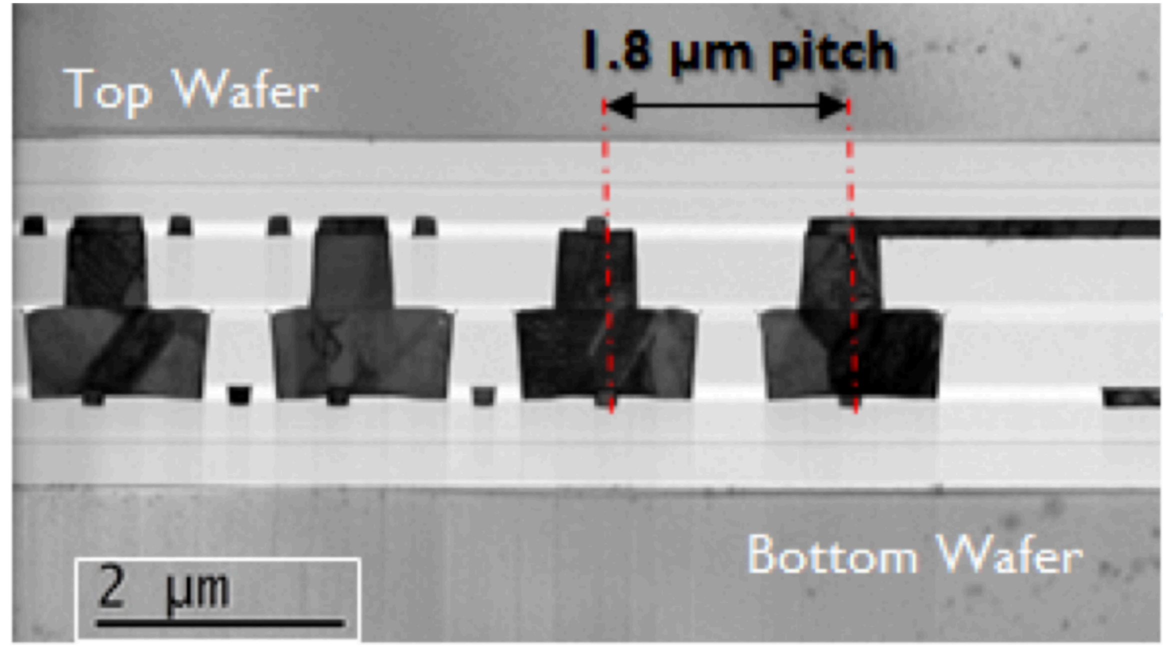
- ❑ Affiliations:
  - ❑ Research Scientist, CNRS-LIRMM, France
    - ❑ Group leader: Integration and Design of Energy Aware Integrated Circuits (IDEA)
  - ❑ Visiting Research Fellow, Cambridge Graphene Center, University of Cambridge, UK
- ❑ Research Interest:
  - ❑ Modeling and simulation of nanoscale devices & interconnects
  - ❑ Emerging integrated circuits and system technologies
    - ❑ Advanced CMOS (<10nm) and beyond (graphene, carbon nanotubes, spintronics, etc.)
    - ❑ 1D and 2D materials
    - ❑ TSV-based 3D and monolithic 3D integration
  - ❑ Biomedical sensors, wearable and implantable devices for health

CNRS-LIRMM/
University of Montpellier



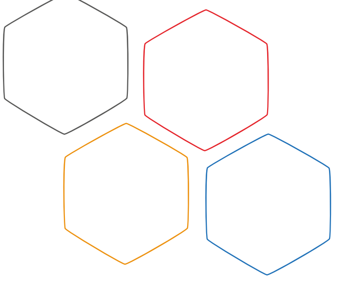
Making Headlines

Imec and EVG have demonstrated 1.8μm pitch overlay accuracy for wafer-to-wafer bonding.



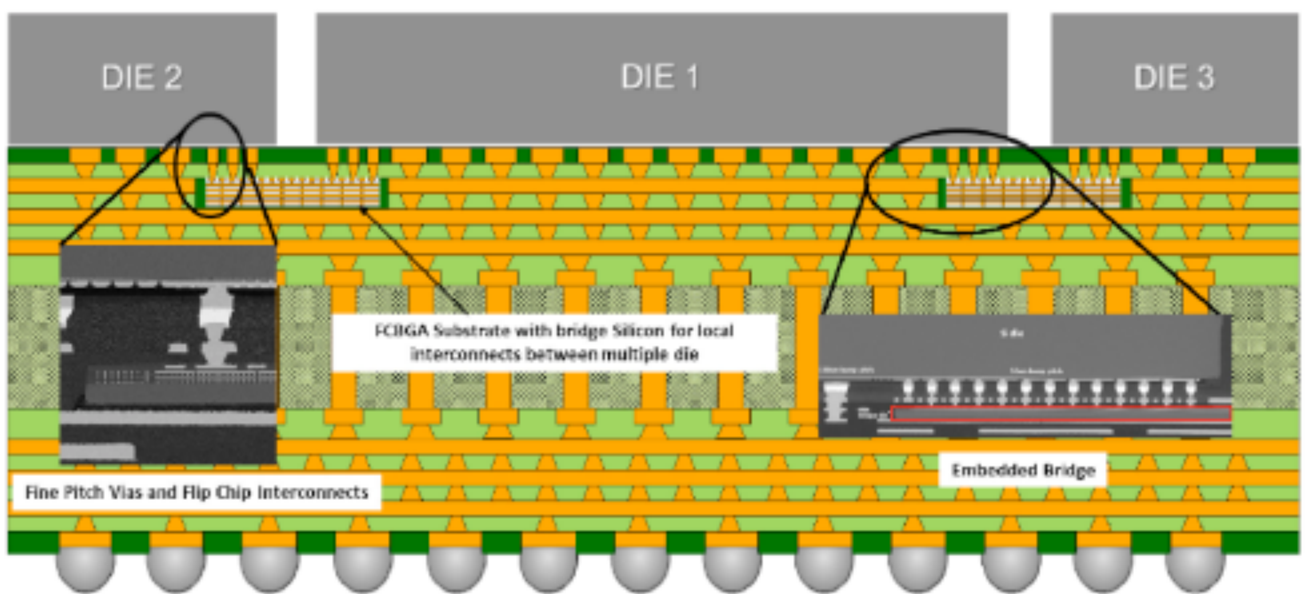
ISSCC 2017

Wafer-to-wafer bonding is a promising technique for enabling high-density integration of future ICs through 3D integration.

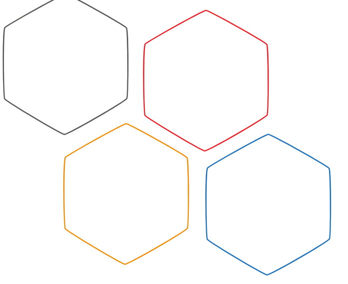


Making Headlines

ISSCC 2017 (Feb 7th, 2017): Intels's Stratix X FPGA



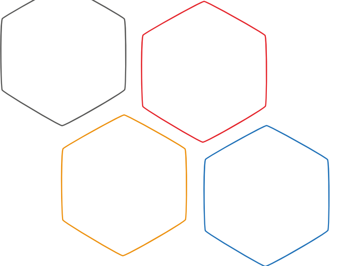
55 micron micro-bumps and 100+ micron flip-chip bumps to support up to 24 transceiver channels with 96 I/Os each. They deliver 2 Gbits/second/pin at 1.2 pJ/bit/die using a proprietary protocol.



Making Headlines

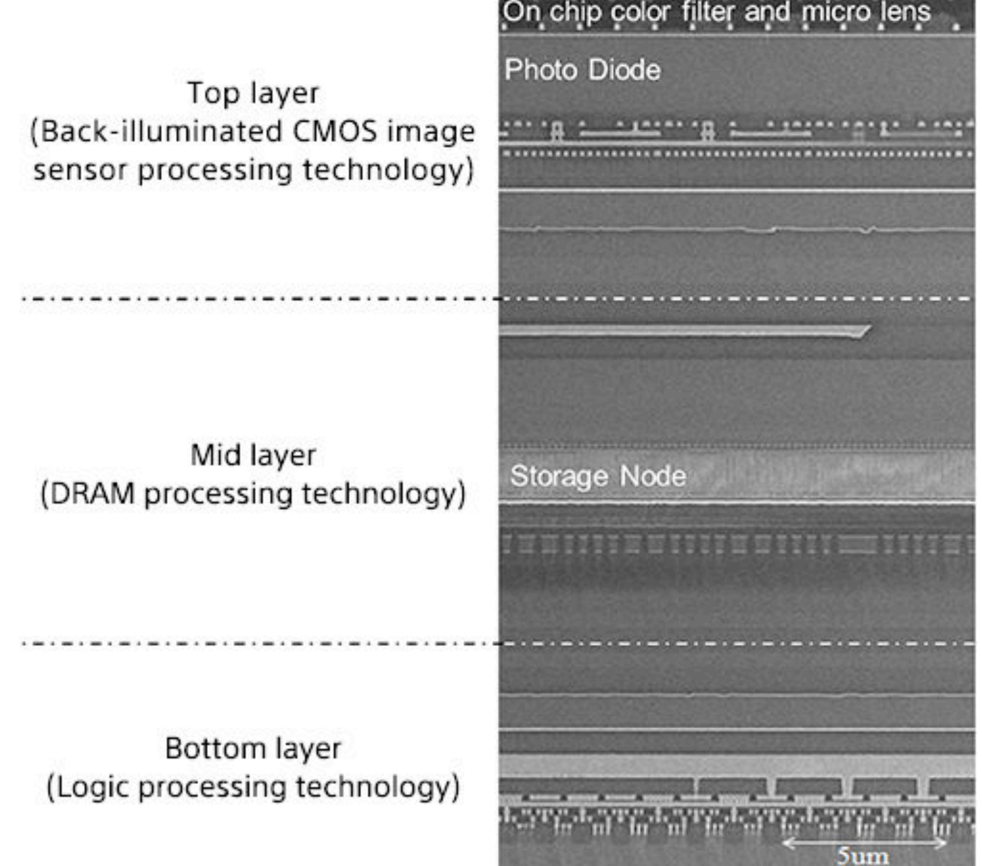
ISSCC 2017: Toshiba and Western Digital **first-ever 512 gigabit 64-layer 3D NAND Flash chip**

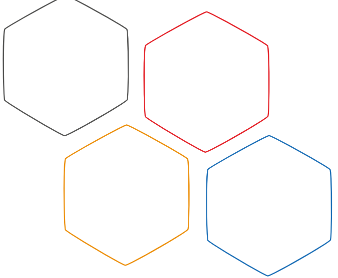
Bit Cost Scalable



Making Headlines

ISSCC 2017: Sony announces the first three-layer stacked image sensor





Making Headlines

2017 Symposia on VLSI Technology and Circuits

T6-4 - 9:45

First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-Layer Contacts, V. Deshpande*, H. Hahn*, E. O'Connor*, Y. Baumgartner*, M. Sousa*, D. Caimi*, H. Boutry**, J. Widiez**, L. Brévard**, C. Le Royer**, M. Vinet**, J. Fompeyrine* and L. Czornomaz*, *IBM Research, Switzerland and **CEA-LETI, France

We demonstrate, for the first time, the 3D Monolithic (3DM) integration of In0.53GaAs nFETs on FDSOI Si CMOS featuring short-channel Replacement Metal Gate (RMG) InGaAs n-FinFETs on the top layer and Gate-First Si CMOS on the bottom layer with TiN/W inter-layer contacts. State-of-the-art device integration is achieved with the top layer InGaAs utilizing raised source drain (RSD) and the bottom layer CMOS having Si RSD for nFETs, SiGe RSD for pFETs, implants, silicide and TiN/W plug contacts. The top layer InGaAs n-FinFETs are scaled down to L_g =25 nm and both the Si nFETs and pFETs in the bottom layer are scaled down to L_g ~15 nm. Finally, utilizing the inter-layer contacts, we demonstrate a densely integrated 3D 6T-SRAM circuit with InGaAs nFETs stacked on top of Si pFETs showing considerable area reduction with respect to a 2D layout.

T17-3 - 16:50

Key Process Steps for High Performance and Reliable 3D Sequential Integration, C.-M. V. Lu*,**, F. Deprat*, C. Fenouillet-Beranger*, P. Batude*, X. Garros*, A. Tsiara*, C. Leroux*, R. Gassilloud*, D. Nouguier**, D. Ney**, X. Federspiel**, P. Besombes*, A. Toffoli*, G. Romano**,*, N. Rambal*, V. Delaye*, D. Barge**, M.-P. Samson**,*, B. Previtali*, C. Tabone*, L. Pasini**,*, L. Brunet*, F. Andrieu*, J. Micoud*, T. Skotnicki** and M. Vinet*, *CEA-LETI and **STMicroelectronics, France

This work provides breakthroughs in key technological modules for high performance and reliable 3D Sequential Integration with intermediate BEOL (iBEOL) in-between tiers. We demonstrate that (i) a high-quality solid phase epitaxy process is possible at 500°C, (ii) TiN native oxide removal prior to poly deposition leads to an improvement in gate stack reliability below 525°C and (iii) state-of-the-art SiOCH ULK in iBEOL is reliable up to 550°C 5h with W metal lines. A process integration is thus proposed to match the process windows of bottom layers (bottom FET and iBEOL) stability and top devices performance and reliability, opening perspectives for a wide range of applications and technologies using 3D Sequential Integration.

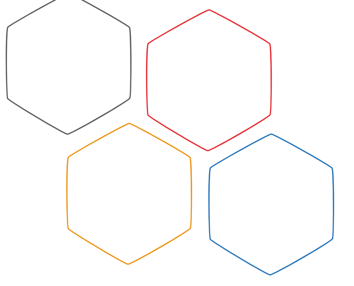
Table 1: Device architecture and ground rules roadmap for logic device technologies. PxxMxx notation refers to Pxx: contacted poly pitch and Mxx: metalx pitch in nm. This shows the technology capability. On top of pitch scaling there are other elements such as cell height, vertical integration, fin depopulation, DTCO contructs, etc define the target area scaling (gates/mm2).

IRDS Report March 2017

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P54M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
	FinFET / FDSOI	FinFET / FDSOI	Lateral Nanowire / FinFET	Vertical Nanowire / Lateral Nanowire	Vertical Nanowire / Monolithic 3D	Vertical Nanowire / Monolithic 3D	Vertical Nanowire / Monolithic 3D
LOGIC DEVICE GROUND RULES							
MPU/SoC Metalx ½ Pitch (nm)[1,2]	28.0	18.0	12.0	10.0	6.0	6.0	6.0
MPU/SoC Metal0/1 ½ Pitch (nm)	28.0	18.0	12.0	10.0	6.0	6.0	6.0
Contacted poly half pitch (nm)	35.0	24.0	21.0	16.0	12.0	12.0	12.0
L_g: Physical Gate Length for HP Logic (nm) [3]	24	18	14	10	10	10	10
L_g: Physical Gate Length for LP Logic (nm)	26	20	16	12	12	12	12
Channel overlap ratio - two-sided	0.80	0.80	0.80	0.80	0.80	0.80	0.80
Spacer width (nm)	12	8	6	5	4	4	4
Contact CD (nm) - finFET, LGAA	22	14	16	12	11	11	11
Device architecture key ground rules							
FinFET Fin Half-pitch (new) =0.75 or 1.0 M0/MI (nm)	21.0	18.0	12.0				
FinFET Fin Width (nm)	8.0	6.0	6.0				
FinFET Fin Height (nm)	42.0	42.0	42.0				
Footprint drive efficiency - finFET	2.19	2.50	3.75				
Lateral GAA Lateral Half-pitch (nm)			12.0	10.0			
Lateral GAA Vertical Half-pitch (nm)			12.0	9.0			
Lateral GAA Diameter (nm)			6.0	6.0			
Footprint drive efficiency - lateral GAA, 3x NWs stacked			2.4	2.8			
Vertical GAA Lateral Half-pitch (nm)				10.0	6.0	6.0	6.0
Vertical GAA Diameter (nm)				6.0	5.0	5.0	5.0
Footprint drive efficiency - vertical GAA, 3x NWs stacked				2.8	3.9	3.9	3.9
Defice effective width - [nm]	92.0	90.0	56.5	56.5	56.5	56.5	56.5
Device lateral half pitch (nm)	21.0	18.0	12.0	10.0	6.0	6.0	6.0
Device width or diameter (nm)	8.0	6.0	6.0	6.0	5.0	5.0	5.0

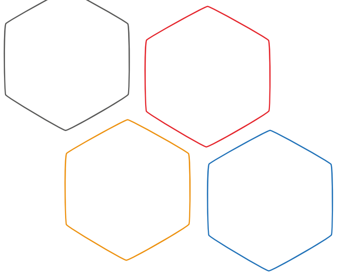
Toward functional scaling

Acronyms used in the table (in order of appearance): FDSOI: Fully-Depleted Silicon-On-Insulator (FDSOI), LGAA: Lateral Gate-All-Around-Device (GAA), VGAA: Vertical GAA, M3D: Monolithic-3D.

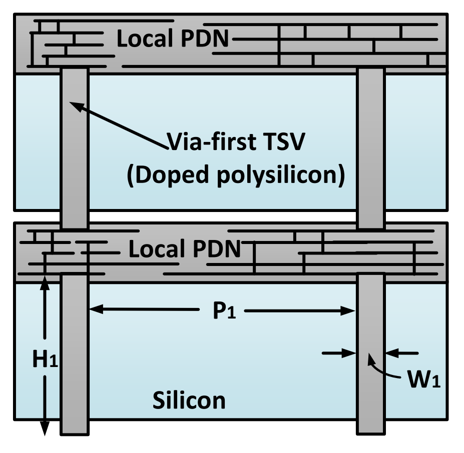


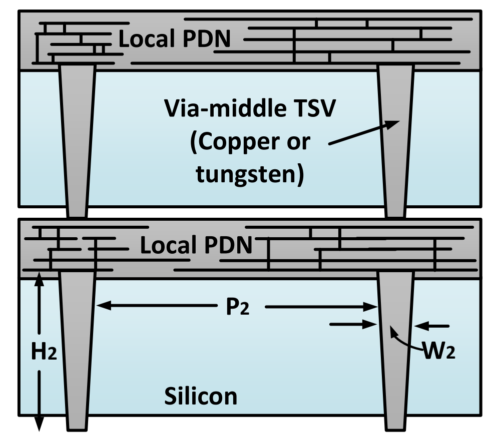
Outline

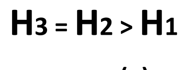
- Introduction & Related Work
- Motivation
- Proposed Method
- Experimental Results
- Conclusion



Introduction of 3D Integration

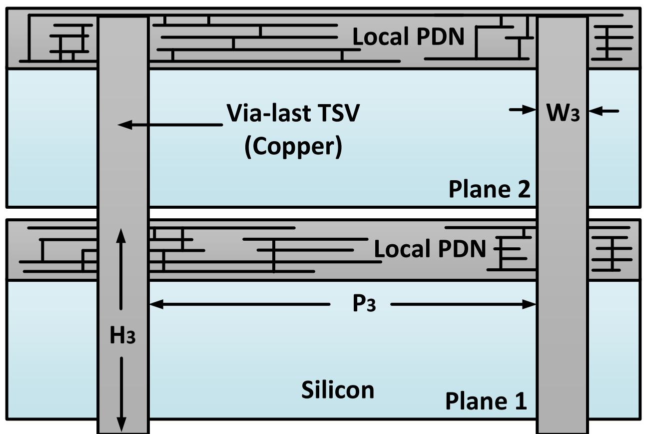






$P_3 > P_2 \geq P_1$ $W_3 > W_1 \geq W_2$

(a) (b)



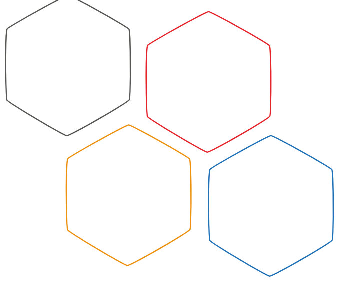
(c)

Advantages of 3D

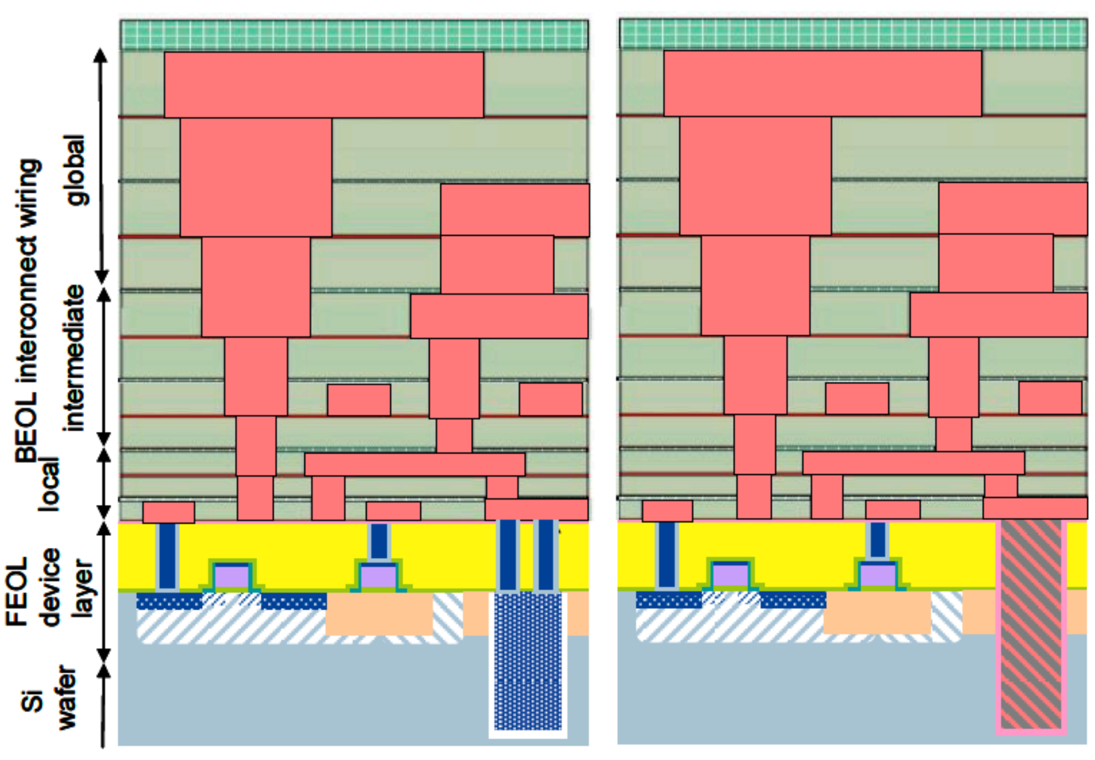
- Smaller global timing delay;
- Smaller interconnect power consumptions;
- Higher integration density (smaller form factor)
- Integration of disparate technologies

Challenges of 3D:

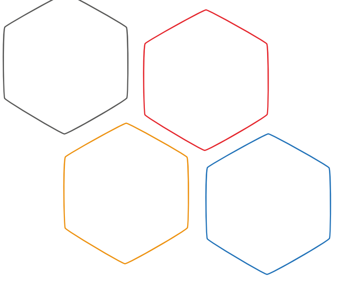
- Chip yield due to novel fabrication process
- Thermal related issues
- Higher current density threatening reliability of 3D ICs…



3D Integration

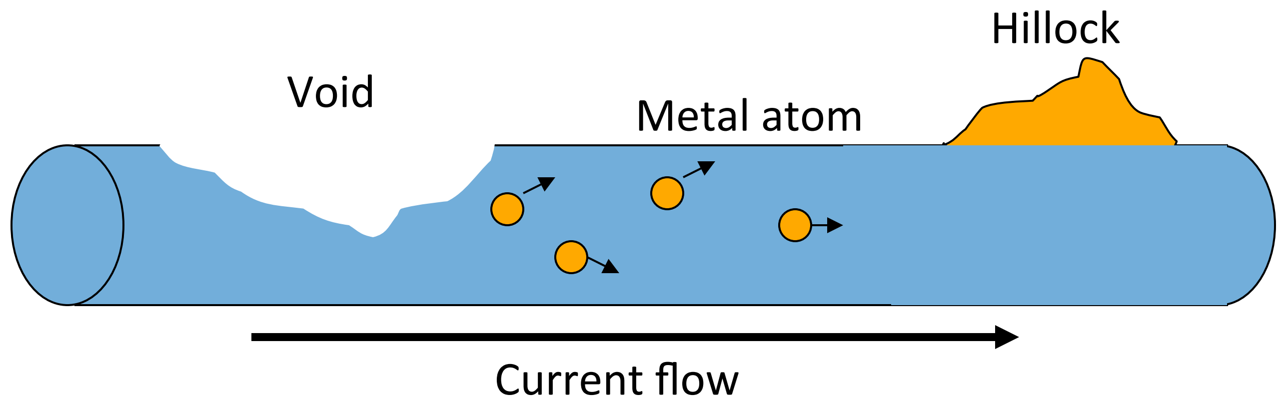


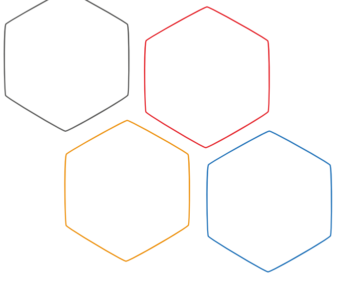
- Physical design problems for 3D ICs:
  - Thermal management, Power management, Power delivery, Noise control, Heat dissipation
  - Placement, routing, floorplanning, etc…



Electromigration Effects

- High current density
- Mass transportation of metal atoms
- Void & hillock formation
- Interconnect breakdown or short

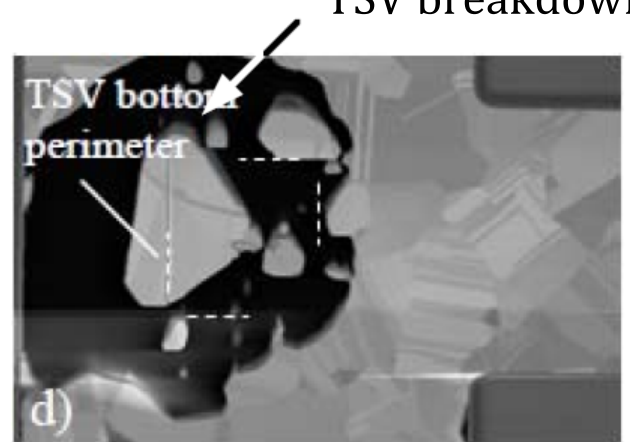




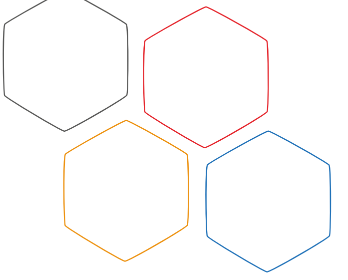
TSV Electromigration

- Higher current density due to higher power consumptions of multiple tiers
- Thermal cycling
- Discontinuous bonding interface of TSV
- TSV defects
  - Filling voids
  - Misalignment
  - Bonding interface contamination

TSV breakdown due to EM

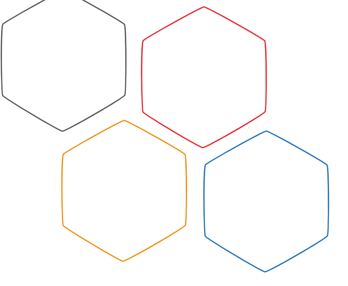


[T. Frank et al. IRPS, 2011]



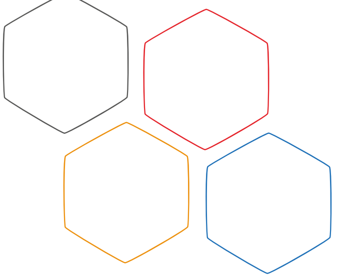
Related Work

- TSV EM effect modeling
  - Pak et al. evaluated EM impact on TSVs from the layout perspective and provided some guidelines for EM-robust TSV design [ECTC’ 2011]
  - Chen et al. proposed a TSV EM model based on finite element method to predict failure positions within a single TSV [ICEPT-HDP’ 2010]
  - Frank et al. explored EM impact on TSV resistance and derived an analytical formula to describe the relationship [IRPS’ 2011]
- 2D interconnect EM effect investigation
  - Gonzalez et al. investigated shape effect on electromigration for metal interconnects [Microelectronics and reliability, 1997]
  - J. Abella et al. proposed an EM mitigation technique by alternating current flows within signal interconnects [Micro’ 08]



Our Contributions

- Investigate TSV EM effects caused by various TSV defects
  - Filling void
  - Misalignment
  - Contamination at bonding interface
- Propose a TSV EM mitigation framework
  - Off-line defective TSV identification
  - Online self-healing circuit



EM - Mean Time to Failure

- MTTF calculation

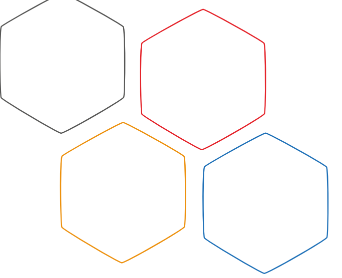
$$MTTF = A \cdot J^{-n} \cdot e^{\frac{Q}{kT}}$$

A, n: technology and material dependent constant
J: TSV current density
k: Boltzman's constant
T: temperature

- Current density calculation

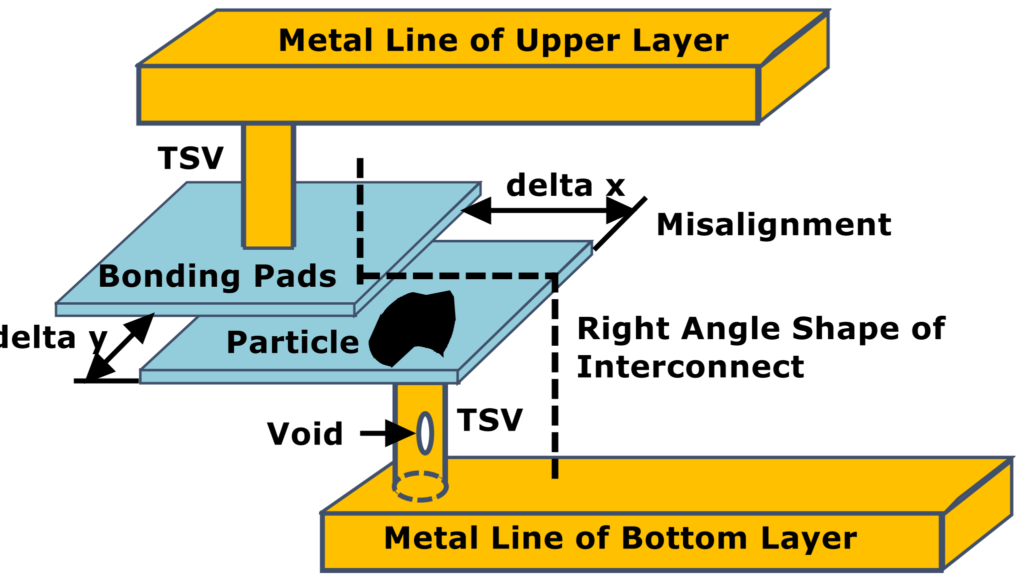
$$J = \frac{C \cdot V_{dd}}{S} \cdot f \cdot p$$

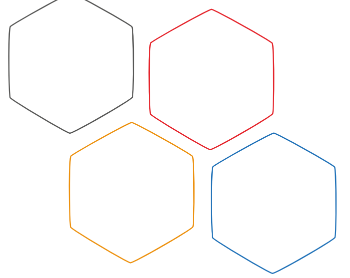
C: TSV capacitance
Vdd: Power supply voltage
S: TSV cross-sectional area
f: operation frequency
p: signal switching activity within TSV



Motivation

- TSV defects
  - filling void
  - misalignment
  - bonding interface contamination





EM Occurrence due to TSV filling

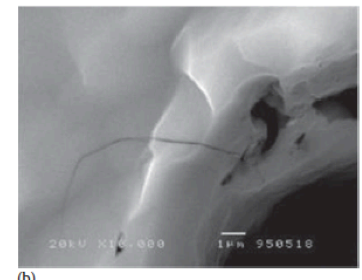
- TSV filling void

Metal Line of Upper Layer
TSV
delta x
Misalignment
Bonding Pads
delta y
Particle
Right Angle Shape of Interconnect
Void
TSV
Metal Line of Bottom Layer

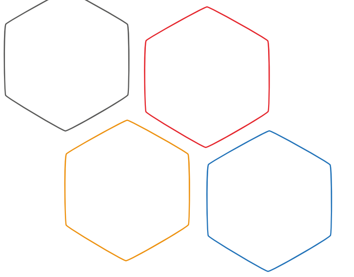
Filling void

[Fraunhofer]

(a)

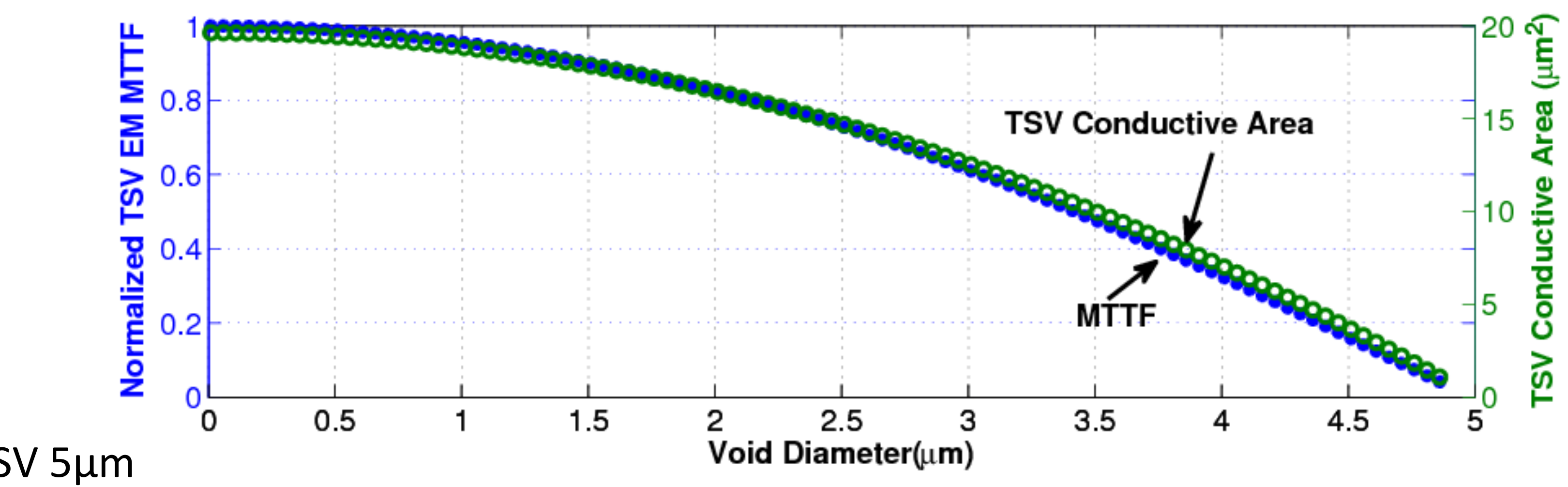


(b)



EM Occurrence

- EM effect due to TSV filling void

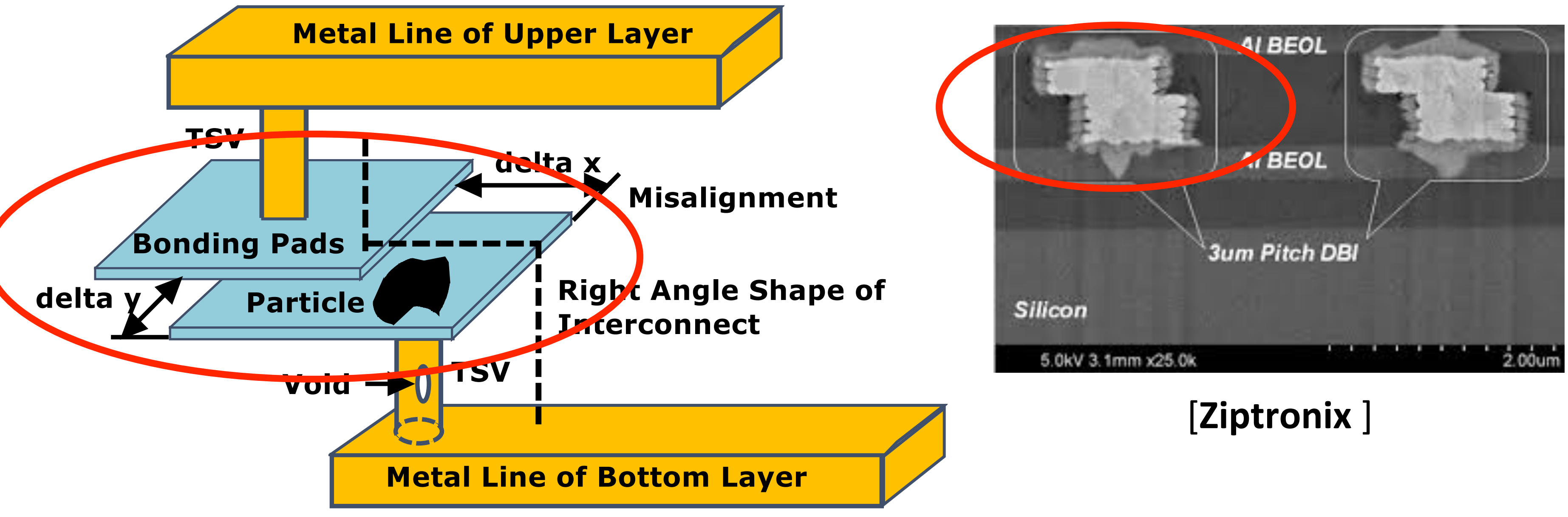


TSV 5µm

Observation: It shows that when void size exceeds 3.5µm, the MTTF value reduces over 50%. As void size increases further, MTTF value falls down quickly.

EM Occurrence due to Misalignment

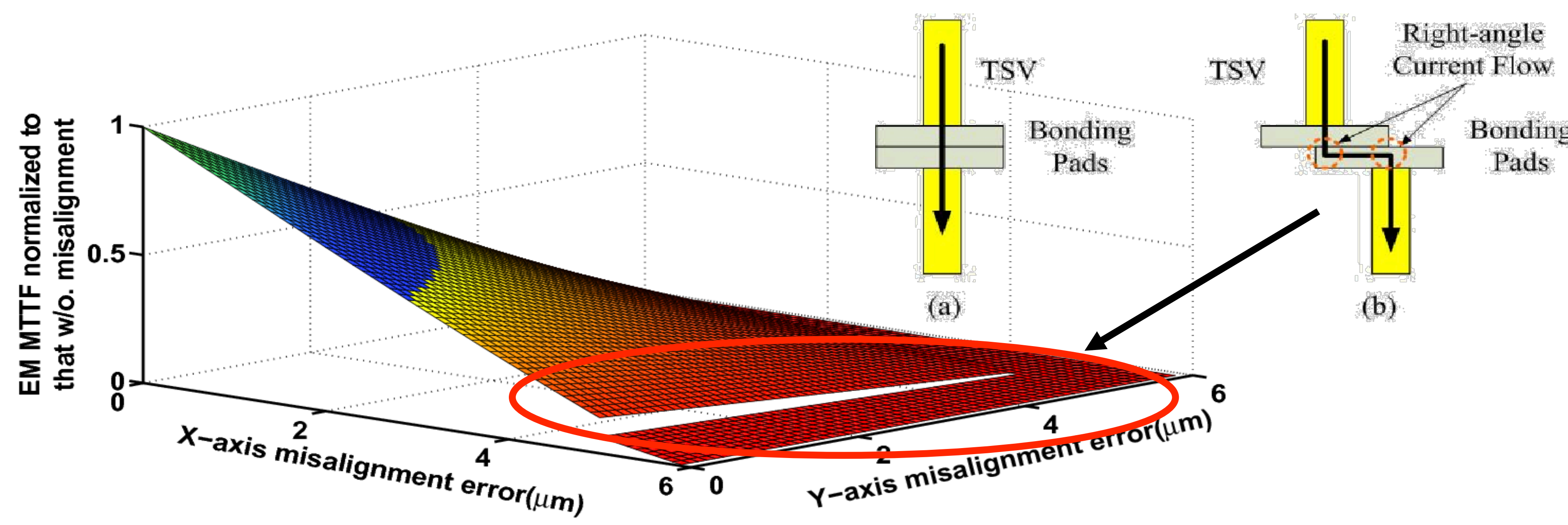
- Bonding pad misalignment



[Ziptronix]

EM Occurrence due to Misalignment

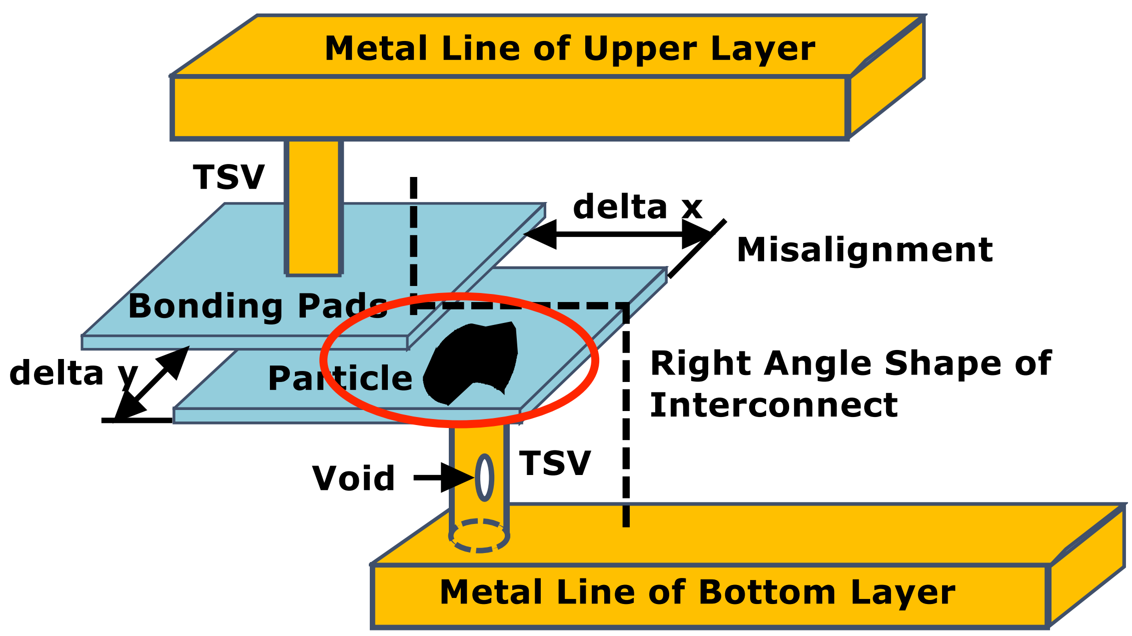
- EM effect due to misalignment

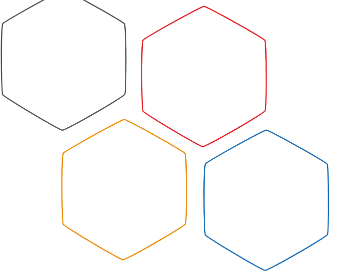


Observation: As shown in the figure, TSV EM MTTF decreases rapidly as the misalignment error increases.

EM Occurrence due to Contamination

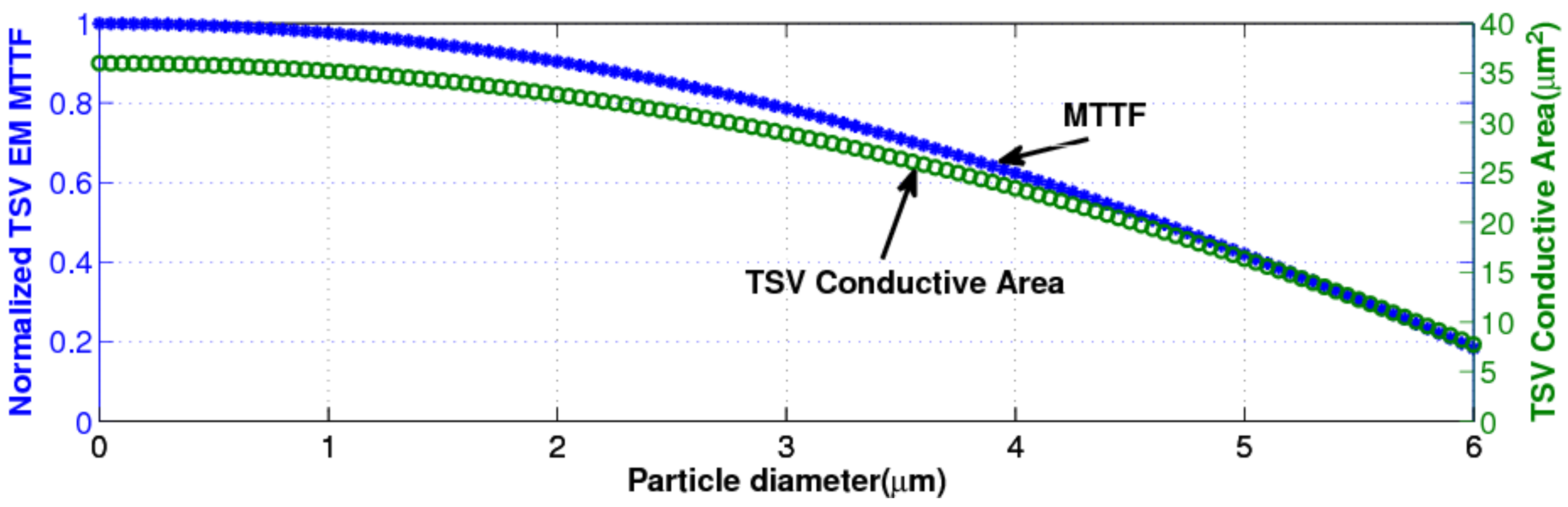
- Bonding interface contamination



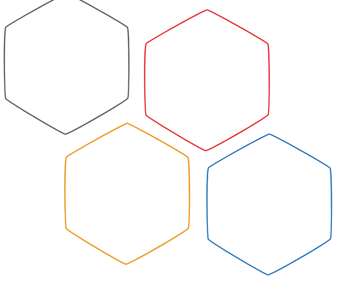


EM Occurrence due to Contamination

- EM effect due to bonding interface contamination



Observation: It shows that TSV EM MTTF reduces quickly with increasing of dust size. When it exceeds 4.5µm in our case, MTTF reduces over 50%.



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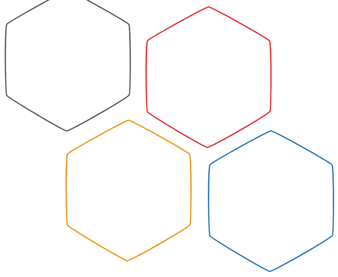


Our Proposed Framework

Off-line defective TSV detection

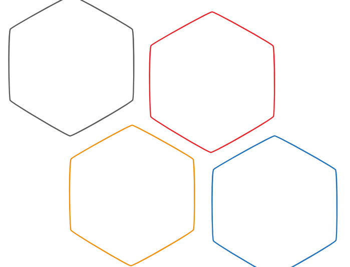
Fault map

Switch network

Defective TSV

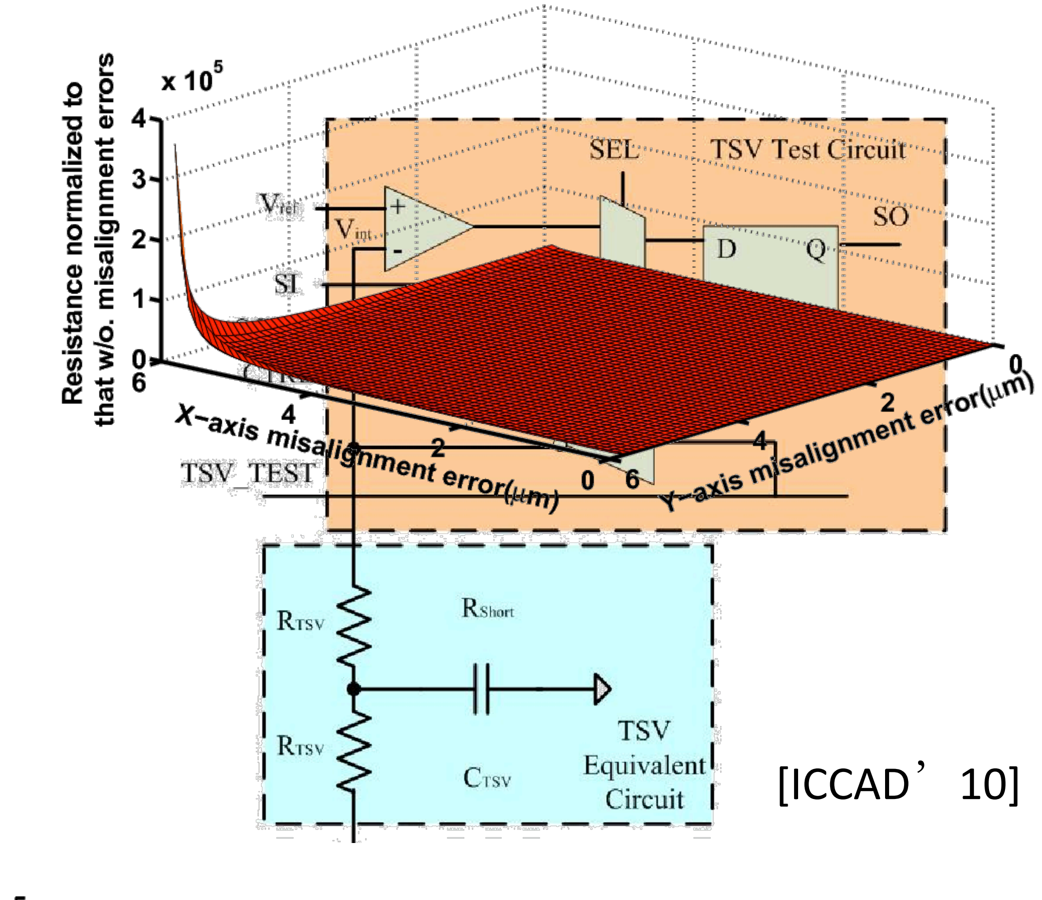
Online self-healing circuit

Fault Map
CTRL_1
CTRL_2
CTRL_3
CTRL_4
CTRL_5
signal1
signal2
signal3
signal4
signal5
EM Mitigation Module
TSV1
TSV2
TSV3
TSV4
TSV5
Another Tier

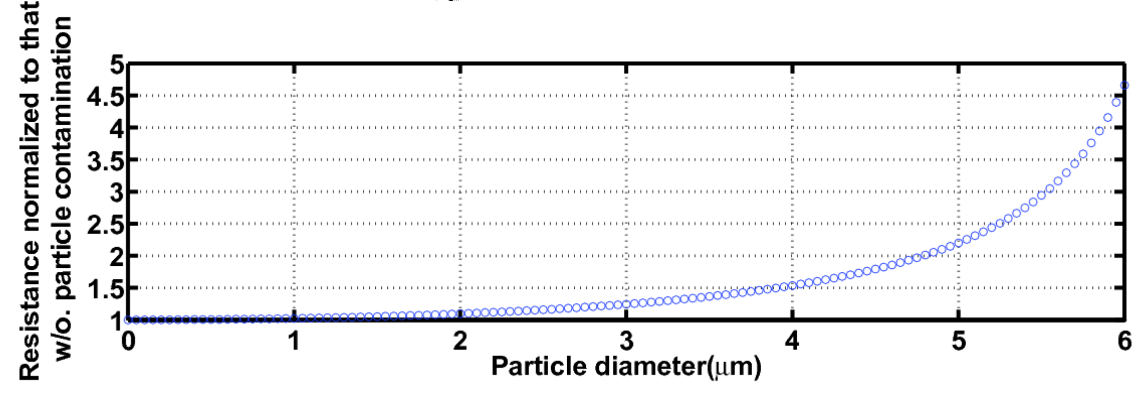


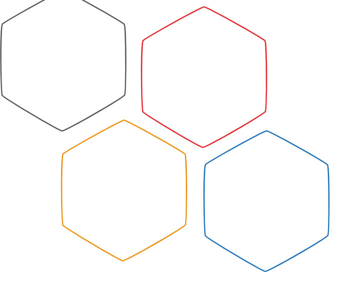
Off-line defective TSV identification

- TSV filling void [pre-bonding]
  - Using sensing circuit to detect defective TSVs by capacitance variation [ATS'09]
- Misalignment and bonding interface contamination detection [post-bonding]



[ICCAD' 10]



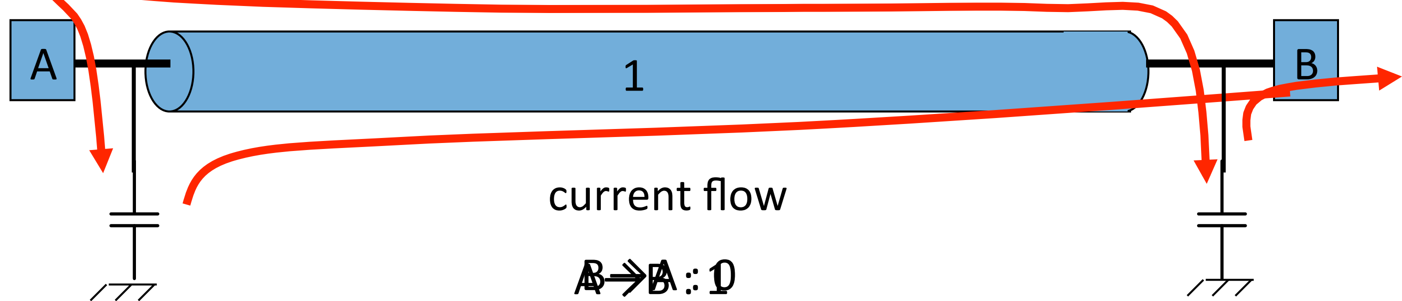


Self-healing Principles

- Current direction and data pattern

Original bus state	Data Transmission	Current flow
0	1, A → B 1, A ← B 0	A → B A ← B --
1	0, A → B 0, A ← B 1	A ← B A → B --

Current direction & data pattern



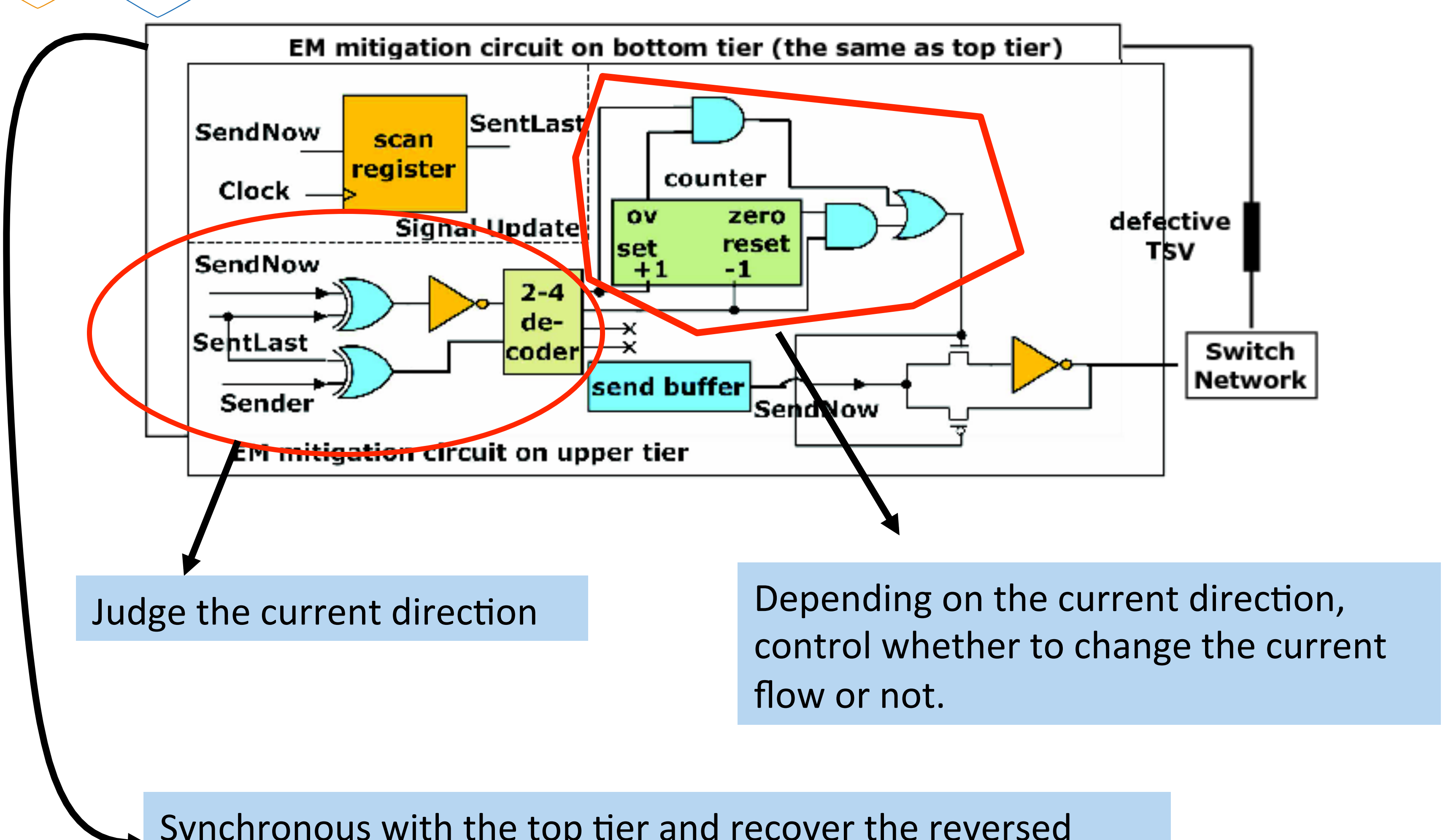
1. Original TSV state ‘0’;

2. A sends ‘1’ to B. Current flows from A to B to charge TSV signal line;

3. B sends ‘0’ to A. Current flows from A to B to discharge TSV signal line.

Current flows from A to B continuously and causes EM effect.

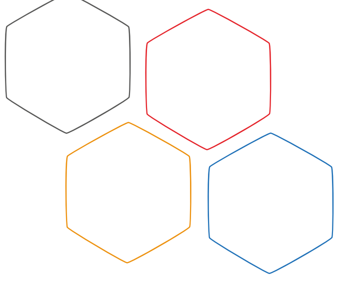
Self-healing circuit



Judge the current direction

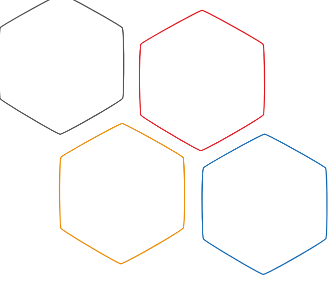
Depending on the current direction, control whether to change the current flow or not.

Synchronous with the top tier and recover the reversed signal at the receive end.

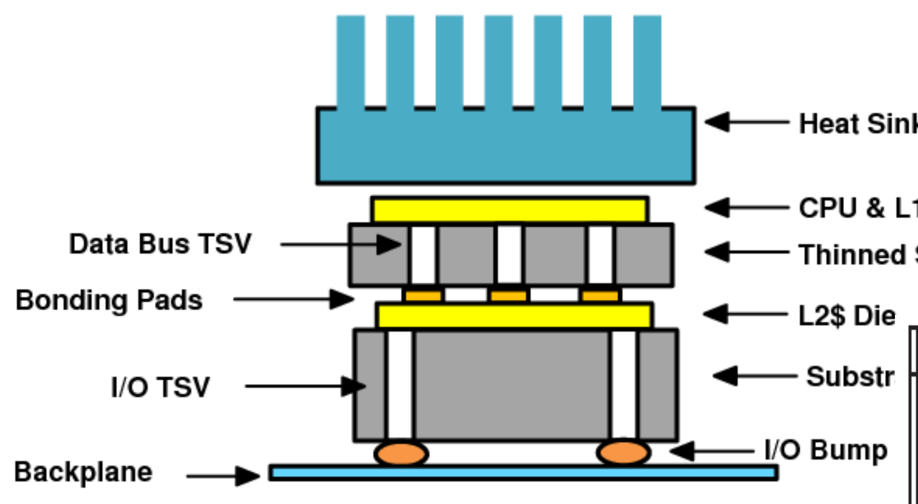


Outline

- Introduction & Related Work
- Motivation
- Proposed Method
- Experimental Results
- Conclusion



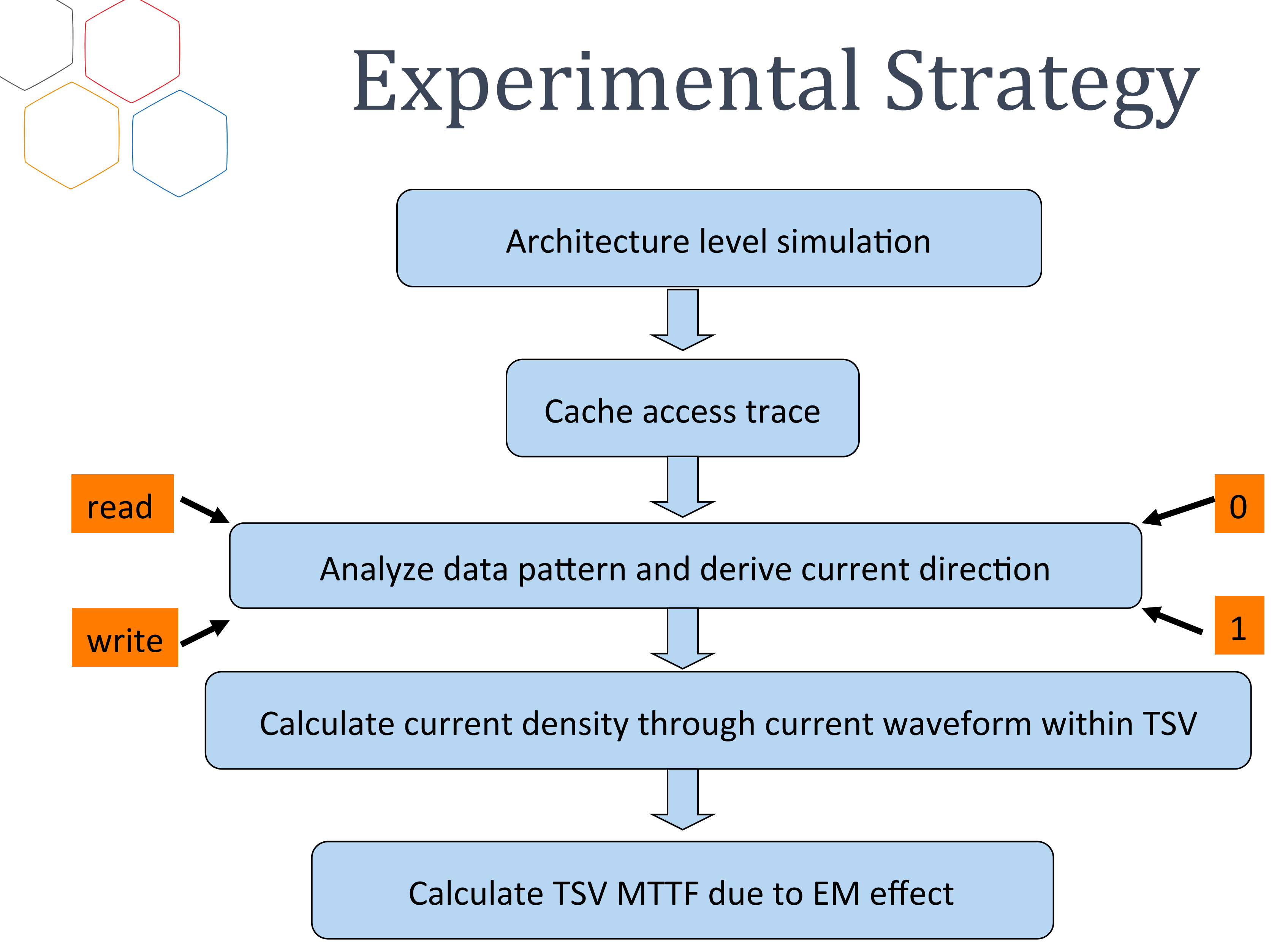
Experimental Setup



Configuration

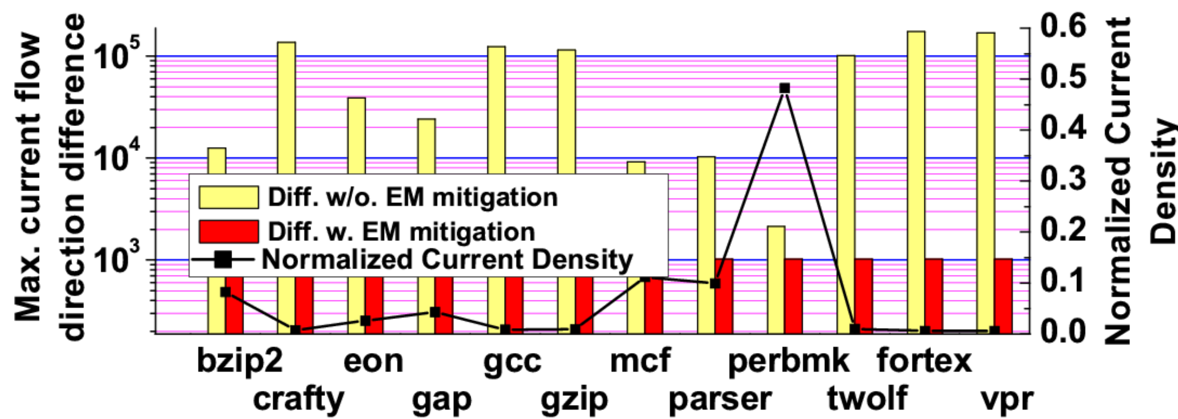
CPU	Alpha 21264 1.33GHz
Predictor	Bimodal predictor, using a BTB with 2-bit counter 3 cycles miss prediction penalty
IFQ Size/LSQ Size	4/8
L1 D$/I$	32KB, 128B block size, 2-way associative, LRU replacement write-back policy, 1 cycle hit latency
L2 Unified $	512KB, 128B block size, 2-way associative, LRU replacement write-back policy, 6 cycles hit latency
ITLB/DTLB	64 entries/128 entries
TSV Bus Width	1024
TSV Feature Size	5μm diameter, 25μm depth
TSV Pad Size	$6\mu m \times 6\mu m$

Experimental Strategy

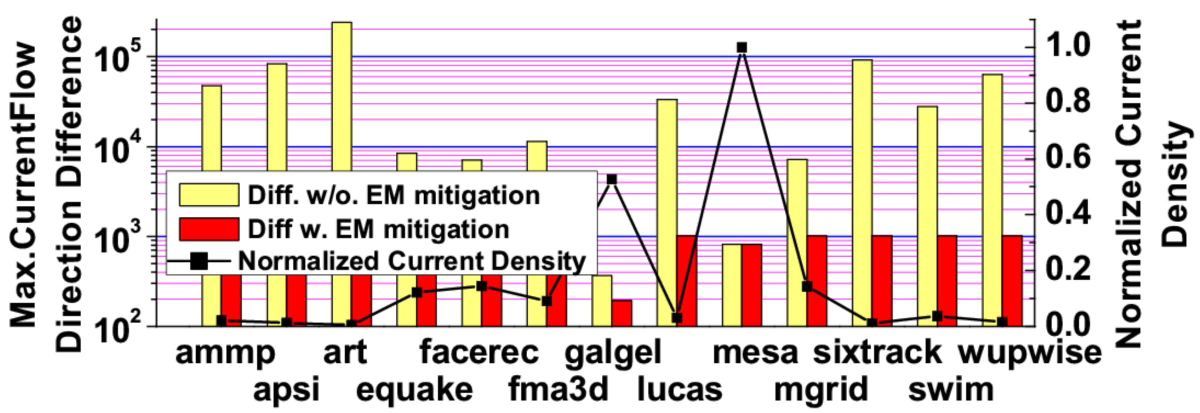


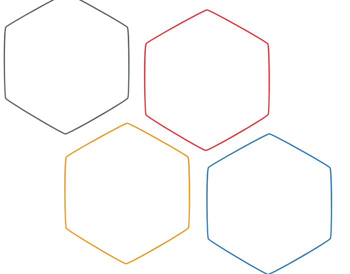
Current direction diff. & current density

- SPECINT



- SPECFP





MTTF comparisons

- SPECINT

1.8×10^4

(a) bzip2

x 10^4

The difference between the number of two directions of current flows

TSV index

(b) ammp

5×10^4

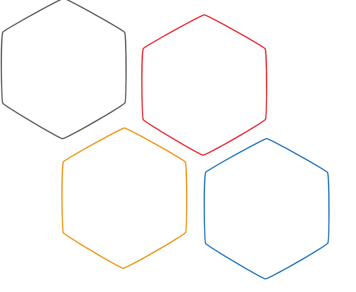
Normalized EM MTTF

W/O. EM Mitigation

EM Mitigation

bzip2 crafty eon gap gcc gzip mcf parser perlbmk twolf vortex vpr Ave.

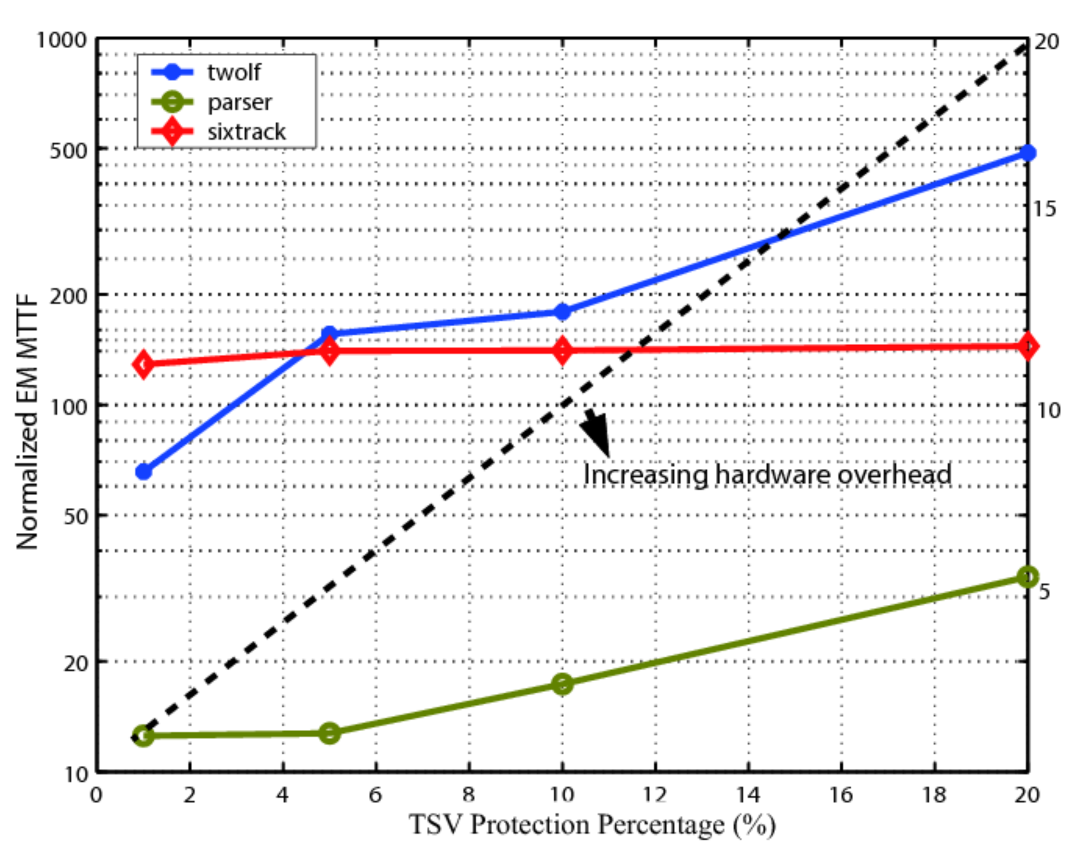
ammp apsi art equake facerec fma3d galgel lucas mesa mgrid sixtrack swim wupwise Ave.



Overhead estimation

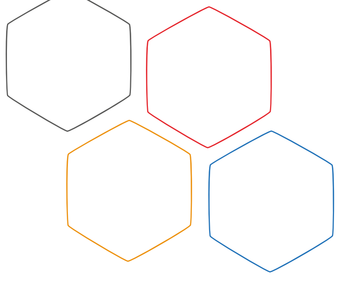
- Assume 5% defective TSVs, chip size 1.6mm×1.6mm, ST 90nm technology
  - Area overhead: 40858um^2 (less than 2% chip area)
  - Power consumption: 11.8mW

Overhead Vs. Protect fraction



1. As protect fraction increases, hardware overhead increases.

2. The current flow balance Property of parser is better than those of twolf and sixtrack



Conclusions

- TSV defects can incur severe EM effect and threaten reliability of 3D ICs
- Investigate relationship between TSV defects and TSV MTTF due to EM effect
- Propose a framework consists of off-line defective TSV detection and on-line self-healing circuit to mitigate TSV EM effect

Thank you!

Q&A?