



# Smart imagers integration in 3D stack technology

**D43D Workshop June 2017**

STMicroelectronics/Imaging Division

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# Presentation content

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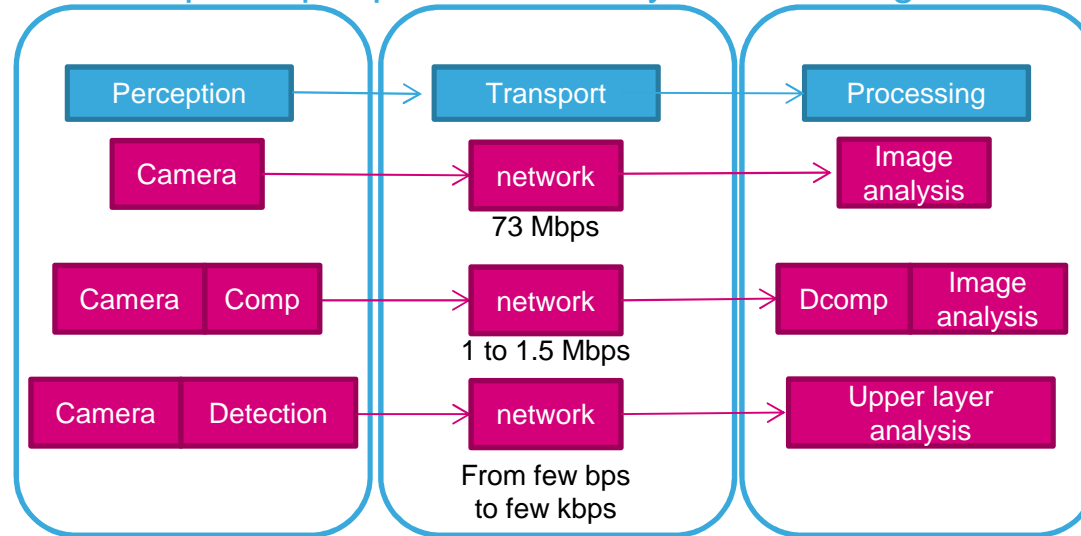
- Why smart imagers ?
- Rationale for using 3D stacking
- Description of STMicroelectronics 3D stacked smart imager prototype
- Next steps and directions for 3D over target markets



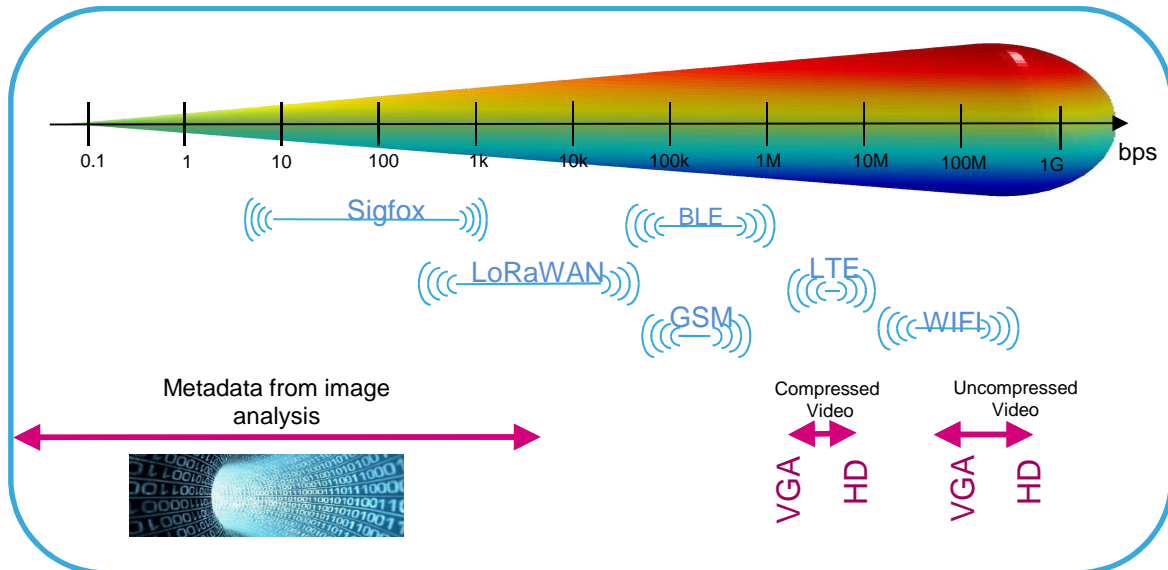
# Why smart imagers ?

# Case analysis: Indoor people detection

Practical example of people detection system running on VGA image at 30 fps.

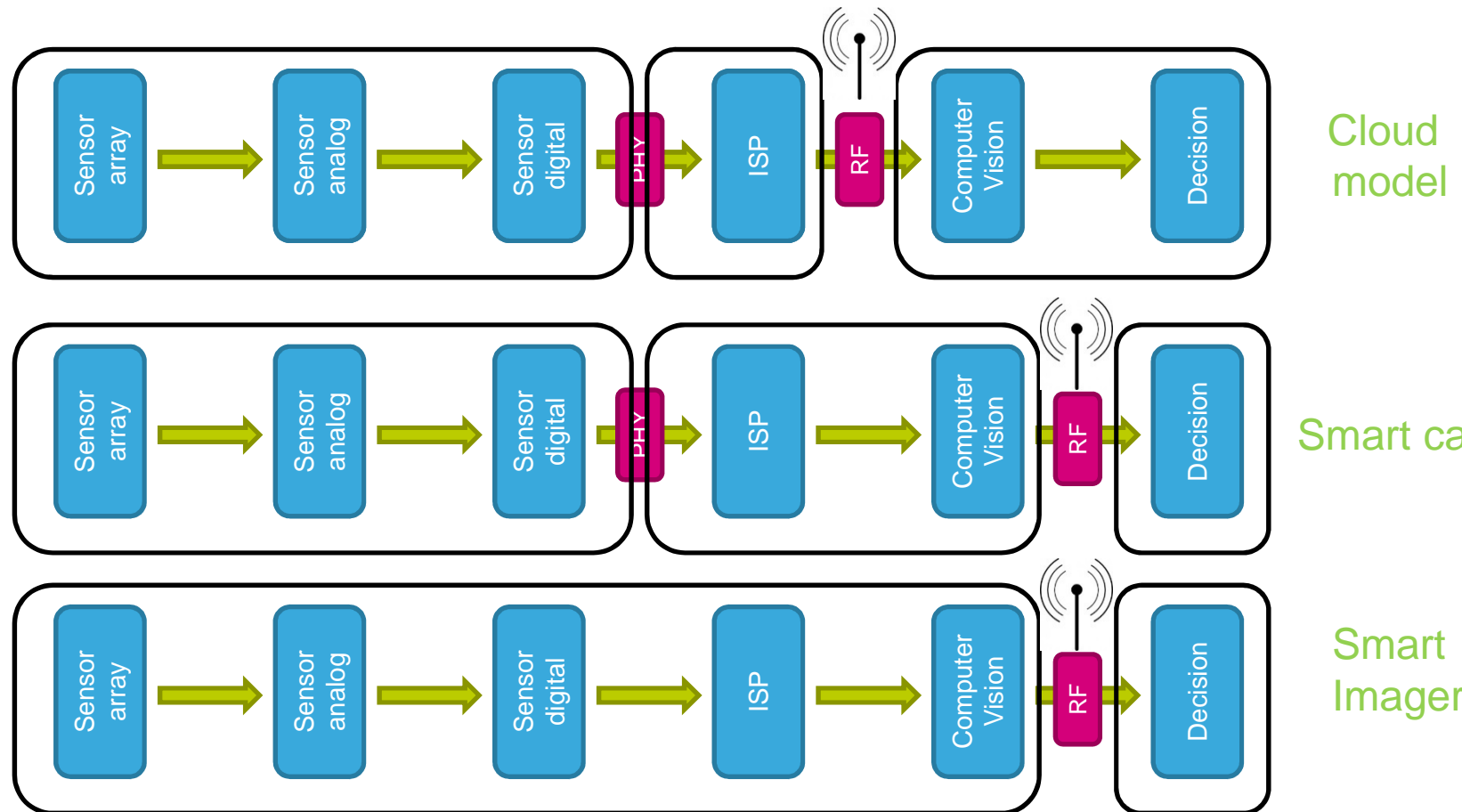


- Transferring metadata rather than raw image is more efficient by a significant ratio ( $\sim 10^7$ )
- This is fully scalable as quantity and frequency of information can be adapted to the network and application needs.
- This is the only approach compatible narrow band Long Range RF communication technologies targeted for IoT.



# From Imager to Analyses – a complete chain

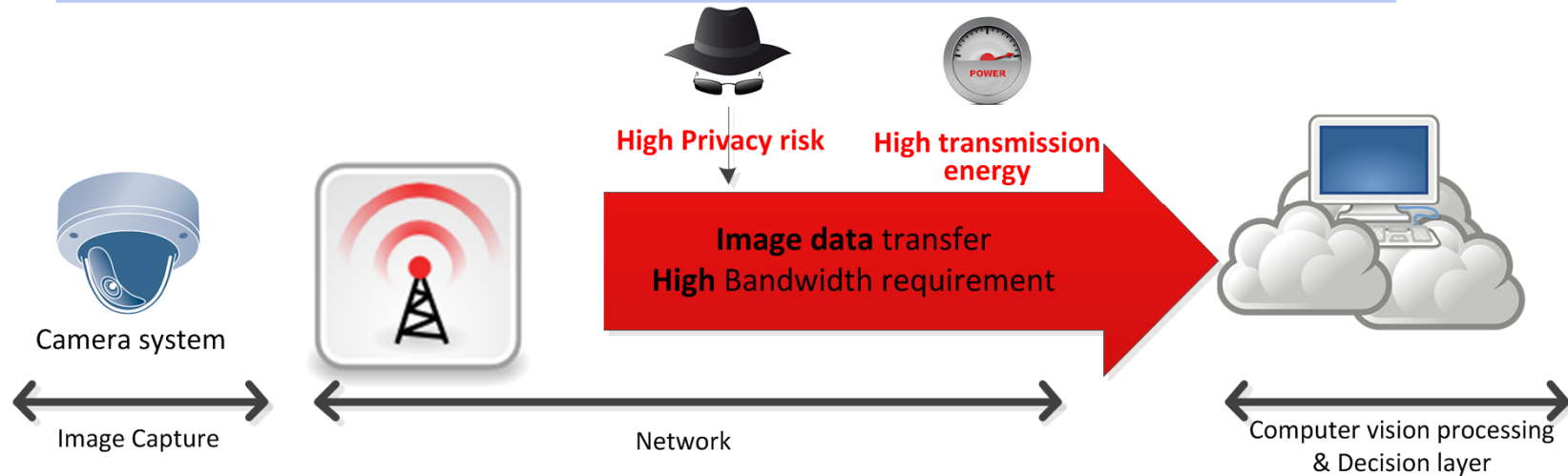
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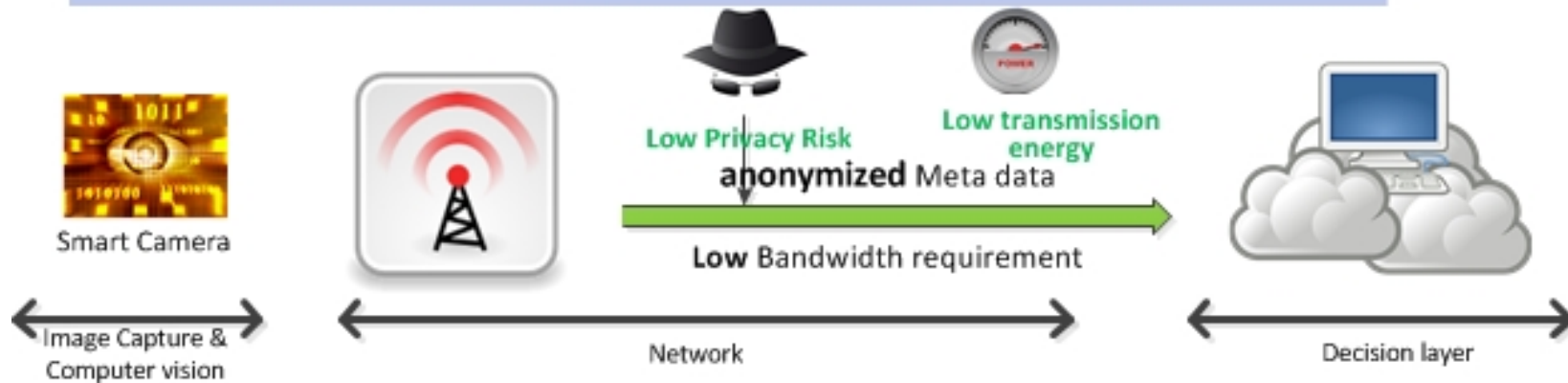
# Benefits of local processing – privacy by design

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Conventional camera with image analysis performed in the cloud



Smart camera with image analysis performed on-chip





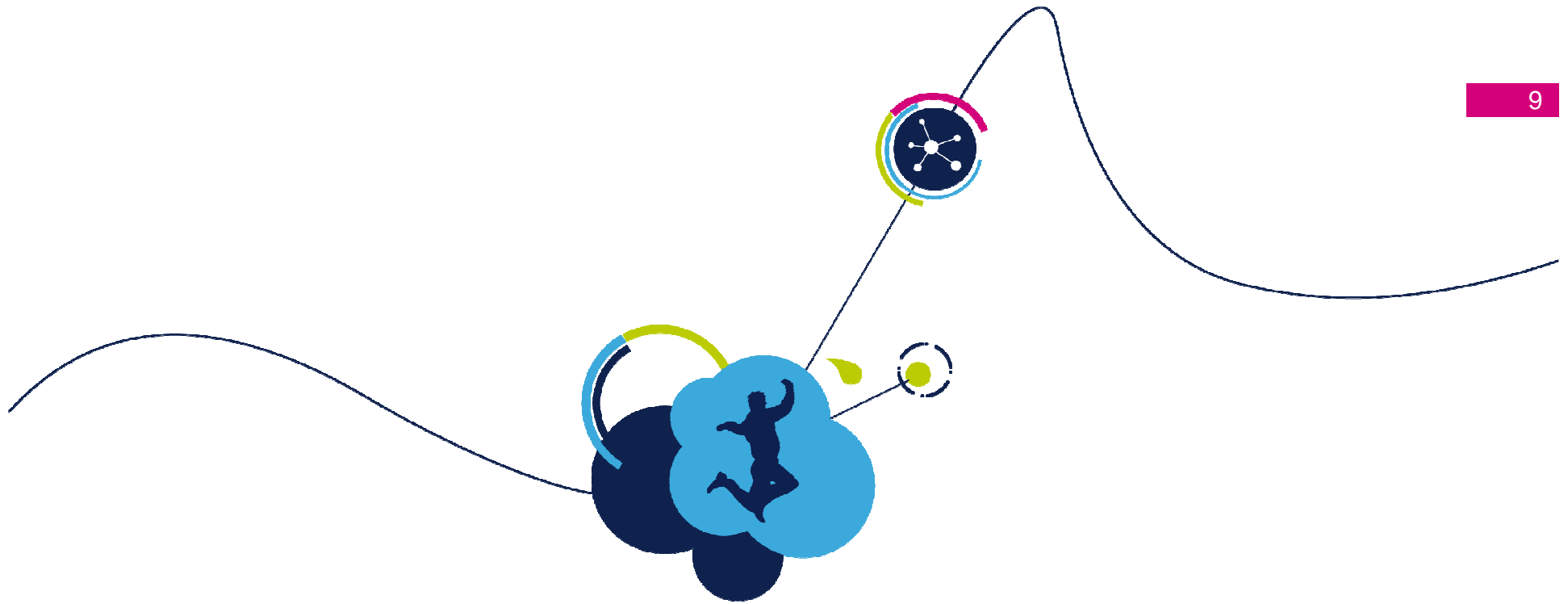
# Rationale for 3D stacking

# 3D stacking rationale for image sensors

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- Enables access to advanced digital technology nodes without effort of porting on a specific imager process.
- Allows an optimization of the pixel process on the top die.
- Device X,Y dimensions can be minimum, and are only dependent of pixel size and array resolution → Benefits on cost and footprint.
- Much better power consumption as logic is developed on thinner technology.
- Large area in the bottom die for integrating functions with added values. Enable proposal for one-chip device as self content camera head, easy to integrate in a system, and including :
  - Image sensor
  - Image signal processing
  - Computer vision
  - Security IPs
  - Opening a world new capabilities...
- Privacy by design (image never sent out)
- Thermal to be modeled and managed carefully to avoid visible thermal artifacts on the image.



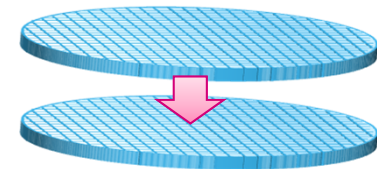


# STMicroelectronics 3D stacked smart imager prototype

# Image Sensor 3D stack technology

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- Wafer on Wafer stacking
- Hybrid bonding technology
- Passive substrate replaced by advance digital CMOS wafer
- Cut done at Column level – only pixels matrix on the top die.



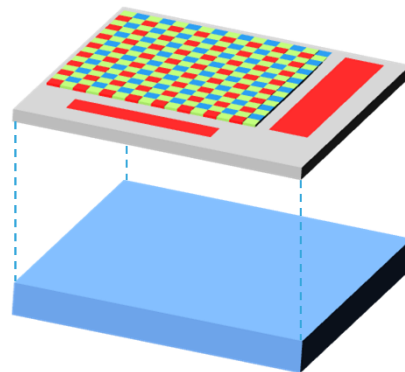
## Conventional BSI Imager

### Top die

- Pixels
- Analog & Readout
- Sensor Logic

### Bottom die

- Substrate for mechanical support



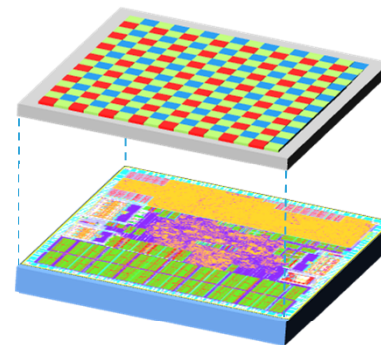
## 3D stacked BSI Imager

### Top die

- Pixels

### Bottom die

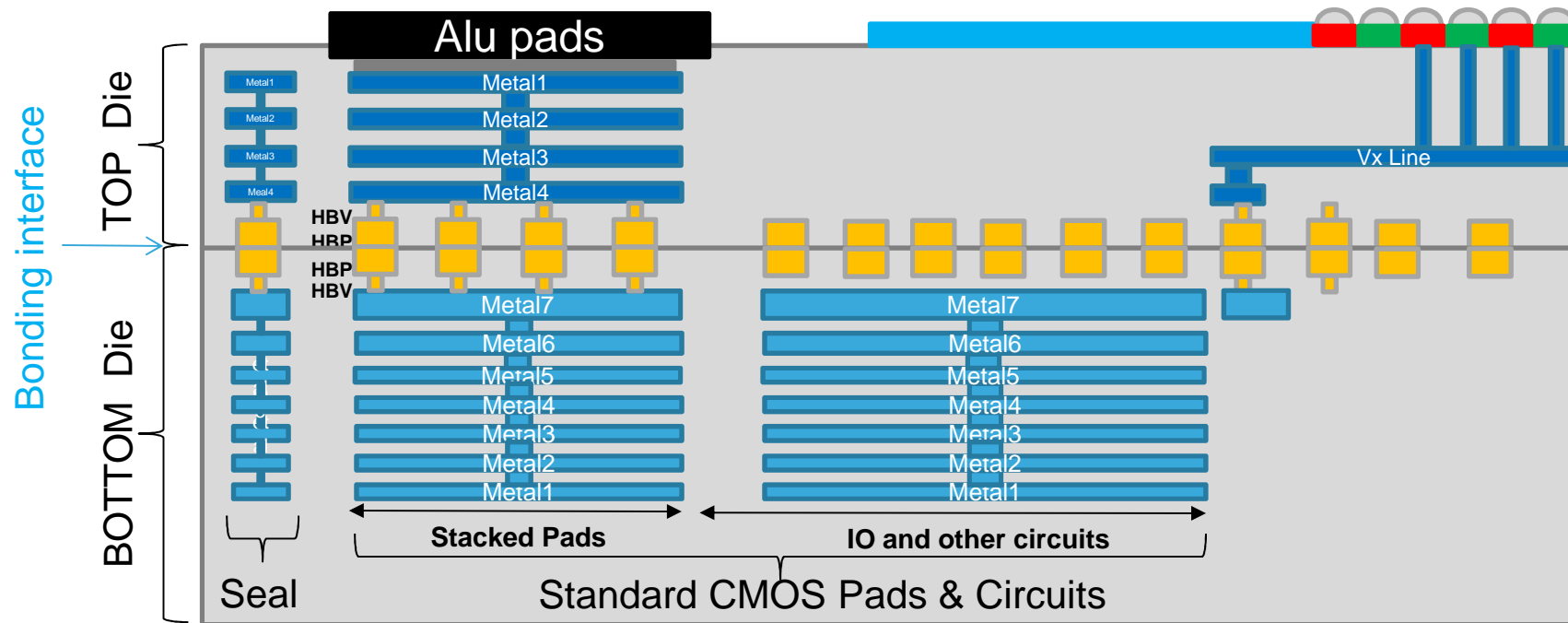
- Analog & Readout
- Sensor Logic
- And more !!!



# Image Sensor 3D stack technology

## 3D stacking

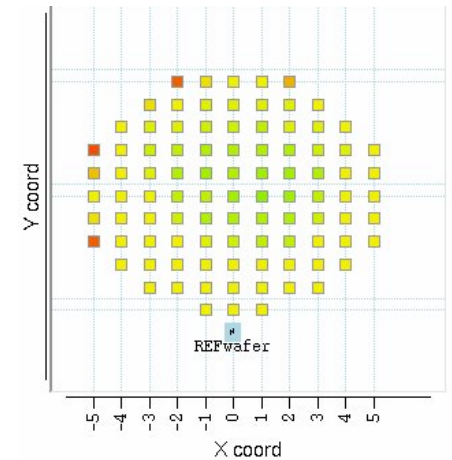
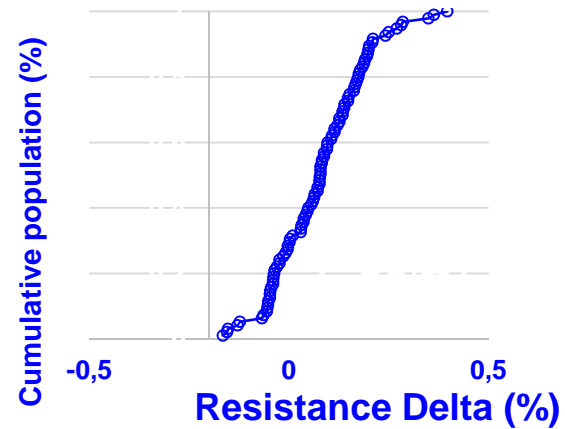
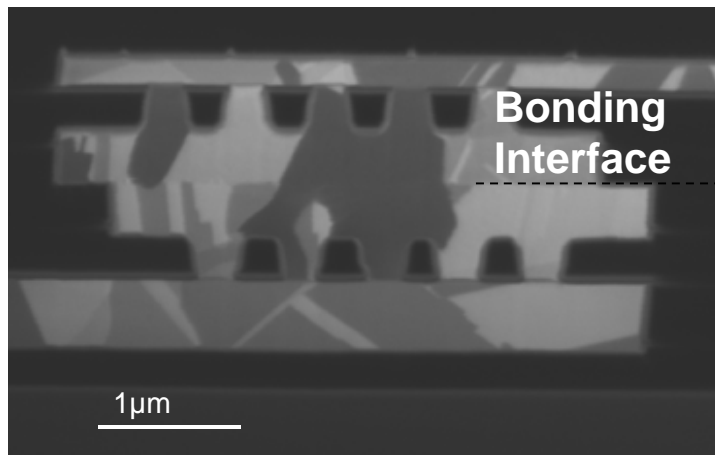
- Fine pitch interco thanks to **Hybrid Bonding technology**
- Top die optimized for pixel – keep only pixel layers
- Process developed with CEA/Leti



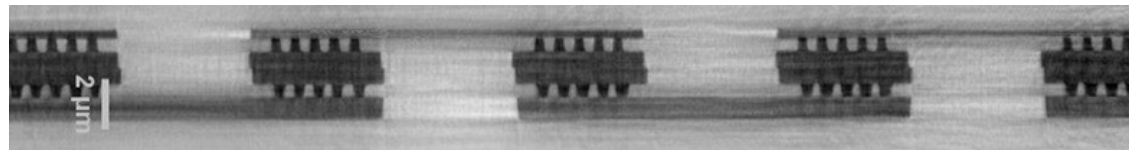
Credits: STM CRL R&D 3D team

# Hybrid Bonding Interface

- 100% yield measured on electrical structures
  - Including 30k daisy chains
  - Alignment perf <200nm +/-3s



leti

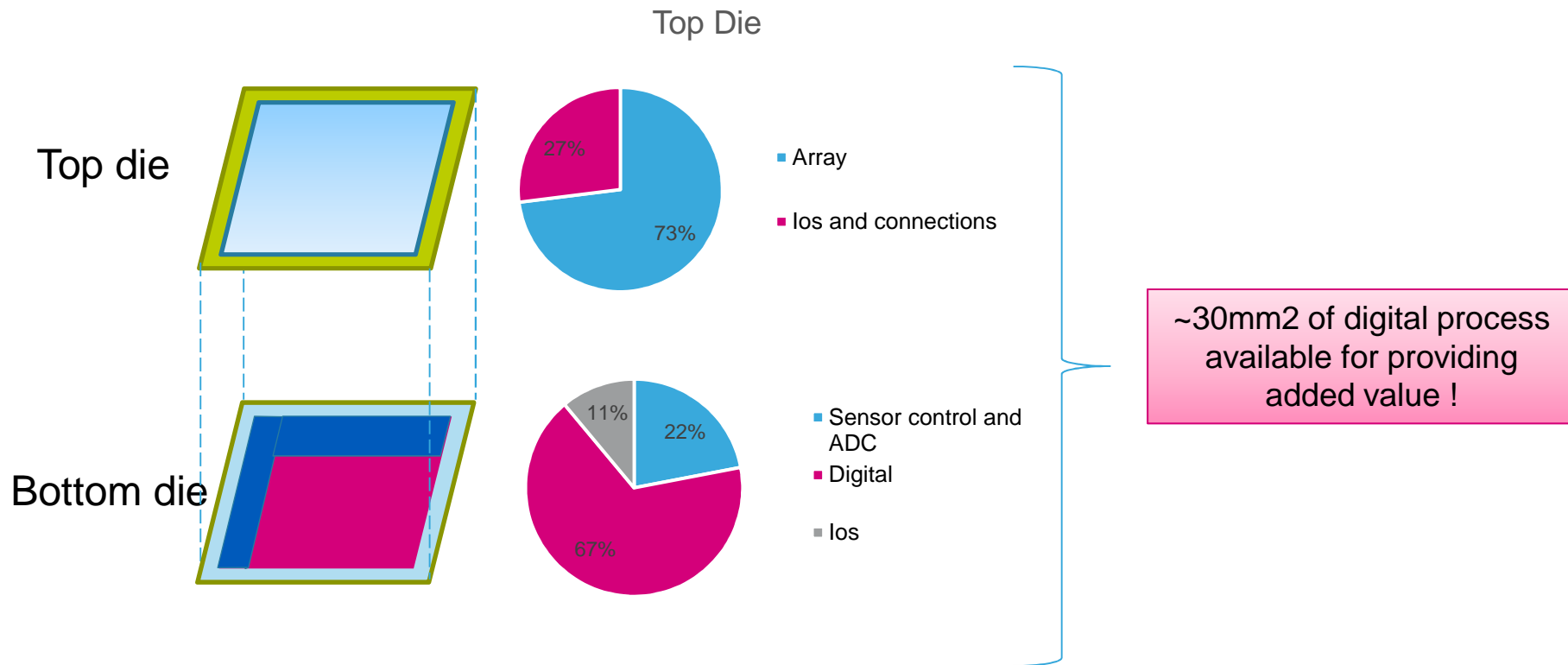


ST  
life.augmented

Credits: STM CRL R&D 3D team

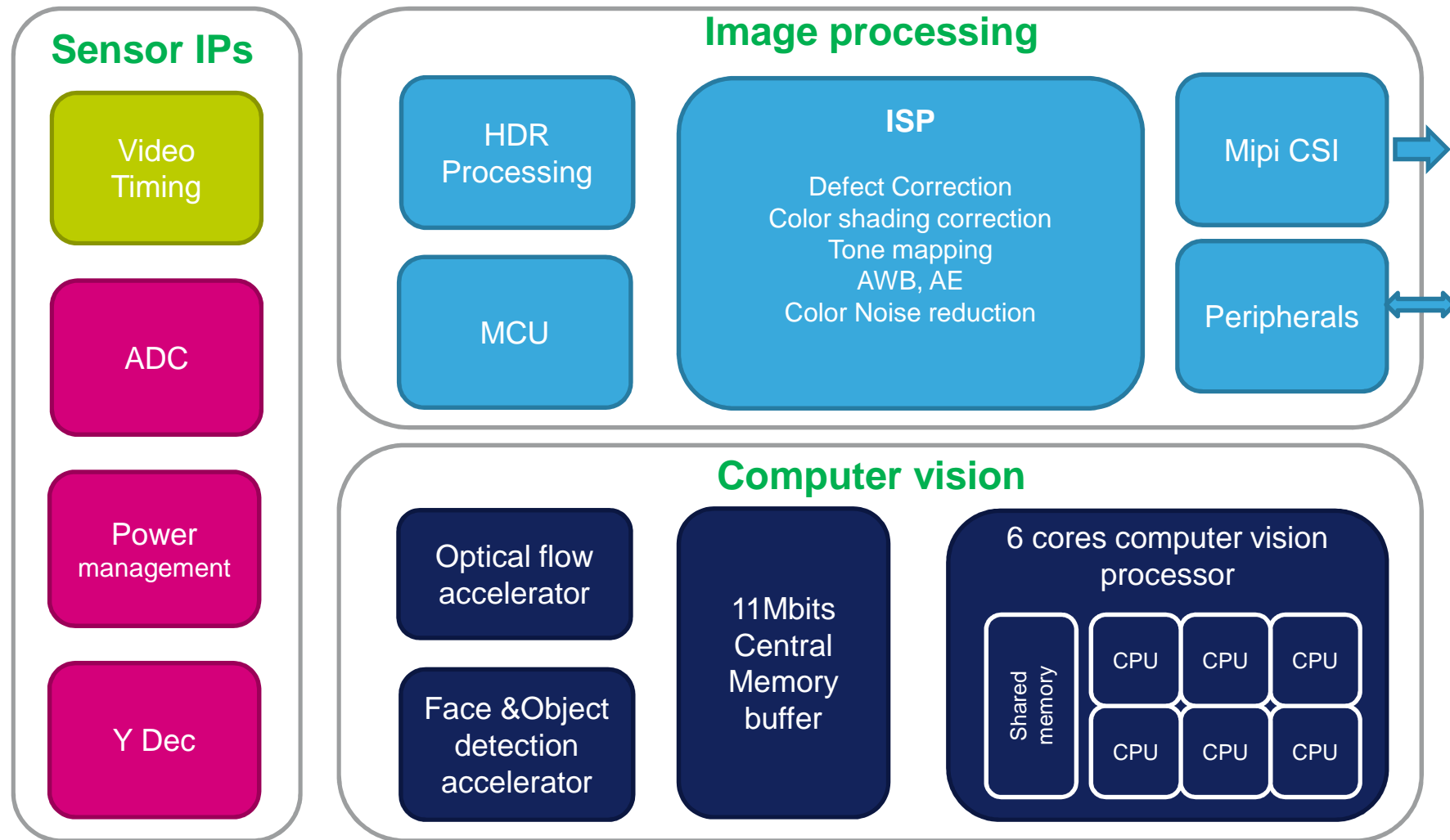
# Area budget available on both layers

- Example top and bottom dies breakdown for a
  - 14Mpix, 1.5um pixel pitch, imager or
  - 3.5Mpix 3um device (2x2 pixel grouping) .

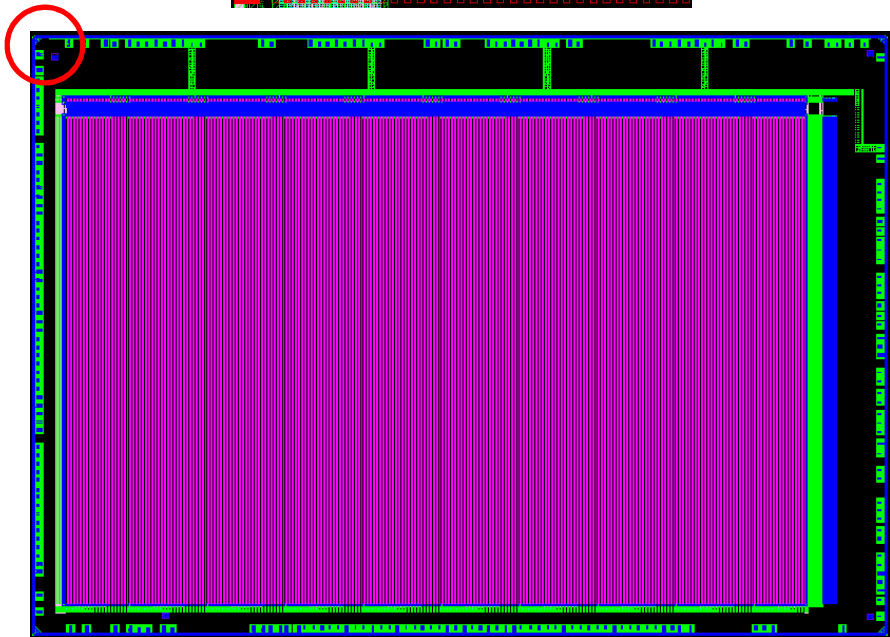
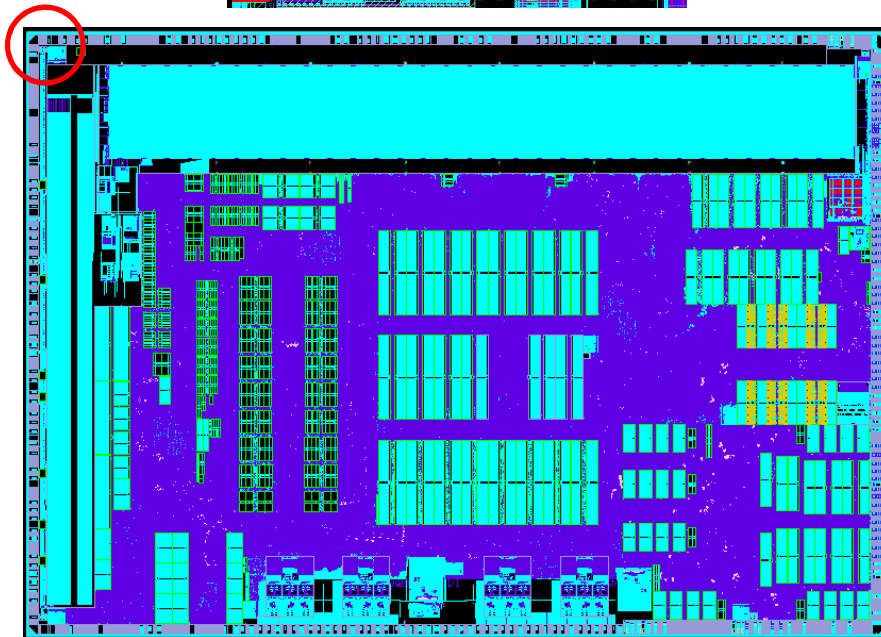
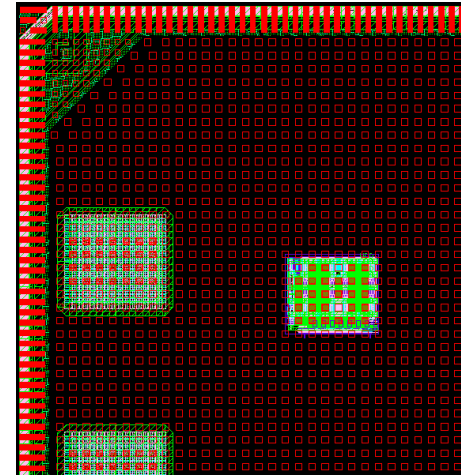
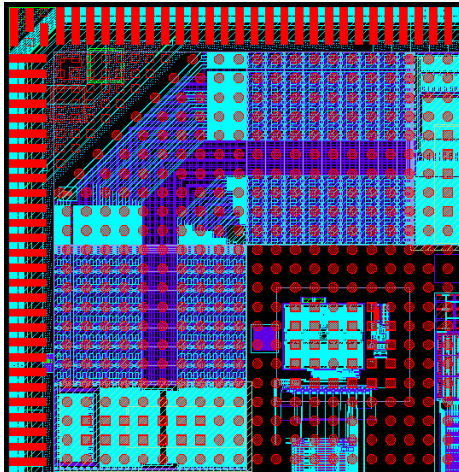


# 3D Stack imager content

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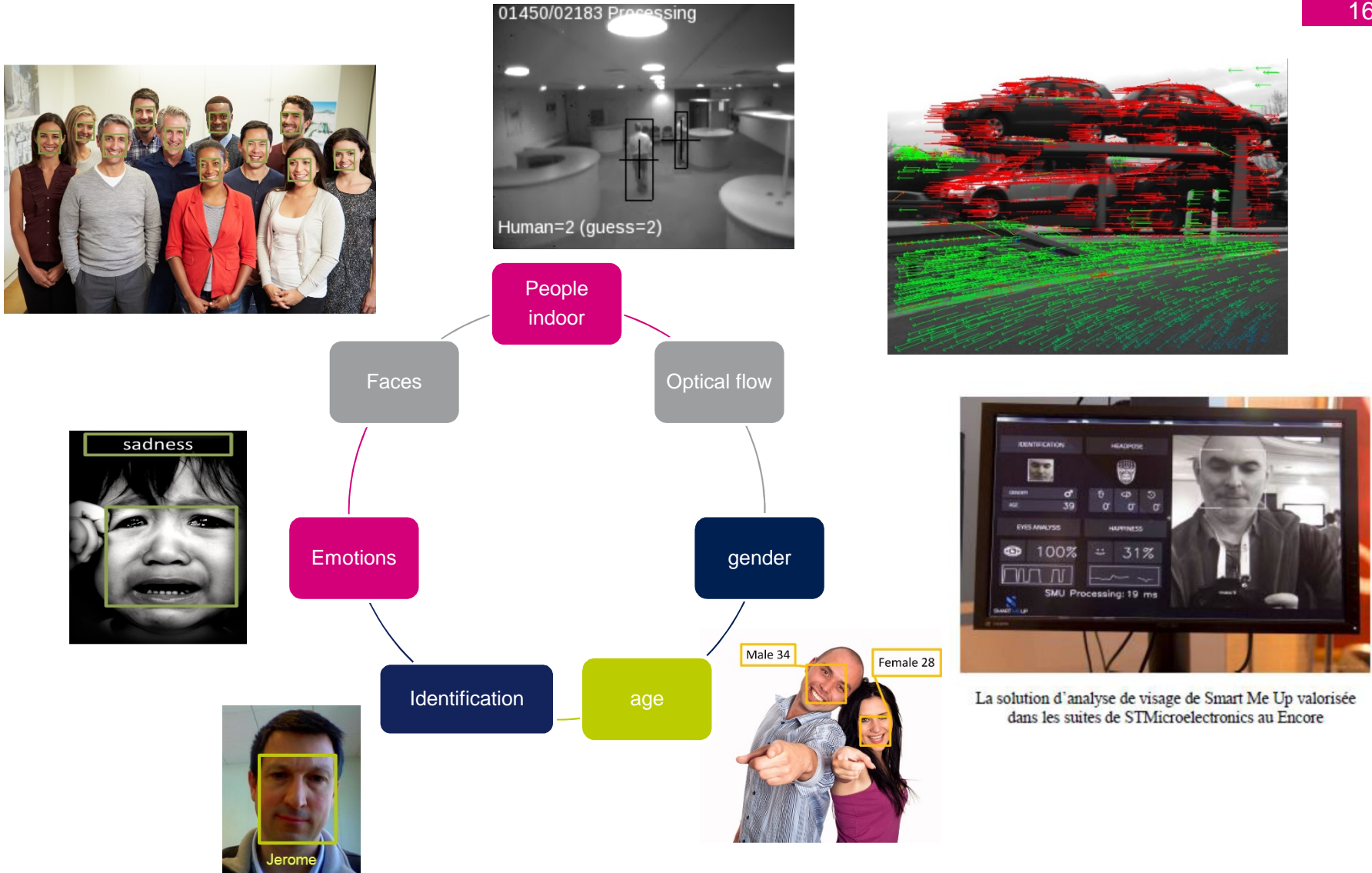
# 93D Top and bottom dies floorplan



Bottom die

Top die

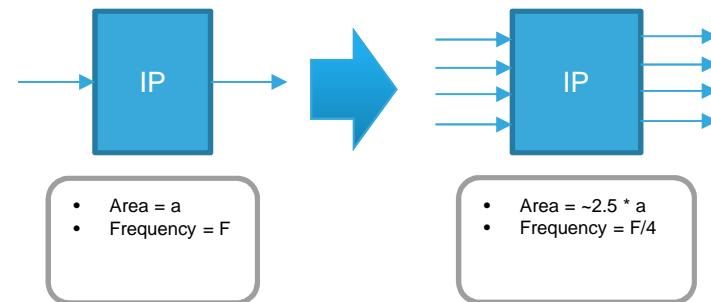
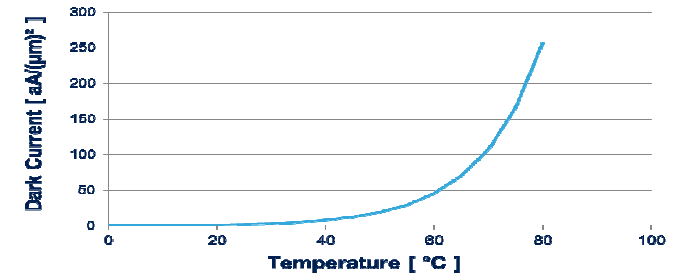
# 93D smart camera use cases shown at CES



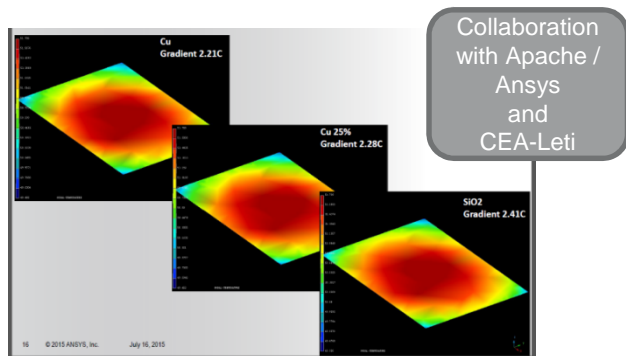


# Power consumption and thermal

- **Goal**
  - To minimize global heating and avoid increasing dark current
  - To minimize local heating (hot spots) which could become visible on the imager.
- **Architecture**
  - Frequency reduction higher than area increase  
→ IP dependent gain b/w 10% and 60%
  - Easier timing closure at ¼ frequency  
→ saving b/w 10% and 30%
  - Can work at lower voltage (e.g. 1.0V instead of 1.1V)  
→ 10% saving

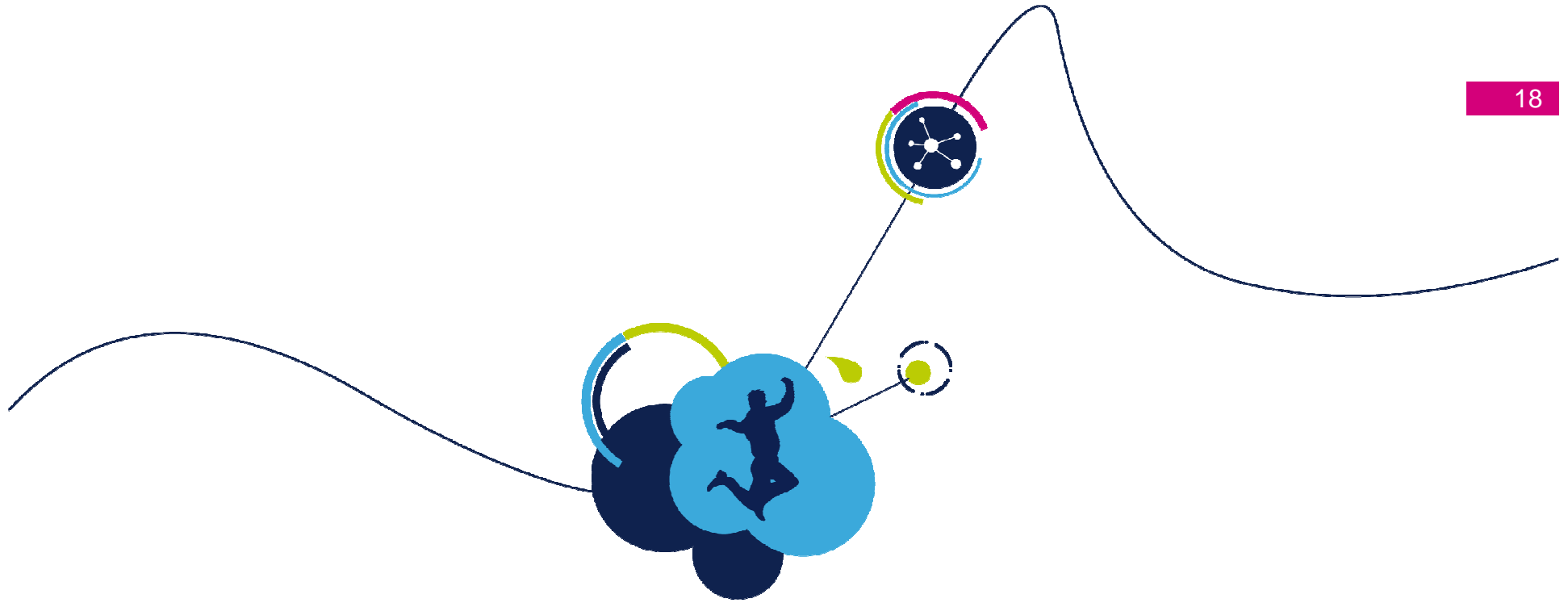


## Modeling



## Measurements

Algorithm	speed	Power
Image Signal Processing	30fps	82mW
Face detection	10fps	39mW
Face Identification	10fps	21mW
Human Body detection	3.6fps	50mW

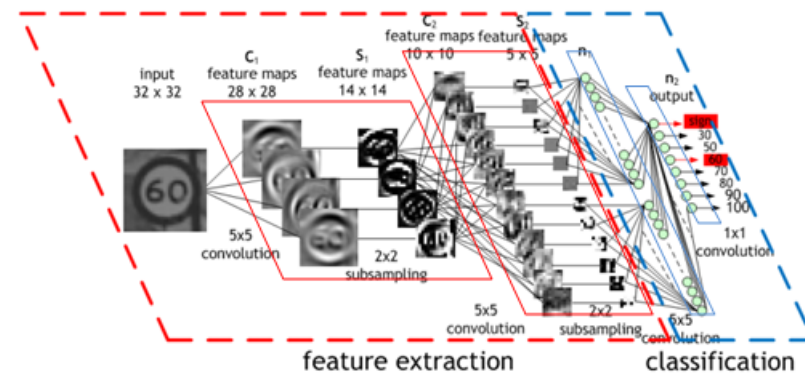


# Next steps and directions for 3D

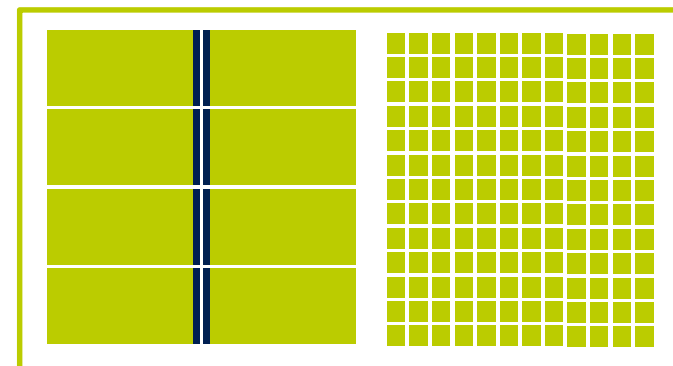
# Convolutional Neural Networks

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- State of the Art convolutional neural networks are now delivering high performances for classification and detection.
- Their integration in constrained systems is however still challenging in term of:
  - Memory size
  - Memory bandwidth/granularity
- 3D is helping as:
  - Stacking a 3rd layer for increasing total memory budget
  - Providing a direct interconnect b/w a layer of small distributed memories and a layer of HW accelerators.



## Memory layer



Large banks (regular cores)      Distributed fine grain (CNN and HW acceleration)

# 3D directions over target markets

## Markets

## Architectures

## 3D requirements

### Automotive imagers



- ISO 26262
- Image Signal Processing
- Minimal thermal dissipation
- Security



- Mid resolution
- Integrated ISP chain
- Complex safety features
- Advanced low power node
- Security functions



- 2 Layers 3D device
- Pitch interconnect: med pitch

### Specific pixels

- Event based imagers
- Global shutter
- Flicker free



- Mid resolution
- Pixel split on 2 layers



- 2 Layers 3D device used for pixel split
- Pitch interconnect: pix pitch



### Conventional imagers

- Pixel quality optimization
- X/Y dimensions (Cost and size)
- Readout speed
- Power consumption

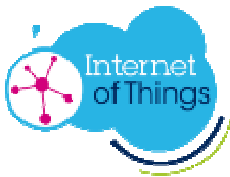


- Large resolution
- Multiple readouts
- Some ISP functions
- Advanced low power node



- 2 Layers 3D device
- Pitch interconnect: med pitch

### Smart imagers



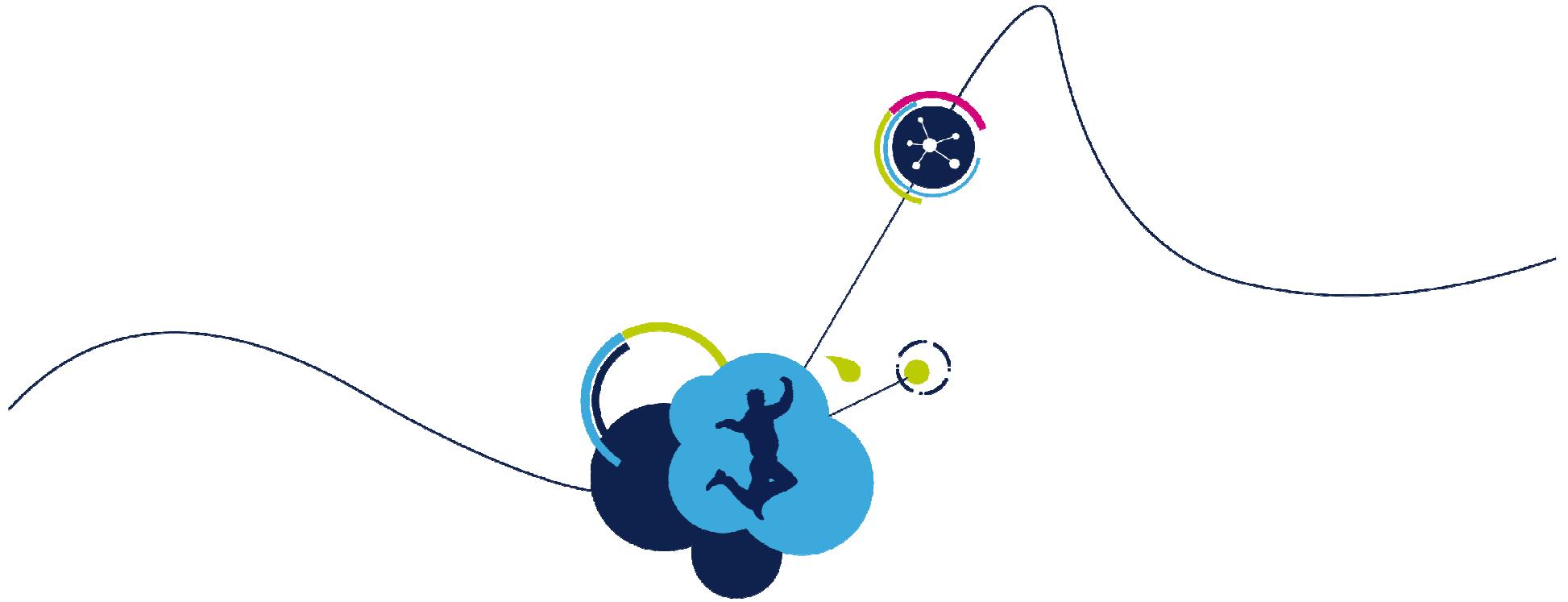
- Ultra low power consumption
- Computer vision
- Security



- Small resolution
- Multi-core processing
  - Large memories
- Neuronal processing
  - Many distributed memories



- 3 Layers 3D device
  - Imager layer
  - Processing layer
  - Memory layer
- Pitch interconnect: small pitch



Thanks for your attention