MANCHESTER 1824

The University of Manchester

Design Considerations and Noise Issues for Heterogeneous Contactless 3-D ICs

Vasilis Pavlidis

Advanced Processor Technologies Group

School of Computer Science

University of Manchester

http://www.cs.man.ac.uk/~pavlidiv/

Outline

- Contactless 3-D Integration
- Interference due to Inductive Links
- Crosstalk Noise in Contactless ICs
- Design of Heterogeneous Inductive Links
- Summary

Contactless 3-D ICs

- Alternative to wired 3-D implementations
- Several advantages over TSV and microbumps
  - Compatible with standard CMOS lithography
  - No need for level shifters
  - Reduced ESD protection
- Stacking at affordable cost
- EM field coupled interfaces
  - Inductive links
  - Capacitive links

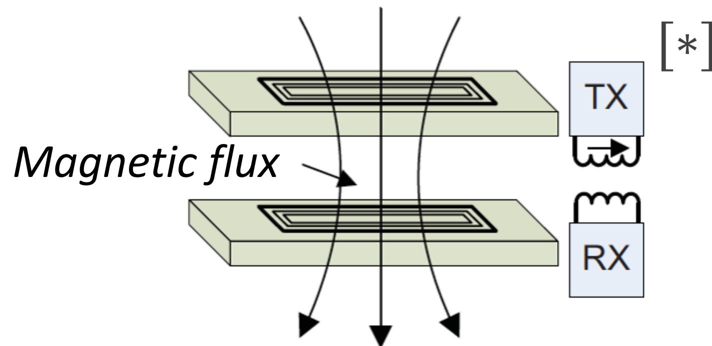
Contactless Inter-Tier Interfaces

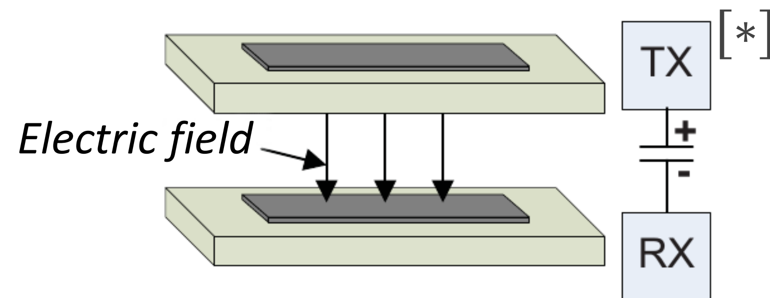
Inductive links

- Manipulates magnetic flux between on-chip inductors
- Current driven
- Long communication distances
- Support multiple integration styles

Capacitive links

- Manipulates electric field between capacitor plates
- Voltage driven
- Short communication distances
- Limited to face-to-face integration



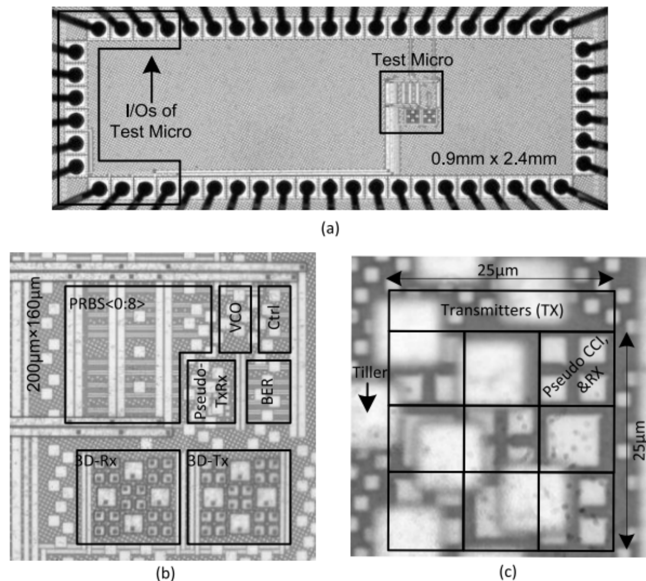


[∗] *J. Ouyang et al, "Evaluation of Using Inductive/Capacitive Coupling Vertical Interconnects in 3-D Network-on-Chip," Proceedings of the International Conference on Computer-Aided Design, pp. 477-482, November 2010.*

MANCHESTER 1824
The University of Manchester

State-of-the-Art Capacitive Links

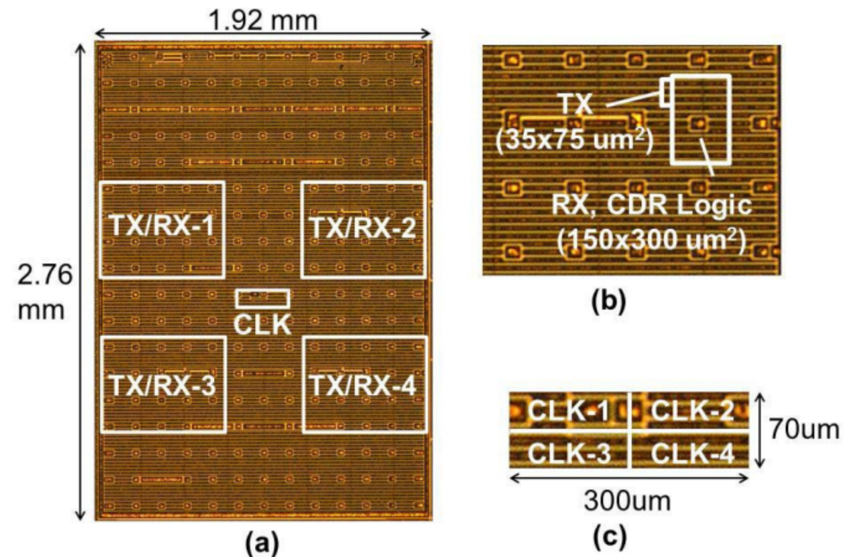
- **Crosstalk cancelled capacitive coupling**



- 65 *nm* process
- 2.31 *Gb/s/ch*
- 53 *µW/Gb/s*

Aung et al., "2.31-Gb/s/ch Area-Efficient Crosstalk Cancelled Hybrid Capacitive Coupling Interconnect for 3-D Integration," IEEE Transactions of Very Large Scale Integration, Vol. 24, No. 8, pp. 2703-2711, August 2016.

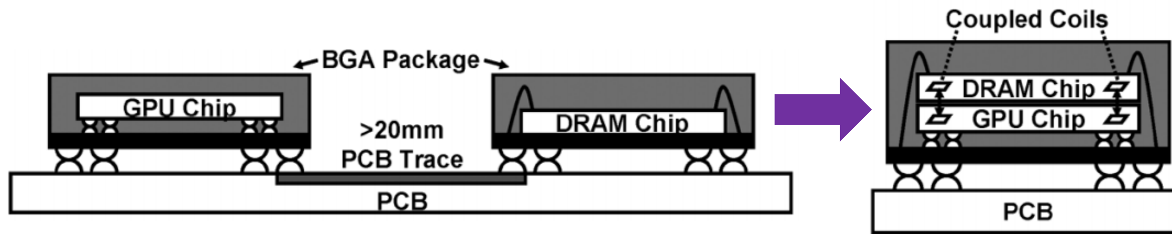
- **Bi-directional 4 channel capacitive link**

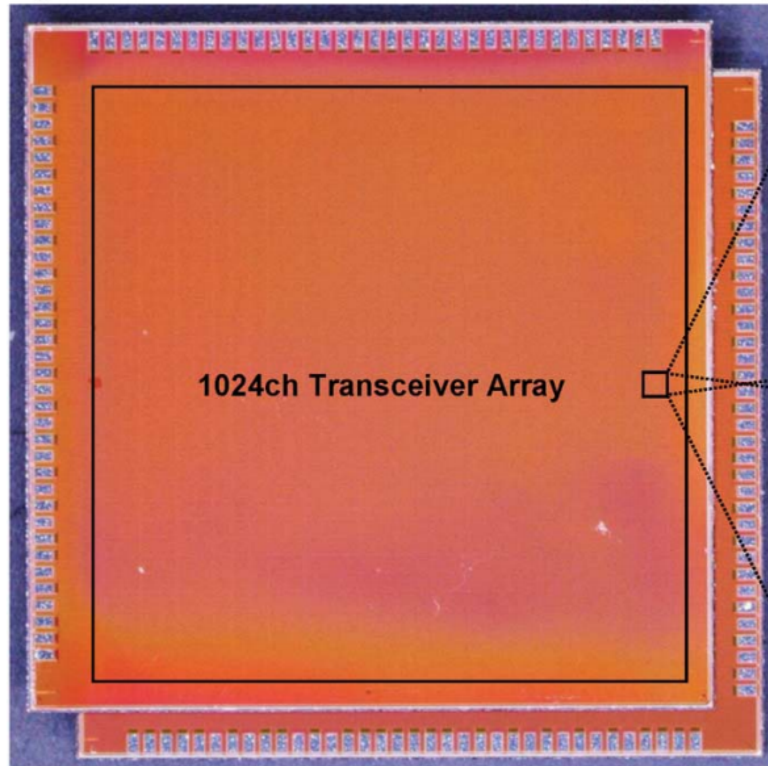


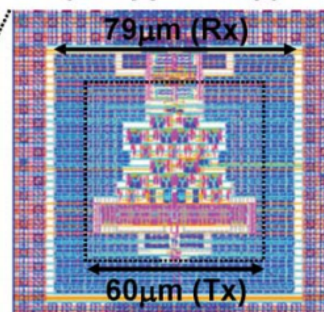
- 14 *nm* process
- 32 *Gb/s*
- 4 *pJ/bit*

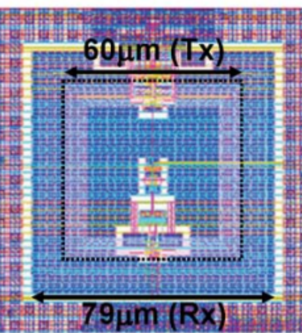
Thakkar et al., "A 32 Gb/s Bidirectional 4-channel 4pJ/b Capacitively Coupled Link in 14 nm CMOS for proximity Communication," IEEE Journal of Solid-State Circuits, Vol. 51, No. 12, pp. 3231-3245, December 2016.

State-of-the-Art Inductive Links









- 1 *TB/s* from 1024 transceivers
- 1 *pJ/bit*
- 20 *μm* separation distance
- BER < 10^{-16}
- 65 *nm* process

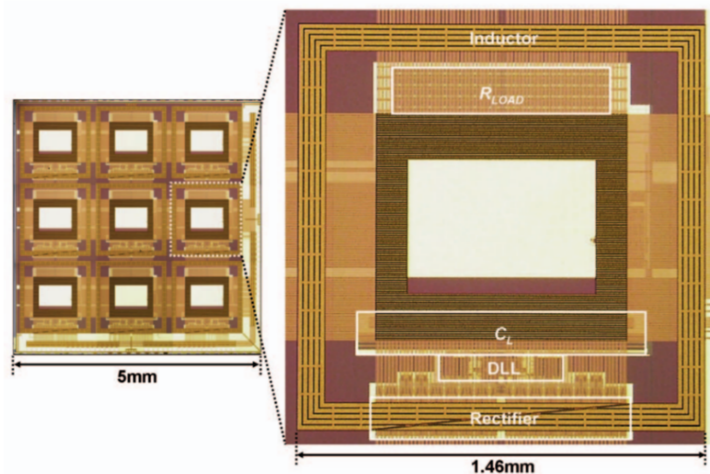
N. Miura et al., "A 1 TB/s 1 pJ/b 6.4 mm²/TB/s QDR Inductive Coupling Interface Between 65-nm CMOS Logic and Emulated 100-nm DRAM," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol. 2, No. 2, pp. 249-256, June 2012.

MANCHESTER
1824

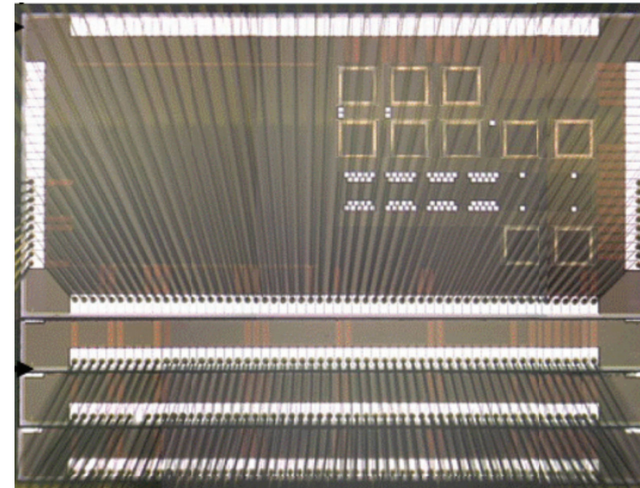
The University
of Manchester

Applications of Inductive Links

- **Non-contact wafer level testing**



- **3-D multicore CPU**

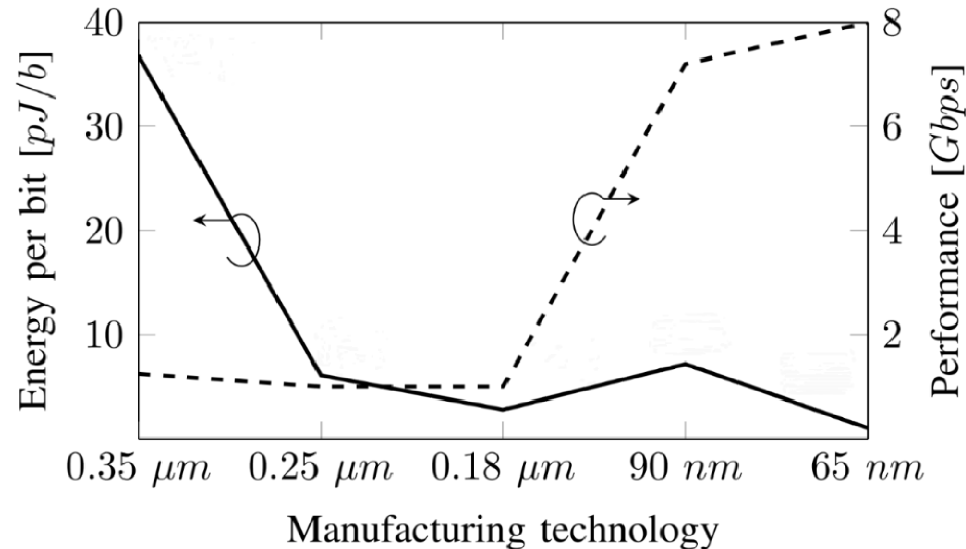


- Potential platforms for novel inductive links include
  - Internet of things edge devices
  - Biomedical circuits and micro-fluidic sensors

A. Radecki et al., "6W/25mm² Inductive Power Transfer for Non-Contact Wafer-Level Testing," Proceedings of the International Solid-State Circuits Conference, pp. 230-233, February 2011.

N. Miura et al., "A Scalable 3D Heterogeneous Multi-Core Processor with Inductive-Coupling ThruChip Interface," Proceedings of IEEE Cool Chips XVI, pp. 1-3, April 2013.

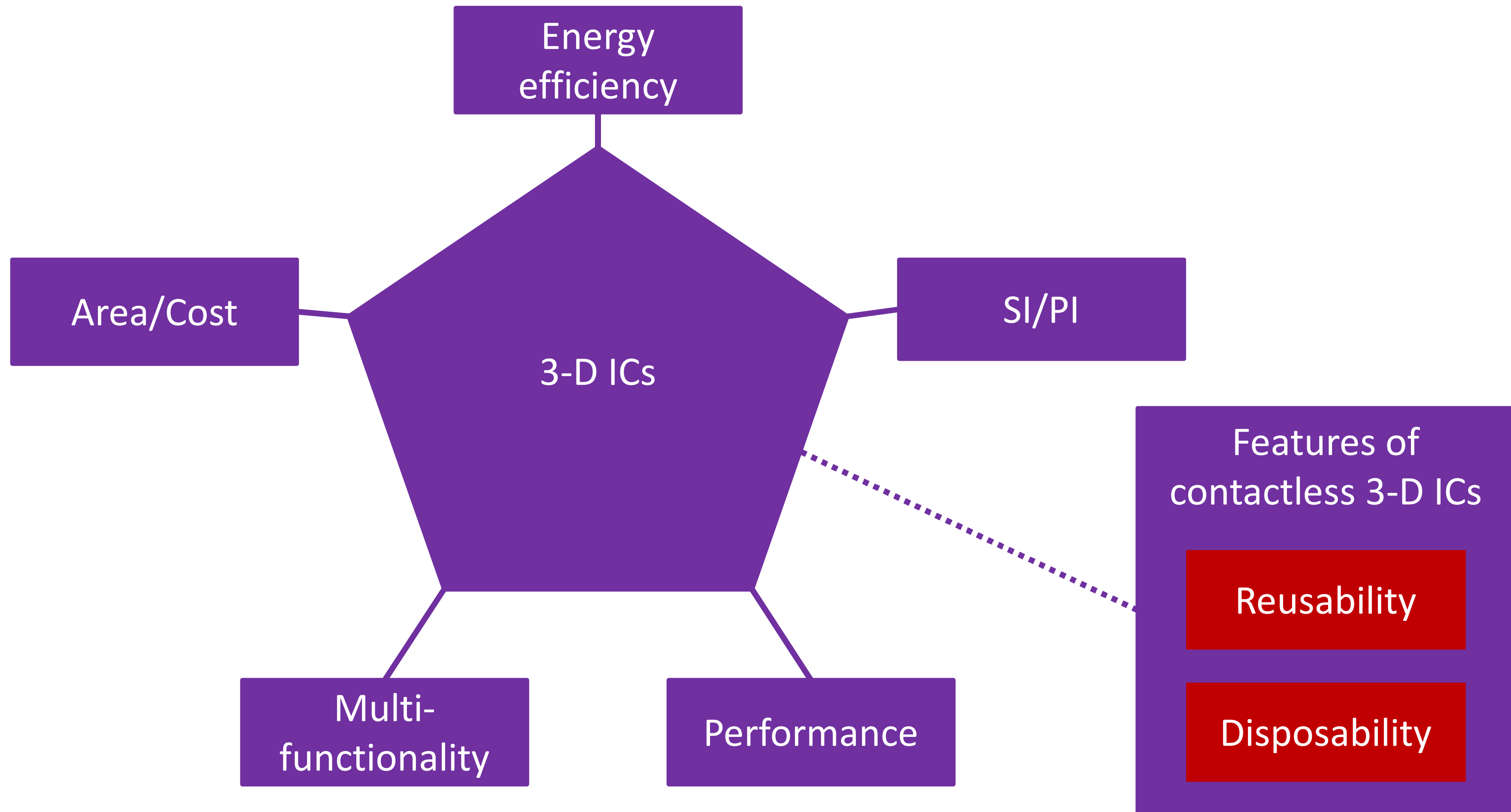
Evolution of Inductive Links



- Logic-memory applications
- Energy per bit
  - 1 *pJ/bit*
- Maximum performance
  - 8 *Gbps*

- Heterogeneous contactless systems have not been investigated
- Design considerations differ for heterogeneous systems

Design Space for (3-D) ICs



Challenges in Inductive Link Design

- Interference with noise sensitive components in the vicinity requires attention
- Crosstalk effects due to inductive links can affect inter-tier communication and power integrity
- Large currents flowing the inductor induce thermal effects and possible reliability issues
- Scaling in deep-submicrometer technologies is demanding
  - On-chip interconnects exhibit increasing resistance
  - Low voltage operation requires complex transceivers

Outline

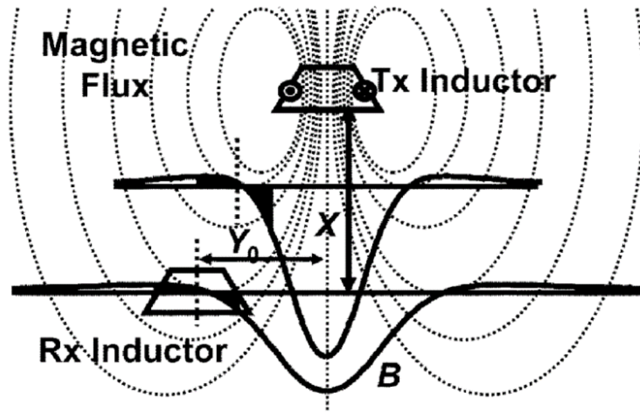
- Contactless 3-D Integration
- Interference due to Inductive Links
- Crosstalk Noise in Contactless ICs
- Design of Heterogeneous Inductive Links
- Summary

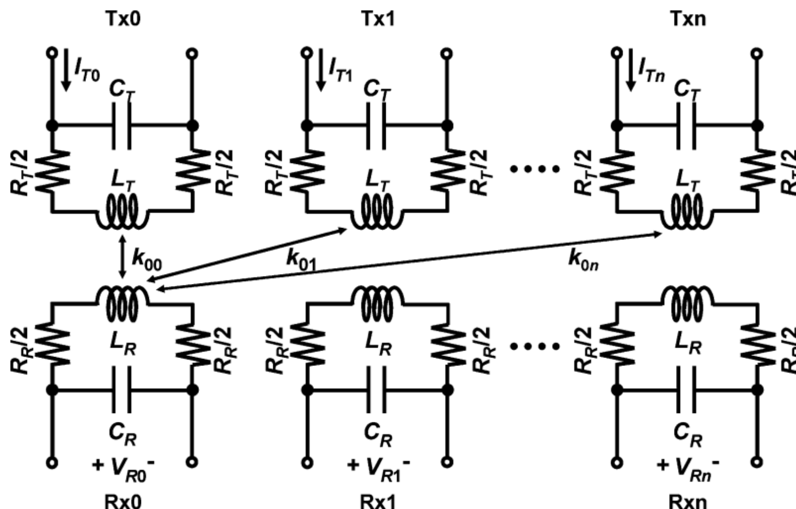
Inductive Link Interference

- Wireless signals couple with nearby circuits & interconnects
- Interference between inductive links is not negligible
- Effect varies depending upon the nature of "victim" circuit
- "Victim" circuits can be categorized as
  - Nearby inductive links
  - Digital circuits
  - Analog and sensing circuits
  - Signal and power on-chip interconnects

Interference on Neighboring Inductive Links

[∗]





- Crosstalk to adjacent links similar to received signal (50 *mV*)
- Solutions to reduce crosstalk
  - Increase distance between links
    - Not suitable for high density applications
  - Time division interleaving technique
    - Maximum division depends upon performance constraints
    - 4-phase division sufficiently mitigates crosstalk

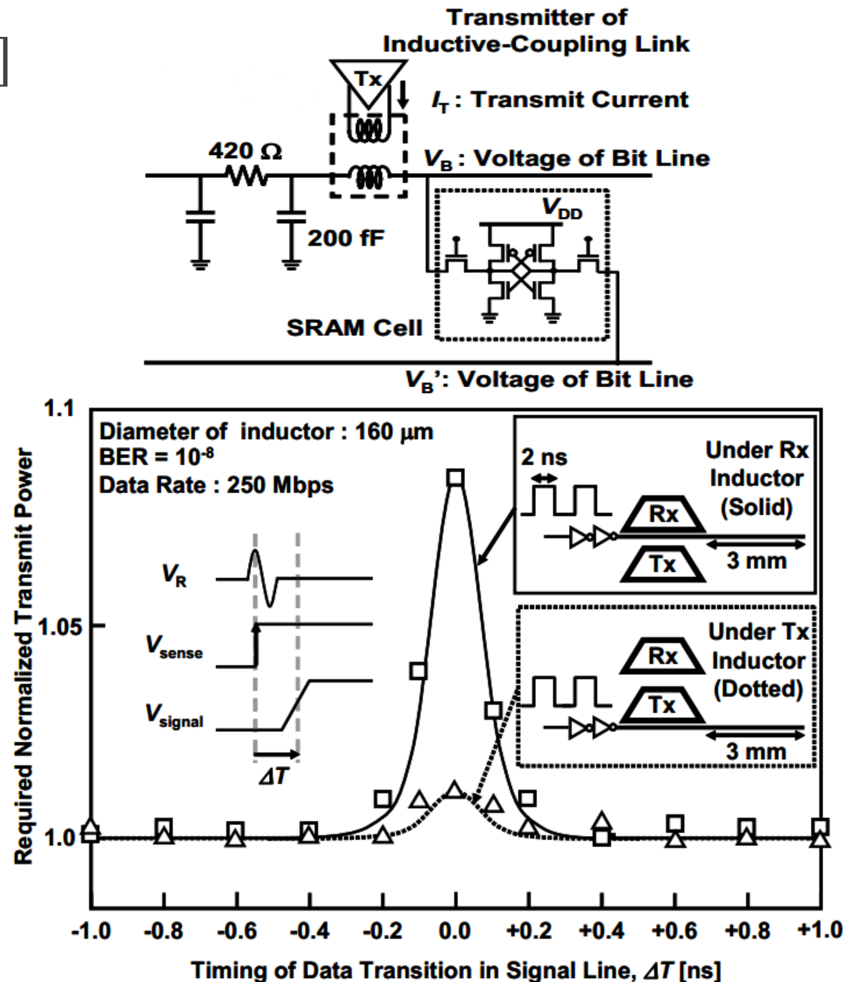
For 1 *Gbps* datarate time division

- 2-phase ⇒ crosstalk of 25 *mV*
- 4-phase ⇒ crosstalk of 10 *mV*

[∗] – *N. Miura et al., "Crosstalk Countermeasures for High-Density Inductive-Coupling Channel Array," IEEE Journal of Solid-State Circuits, Vol. 42, No. 2, pp. 410-421, February 2007.*

Interference on Circuit Components

[*]

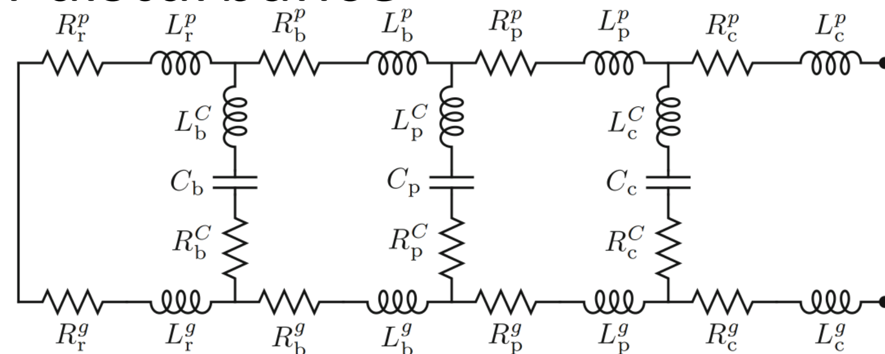


- Noise on digital circuits
  - Coupling through local interconnects
  - Crosstalk on local interconnects is negligible
    - < 1 *mV*
- Noise on global interconnects is significant
- Power integrity may be compromised in high density interfaces

[*] – *K. Niitsu et al., "Interference from Power/Signal Lines and to SRAM Circuits in 65nm CMOS Inductive-Coupling Link," IEEE Asian Solid-State Circuits Conference, pp.131-134, November 2007.*

Power Integrity in Contactless 3-D Circuits

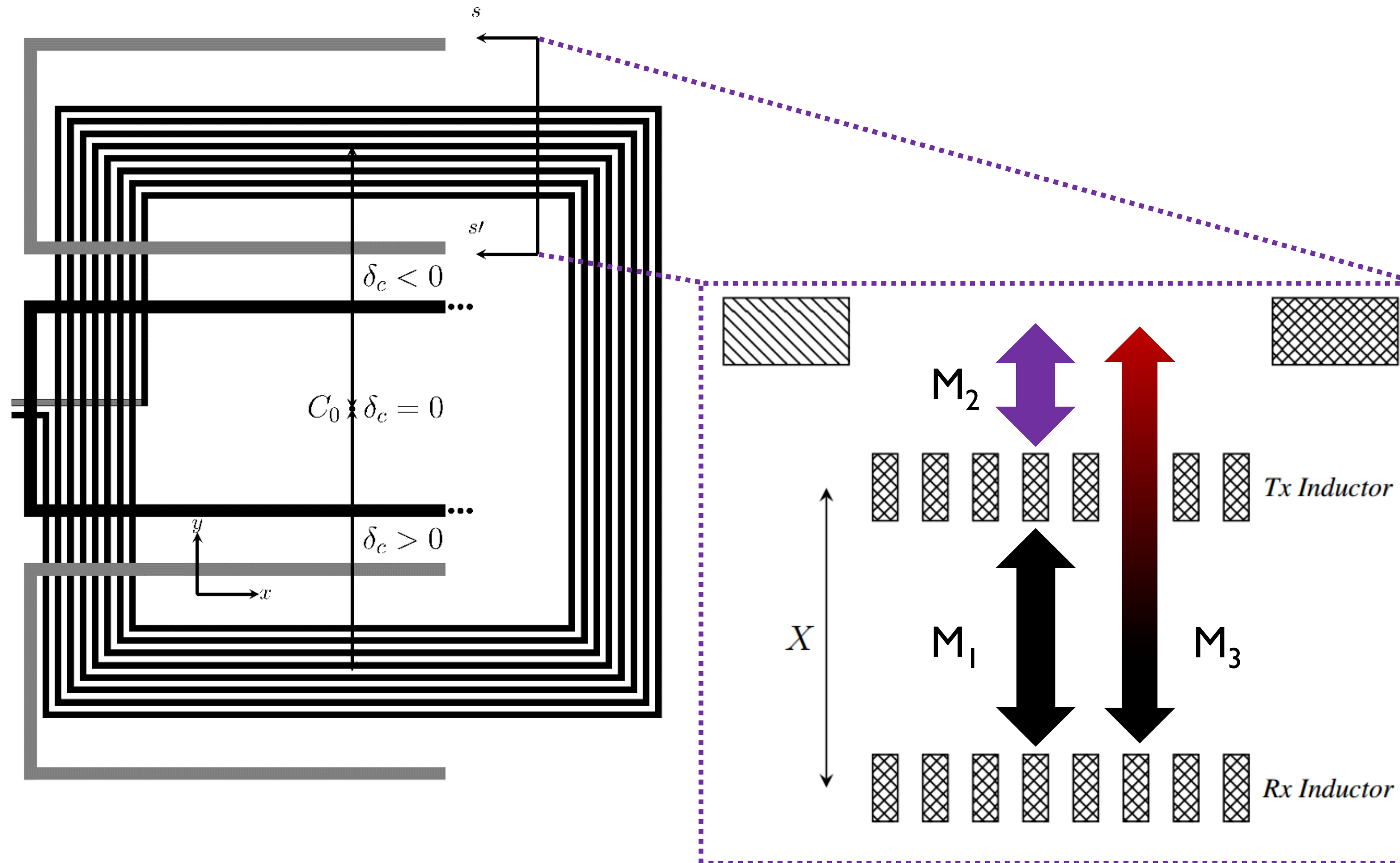
- On-chip power distribution networks (PDN)
  - Include regular topologies
  - Contain long wire segments
- Power integrity includes two types of noise
  - Resistive noise, IR drop
  - Device switching noise, $L\,{}^{di}/_{dt}$
- For contactless 3-D systems inductively induced noise can be another source of disturbance
  - Model the induced noise
  - Efficiently analyse complex structures



Outline

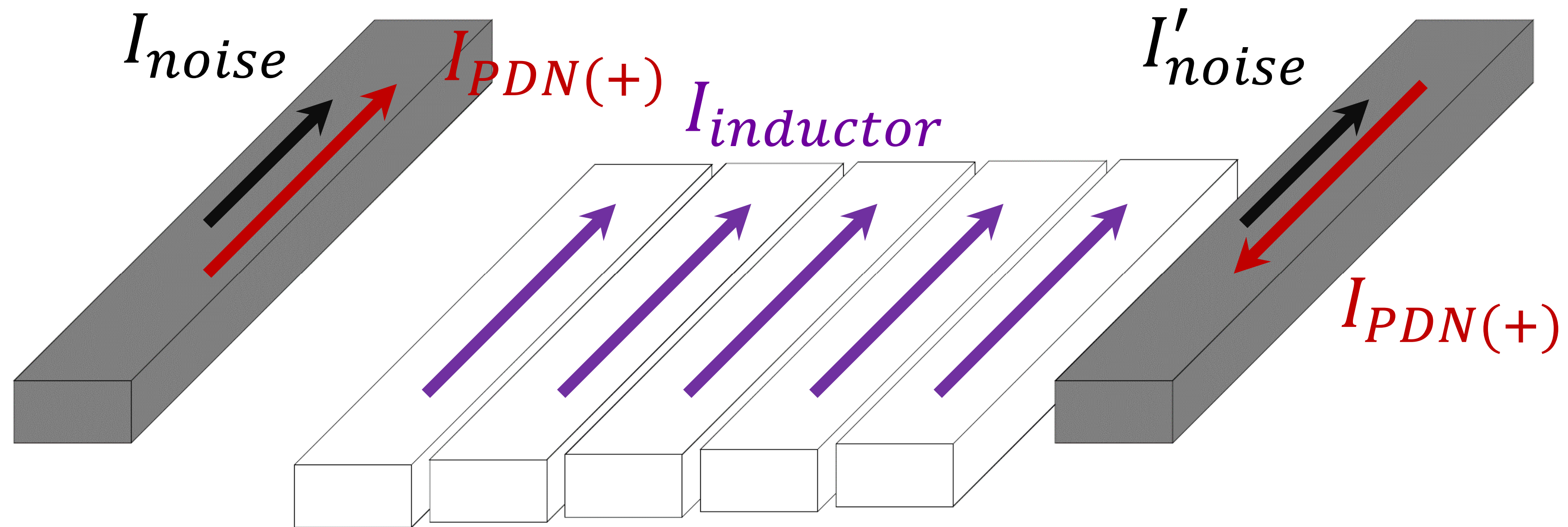
- Contactless 3-D Integration
- Interference due to Inductive Links
- Crosstalk Noise in Contactless ICs
- Design of Heterogeneous Inductive Links
- Summary

Typical Inductor & PDN Structure



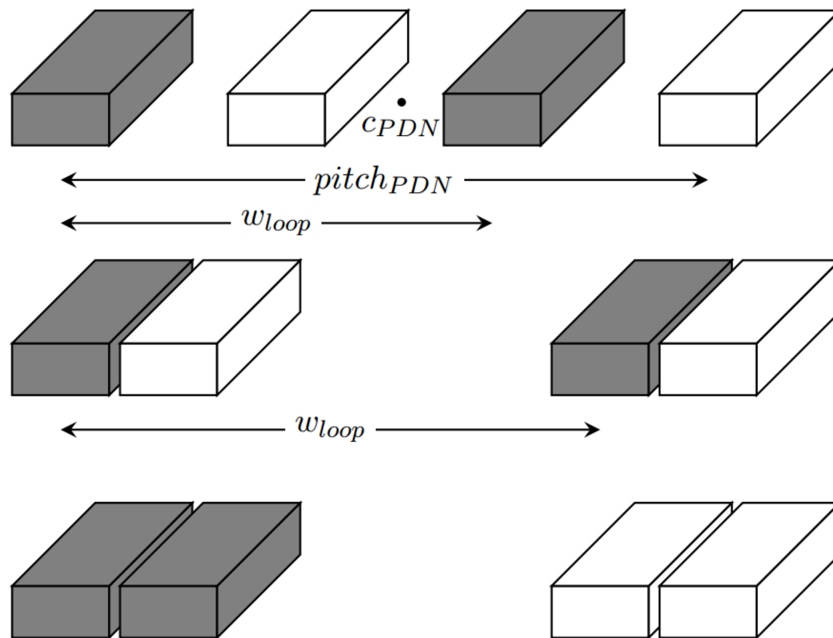
[∗] – *I. A. Papistas, V. F. Pavlidis "Crosstalk Noise effects of On-Chip Inductive Links on Power Delivery Networks, Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 1937-1941, May 2016.*

Induced Crosstalk Noise



- $I_{PDN,acc} = I_{PDN} + (I_{noise} - I'_{noise})$
- Total induced current is minimised

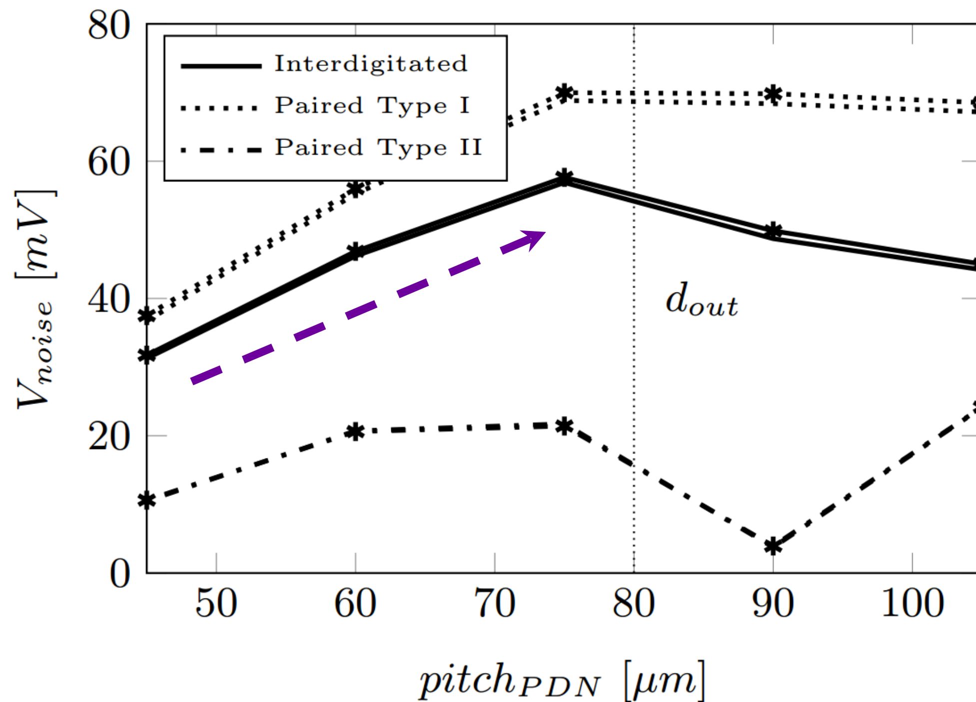
PDN Topologies



- Different PDN topologies have been explored
  - Interdigitated
  - P-G/P-G, paired type I
  - P-P/G-G, paired type II
- Paired type II exhibits overall lowest susceptibility

MANCHESTER 1824
The University of Manchester

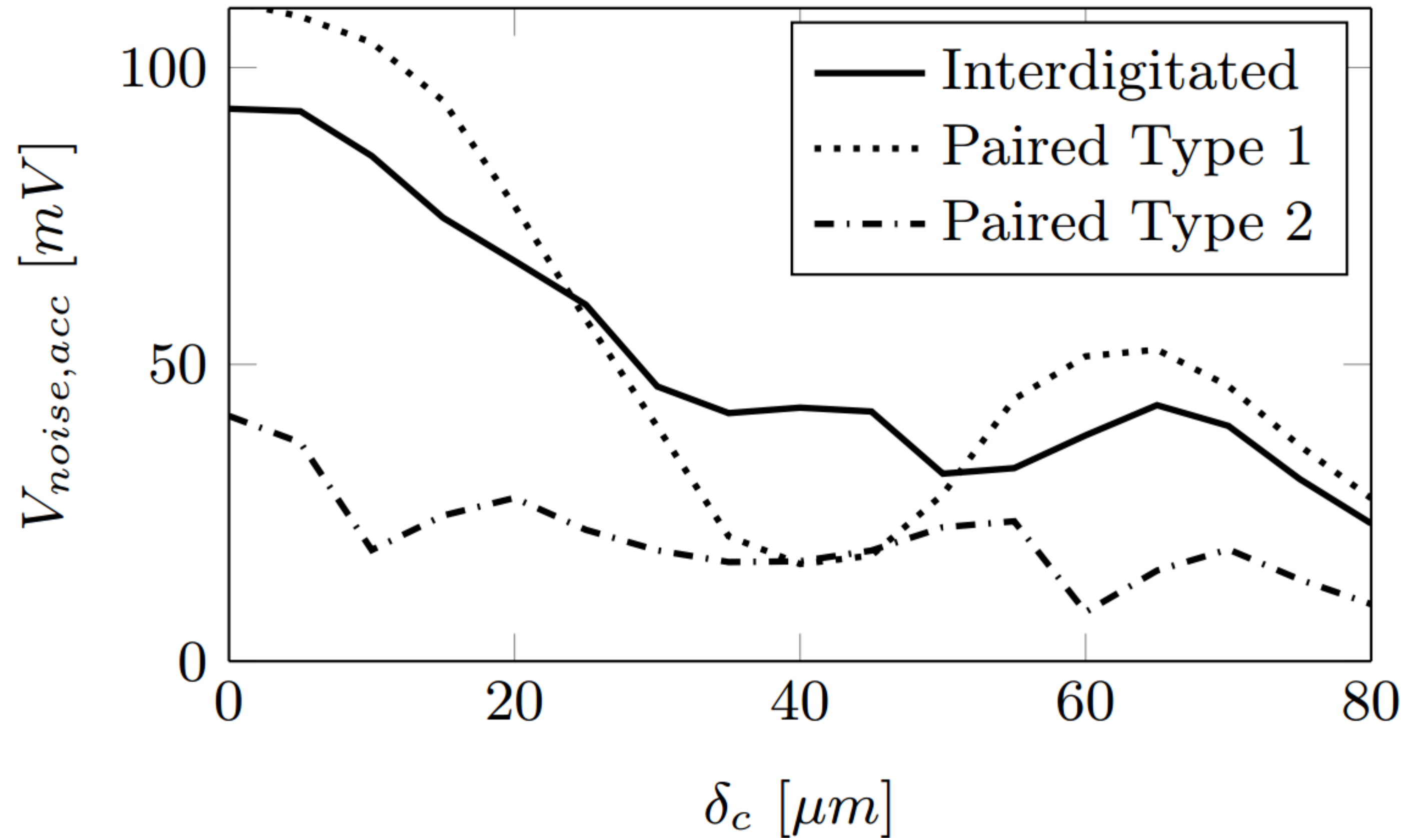
Crosstalk Noise – PDN Pitch



- For $pitch_{PDN} < d_{out}$
  - Noise increases with pitch
- As $pitch_{PDN} > d_{out}$
  - Noise is reduced
- Paired type I presents highest noise susceptibility
- Paired type II the lowest

[∗] – *I. A. Papistas, V. F. Pavlidis "Inter-Tier Crosstalk Noise On Power Delivery Networks for 3-D ICs with Inductively-Coupled Interconnects, Proceedings of the ACM Great Lakes Symposium, pp. 257-262, May 2016.*

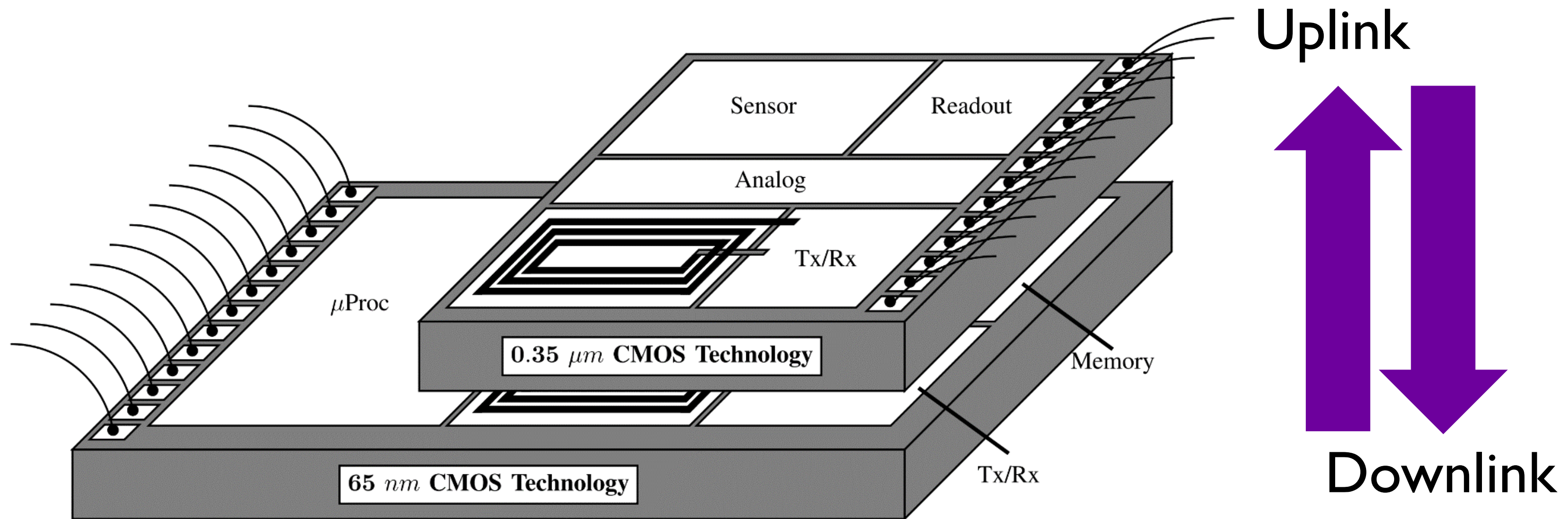
Crosstalk Noise for Varying δ_c



Outline

- Contactless 3-D ICs
- Interference due to Inductive Links
- Crosstalk Noise in Contactless ICs
- Design of Heterogeneous Inductive Links
- Summary

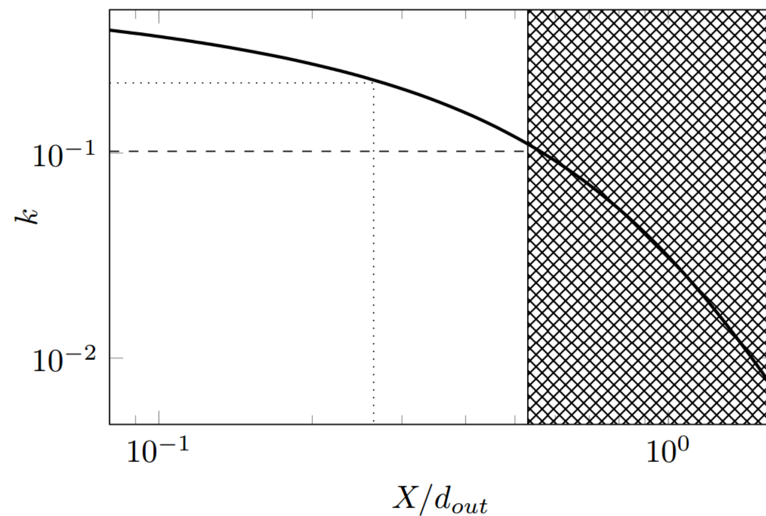
Heterogeneous Contactless Stacked Circuit

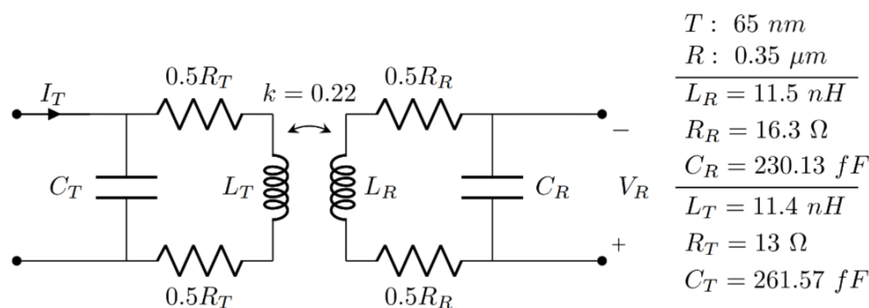


- Processing tier in 65 *nm*
- Sensing tier in 0.35 *μm*
- Stacked face-up for fluidic sensing applications
- Half duplex communication supported
- Substrate thinned to 80 *μm*

[∗] – *I. A. Papistas, V. F. Pavlidis "Contactless Inter-Tier Communication for Heterogeneous 3-D ICs, Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 2585-2588, May 2017.*

Area Considerations



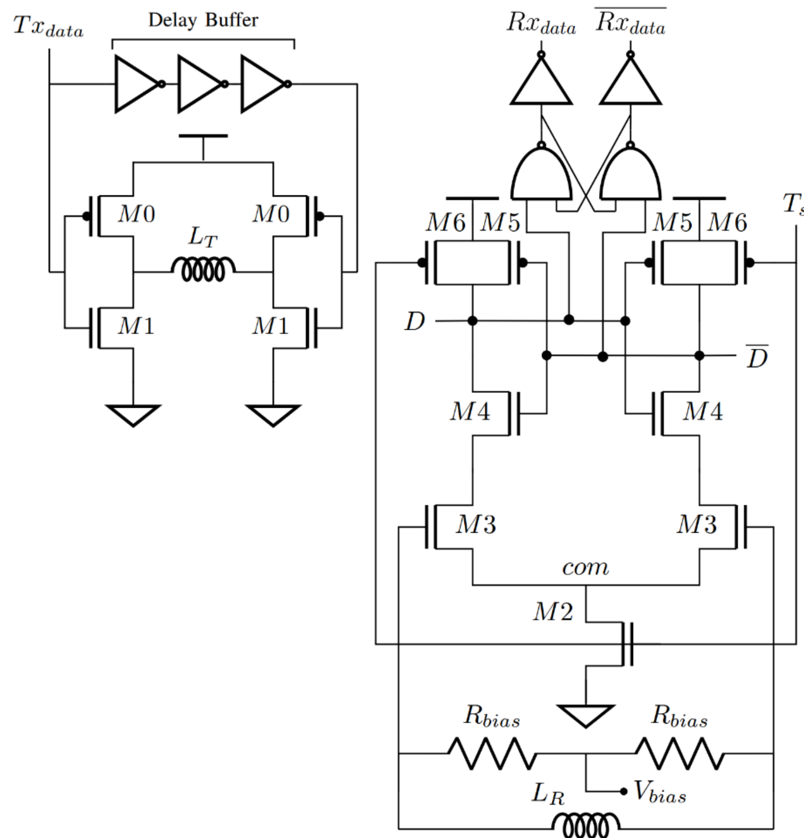


- Coupling depends upon outer diameter and communication distance
- Minimum coupling $k = 0.1$
- This example
  - $k = 0.22$
  - $d_{out} = 300\ \mu m$
- DRC/DFM free inductor layout using VeloceRF*
- Both inductors used for data transmission and reception

VeloceRF User Manual, v2, Helic, Inc., November 2013.

MANCHESTER 1824
The University of Manchester

Transceiver Circuit



- Transceiver circuit
  - H-Bridge transmitter
  - Sense amplifier receiver
- Received pulse is sampled within a specified time interval
  - Crosstalk noise and accidental switches are reduced
- Biasing of differential pair important for circuit operation

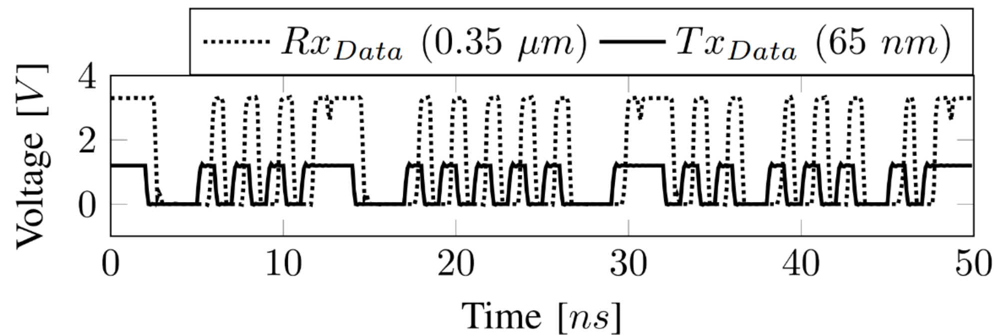
MANCHESTER 1824

The University of Manchester

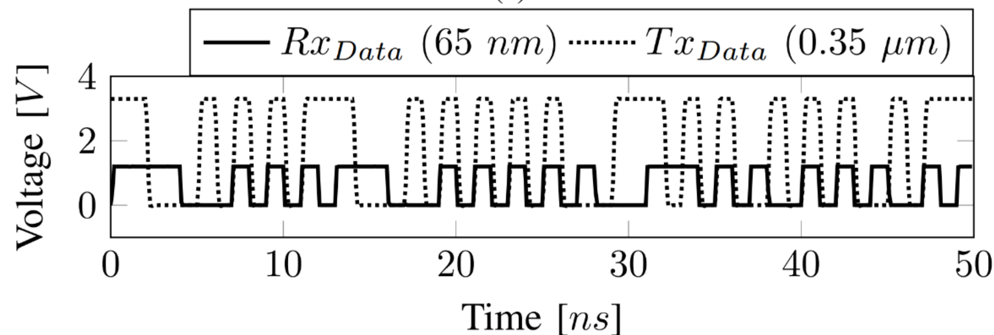
Methodology for Power Efficiency

- Power efficiency is the primary objective
  - $P_{tot} = P_{Tx65} + P_{Tx350} + P_{Rx65} + P_{Rx350}$
- Two design approaches can be followed
  - Minimization of each power component individually
  - Consideration of core voltage in each process node
- Tradeoff between power and sensitivity exists
  - 0.35 μm tier sized for minimum power
    - Sensitivity of 300 mV
  - 65 nm tier sized for highest sensitivity
    - Sensitivity of 75 mV
- 70% decrease in 0.35 μm device width is achieved

Simulation Results



(a)



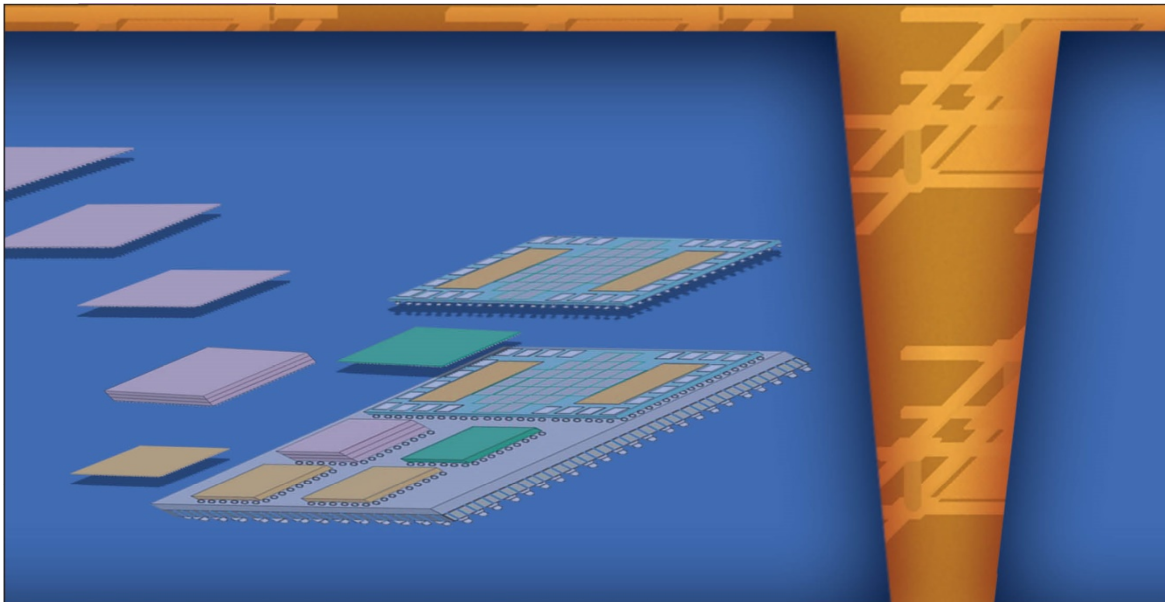
- Full swing signal at nominal voltage
- No level shifters required
- P_{uplink} = 5.28 mW
  - $P_{uplink, avg}$ = 2.5 mW
- $P_{downlink}$ = 8.67 mW
  - $P_{downlink, avg}$ = 2.38 mW

Outline

- Contactless 3-D Integration
- Interference due to Inductive Links
- Crosstalk Noise in Contactless Ics
- Design of Heterogeneous Inductive Links
- Summary

Summary

- Inductive links crosstalk noise on PDNs is not negligible
- PDN topologies exhibit different sensitivity to noise
- Noise-aware PDN placement can supress this type of induced noise up to 70%
- The design space changes for heterogeneous 3-D ICs
- Exploiting the sensitivity versus power tradeoff
  - Significant decrease in device sizes and therefore in power is achieved



THREE-DIMENSIONAL INTEGRATED CIRCUIT DESIGN

2ND EDITION

Available: mid-July 2017
Morgan Kaufmann Publishers

Thank you!

MK
MORGAN KAUFMANN

VASILIS F. PAVLIDIS
IOANNIS SAVIDIS
EBY G. FRIEDMAN