CHIP-TO-CHIP COMMUNICATION ON INTERPOSER BASED SYSTEMS

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OUTLINE

- Motivation
- Packaging Technology
  - Silicon Interposer
- System Description
  - Fiber-optic backbone
  - HBM Memory
- Summary and Outlook

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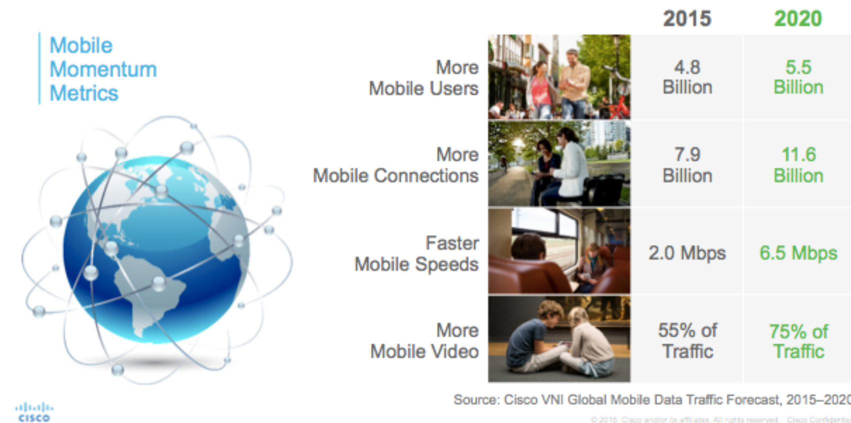
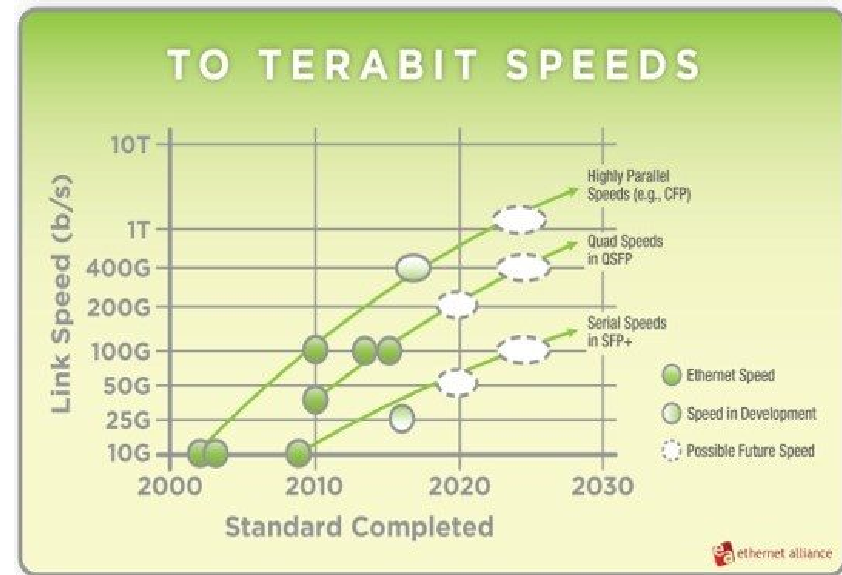
Motivation

- Very high traffic for communication
- Backbone: fiber optic
- 200GSample/s sample rate by 6 bits results in much more than 1Tbit/s data rate
- Heterogeneous integration necessary
  - High end ADC/DAC (mostly SiGe)
  - FPGA/DSP newest CMOS technology





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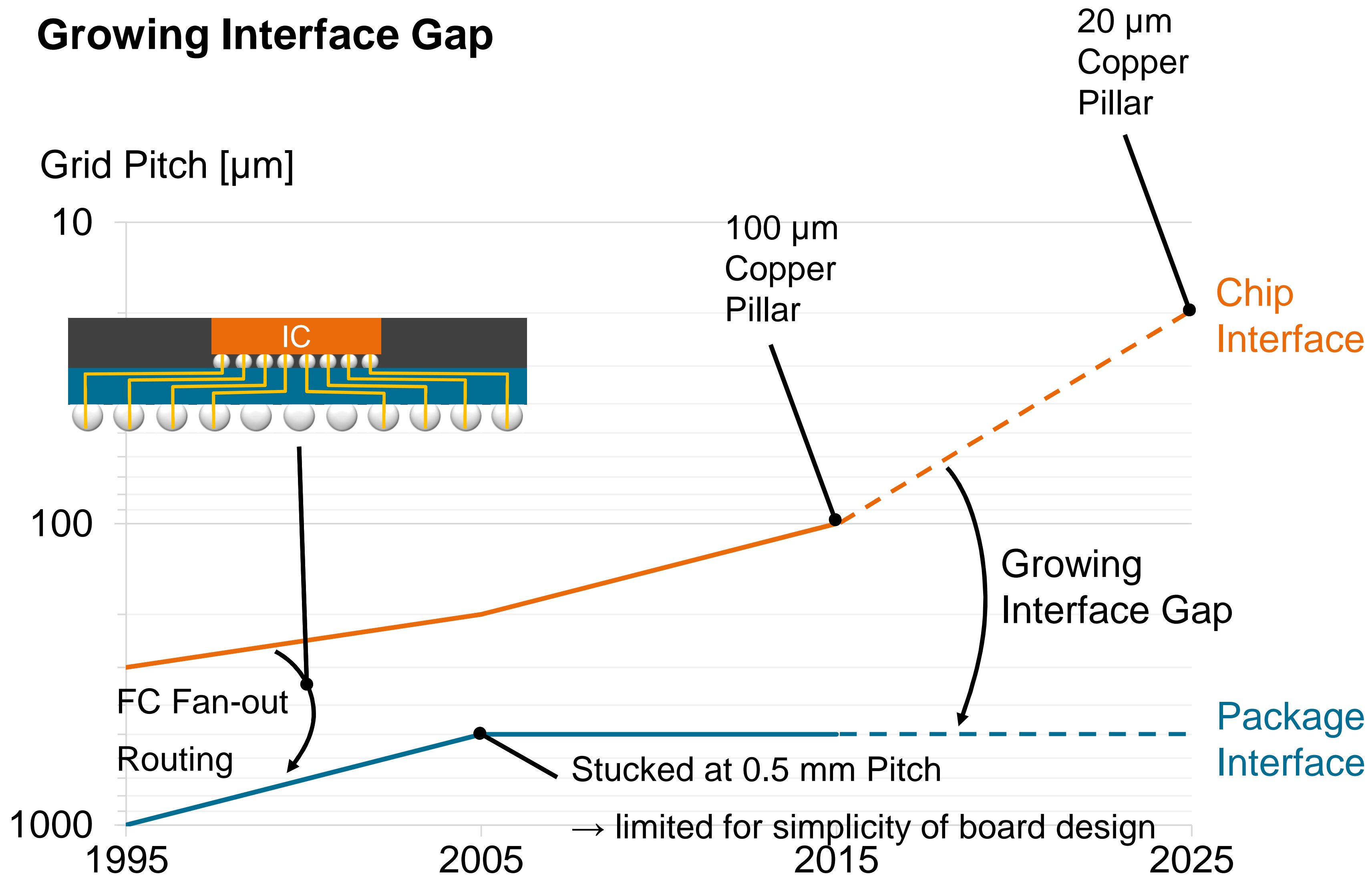
Motivation
Growing Interface Gap



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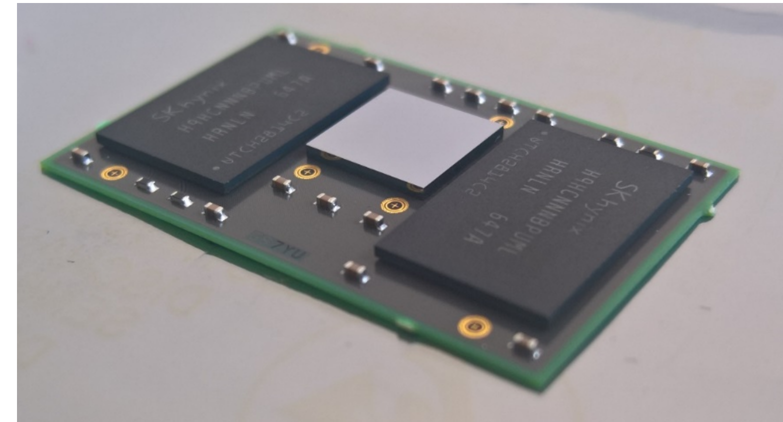
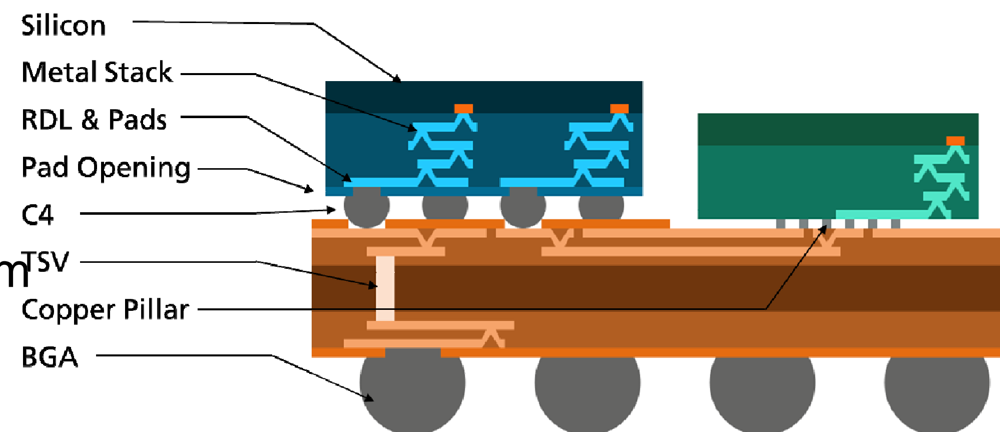
Packaging Technology
Substrates

- Printed circuit board
  - Various possibilities
  - Limited minimal line width and spacing ≈ 50 um
  - Substrate thickness down to 300 um
- Interposer
  - High density routing
  - Low height ≈ 100 um
  - Whole system or subsystem for reuse





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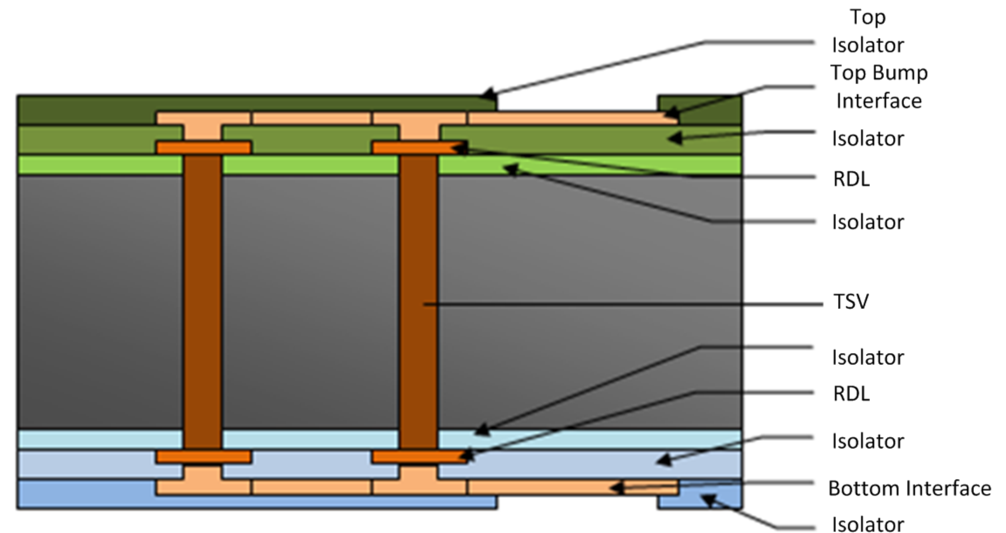
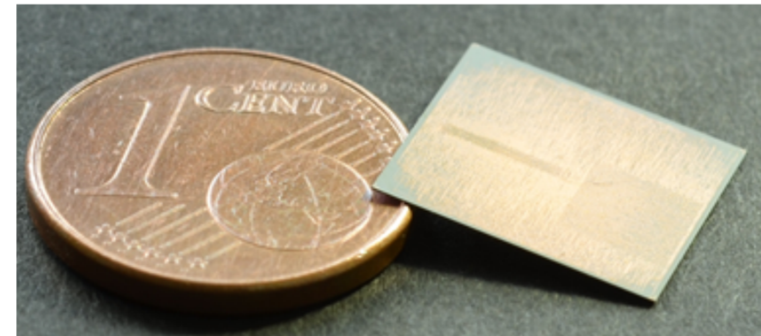
Packaging Technology
Silicon Interposer

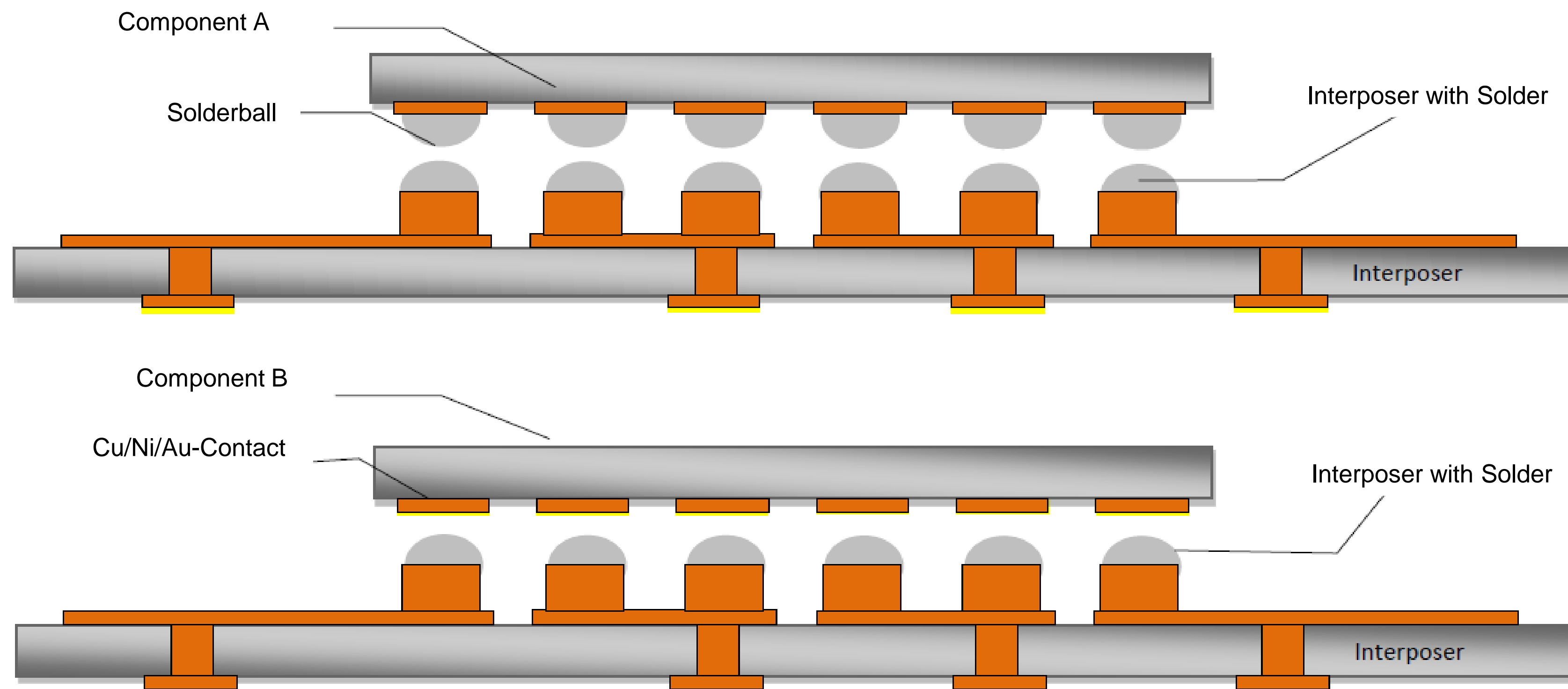
- Technology Parameters:
  - 4 µm metal width
  - 4 µm metal space
  - 10 µm diameter TSV with 100 µm height
- Up to 8 redistribution layers
- Very short interconnects
- Low shielding area costs
- Fine pitch Copper Pillar or micro-bumps (~50µm)
- Better process stability compared to organic substrates





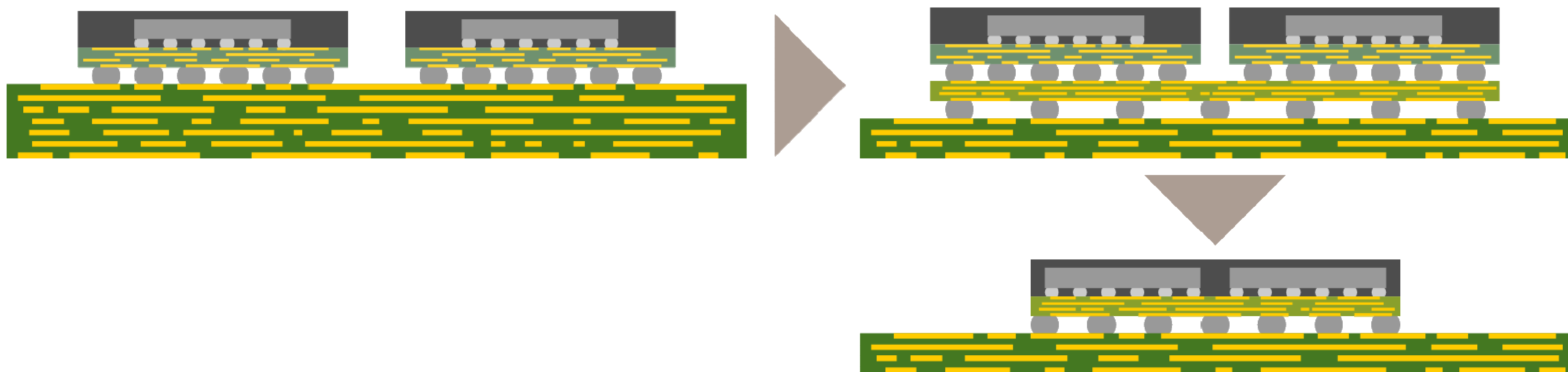
Packaging Technology
Silicon Interposer

- Assembly Options: Mixture of SMD, WLCSP or bare-die



Packaging Technology
Silicon Interposer

- System Options
- Modularization
  - Reduce NRE (non-recurring engineering costs)
  - Concentrate complexity where it occurs
  - Optimize modules on package level



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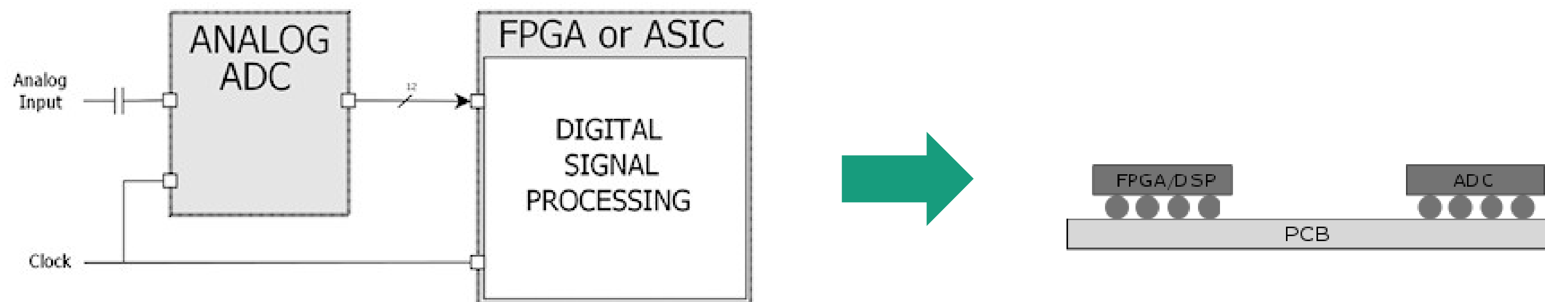
System Description Fiber Optic Backbone
Current Systems

- 50GSample/s data rate by 4 bits resolution results in much more than 200Gbit/s
- Usage of high speed SERDES interface with 12.8Gbit/s -> 20 channels
- 20 channels results in total of around 100 pins; area ≈ 4 mm^2
- ADC area in IC around 4x4 mm^2



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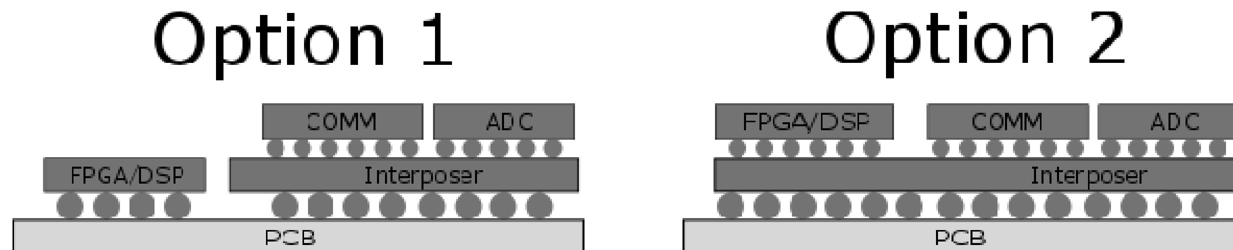
System Description Fiber Optic Backbone
Future Systems

- 1Tbit/s transfer rate between ADC and FPGA/DSP
  - ADC area in the same region 4*4 mm²
- Current FPGA/DSP solutions use 12Gbit/s interface
- Nearly 100 cannels necessary -> 200 IO pins + ~ 400 P/G pins
- SerDes are area constraint (one cell area 200 um by 800 um -> 16mm²)
- Drawbacks
  - IP cost in SiGe technology
  - Noise from SerDes to ADC
  - CMOS technology better suited for SerDes

System Description Fiber Optic Backbone
Principal Built-up

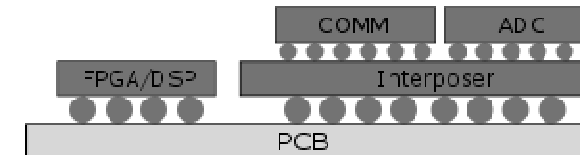
- Usage of standard interfaces necessary on the FPGA/DSP
- Idea: easy interface between the ADC to a new communication chip
- 2 Options for built-up
  - Only ADC and communication chip on interposer – smaller interposer, worse interconnects on the PCB
  - All chips on interposer – very large interposer, shorter and better interconnects



System Description Fiber Optic Backbone
Principal Built-up

- ADC in SiGe
  - Wide channel IO
- Communication ASIC
  - In CMOS
  - With same wide channel IOs
  - Standard SerDes
- Communication Channels
  - ADC<->COMM ASIC
  - COMM ASIC<->FPGA

Option 1



Gbit/s	Number of channels	Number of differential signals	Number of IOs	IO area 40/50um pitch
0.5	2000	2000	2600	5,2mm²
1	1000	1000	1400	2,8mm²
3	333	333	500	1,1mm² -> 4mm² (100um pitch)

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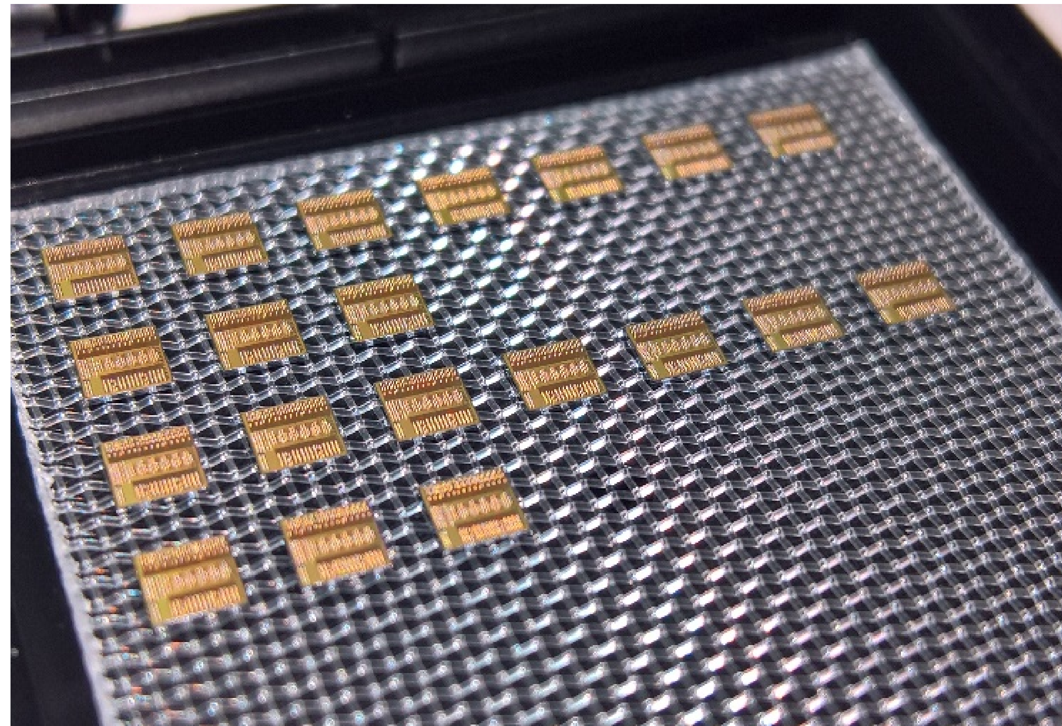
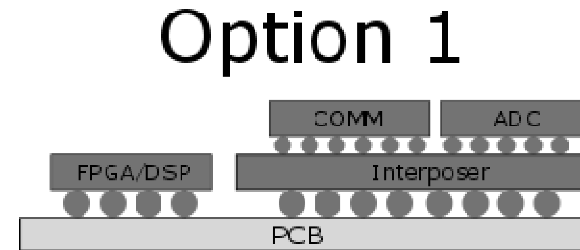
System Description
Status

- Communication Chip manufactured in GlobalFoundries 28nm SLP technology
  - Copper Pillars with 100 um pitch
  - RX and TX SerDes
  - Wide channel IOs



System Description
Status



- Interposer in Fraunhofer technology
  - Currently in production

FPGA
SERDES
SERDES
SERDES
SERDES
SERDES

ASIC
SERDES
SERDES
SERDES
SERDES
SERDES
Wide chann el IOs

Wide chann el IOs
SERDES
SERDES
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SERDES
ASIC

SERDES
SERDES
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SERDES
SERDES
FPGA

Interposer

PCB

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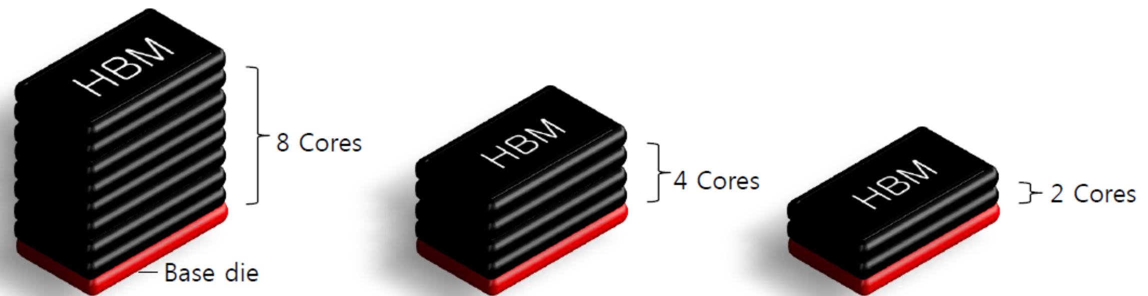
System Description HBM System
Introduction

- High Bandwidth Memory Gen 2



8Gb based	9mKGSD			5mKGSD			3mKGSD		
Density/Cube (GB)	8GB			4GB			2GB		
IO	1024			1024			1024		
Speed/pin (Gbps)	1.0	1.6	2.0	1.0	1.6	2.0	1.0	1.6	2.0
Bandwidth (GB/s)	128	204	256	128	204	256	128	204	256
Usage	HPC, Server			HPC, Server, Graphics, Network			Graphics, Cache		
Config. / system	8 / 6 / 4 Cube			4 / 2 / 1 Cube			2 / 1 Cube		

Sk Hynix

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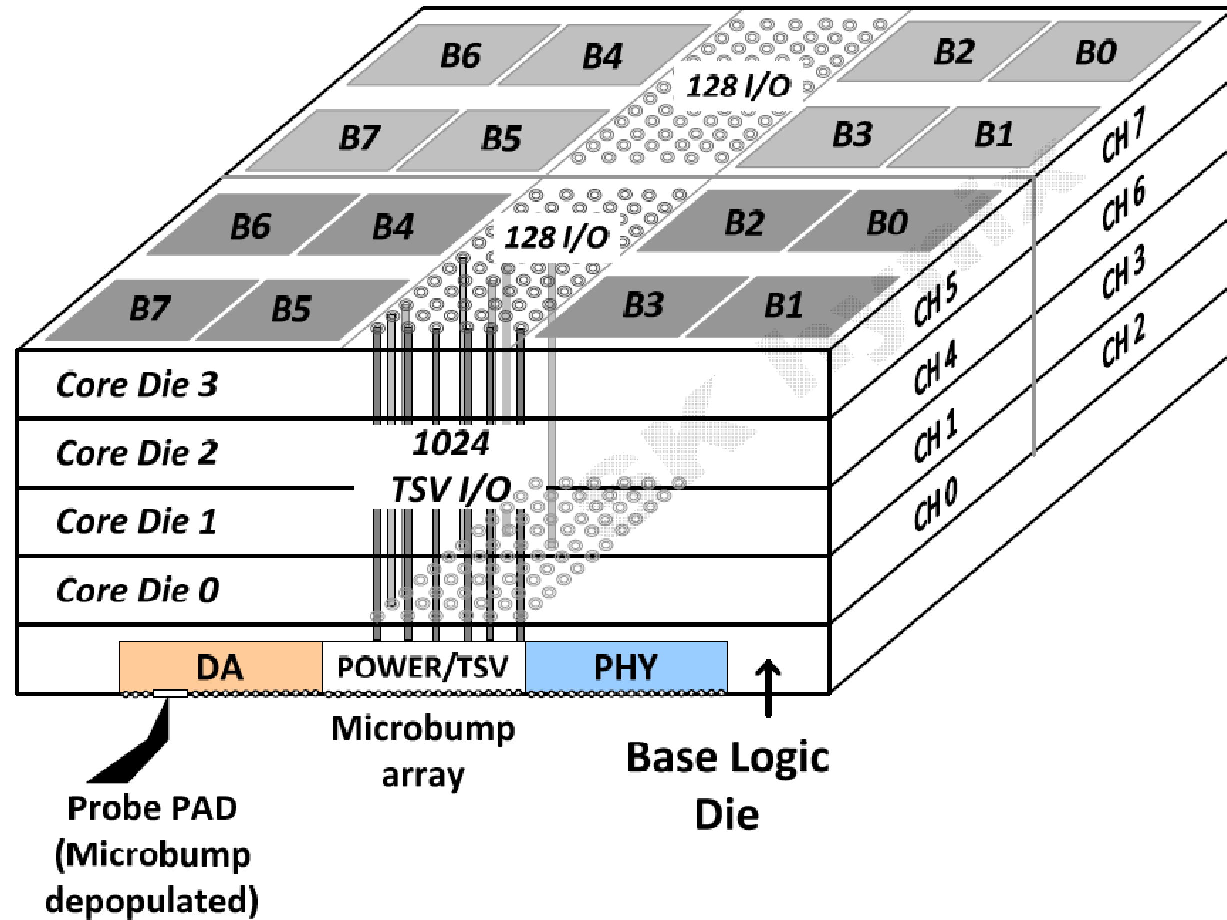
System Description HBM System
Introduction

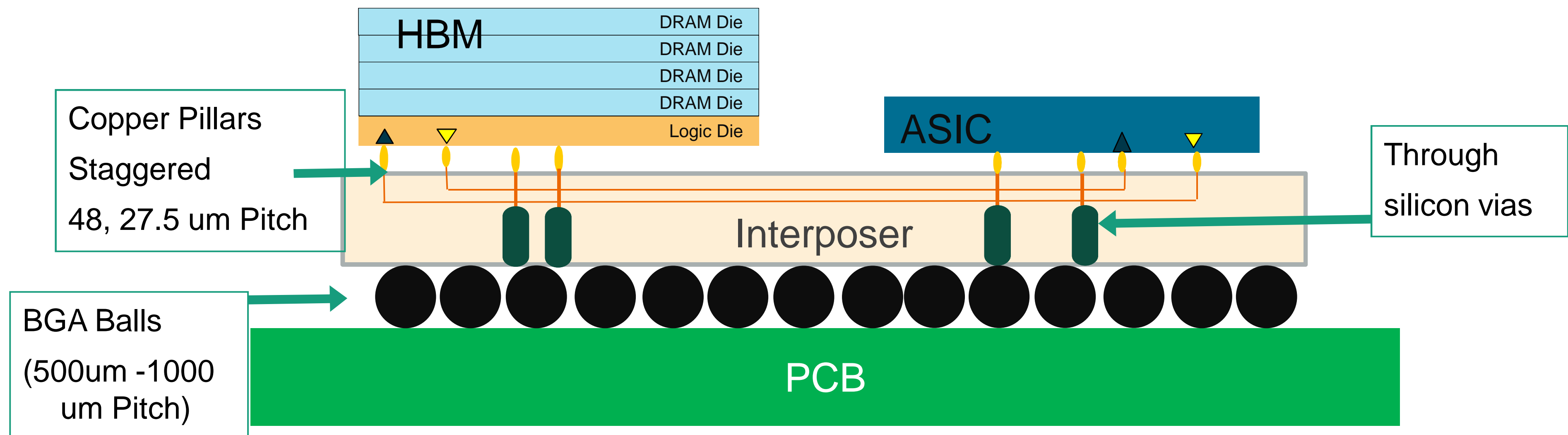
- HBM Structure



[1] D.U Lee, SK hynix, ISSCC 2014

System Description HBM System
System Build-Up

- HBM and ASIC assembled on silicon Interposer
- Bottom side of interposer ready for assembly on PCB



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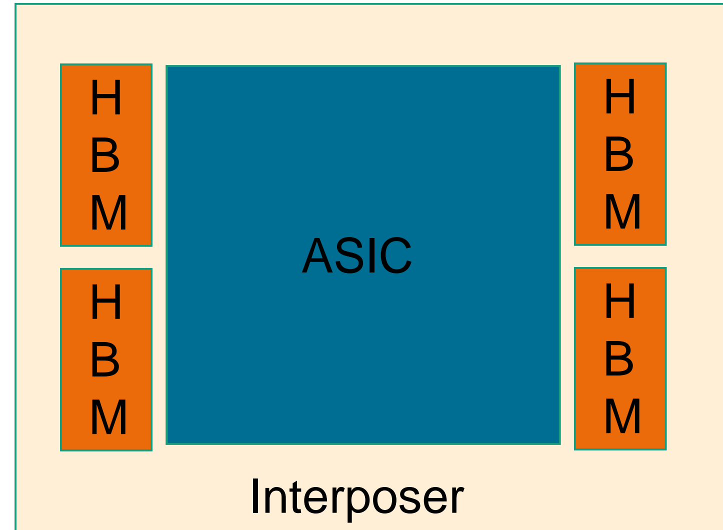
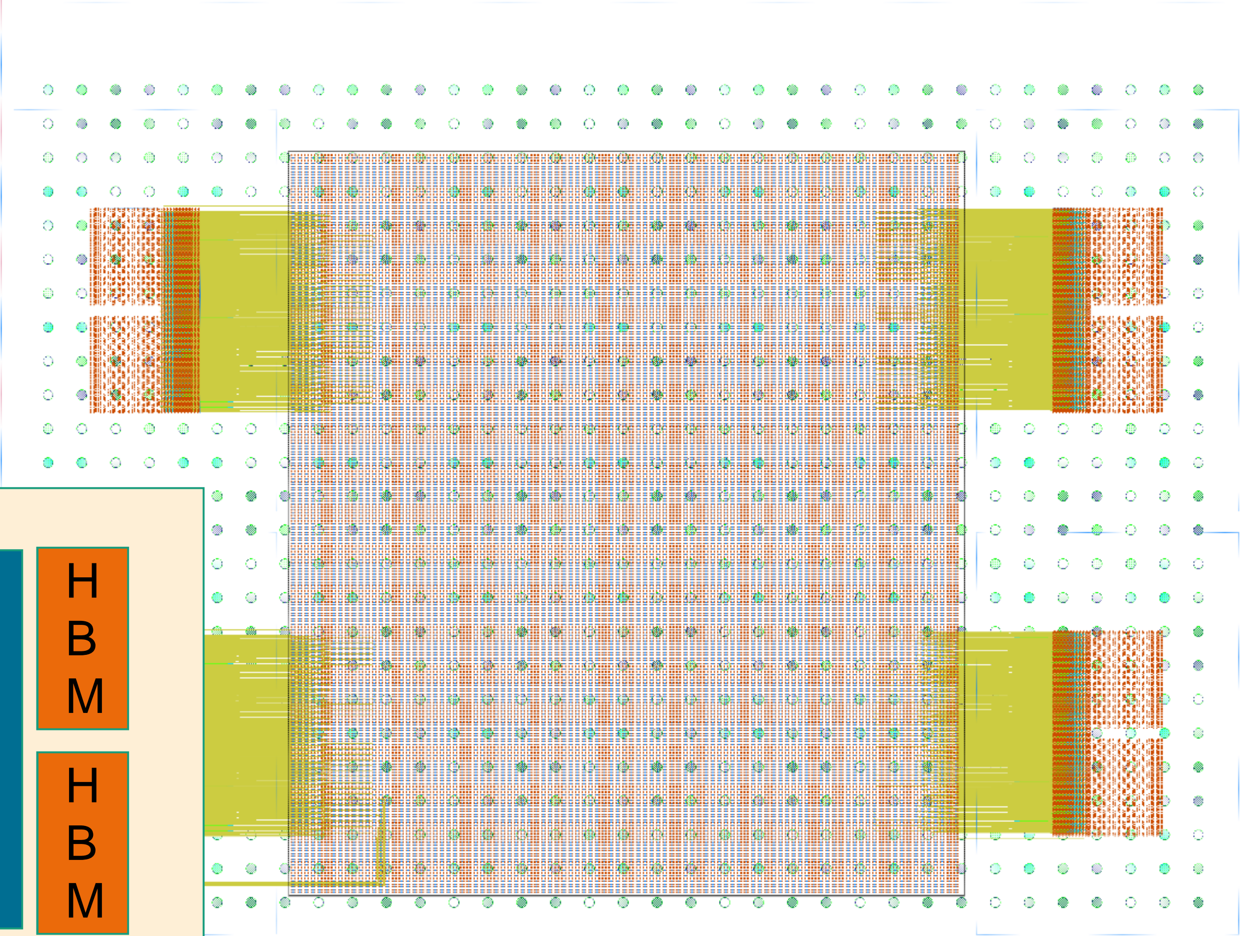
System Description HBM System
Interposer

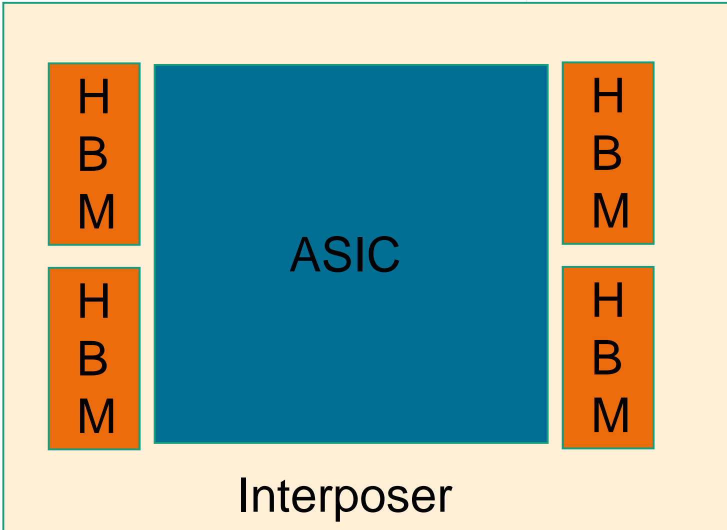
- Technical demonstrator
  - Interposer Routing
  - Speed performance Interposer
- Components
  - ASIC
  - 4x HBM
  - Additional passive are possible
- Interposer Data
  - 37x28 mm
  - 3 metal layers top
  - 1 metal layer bottom (landing for bumps)



System Description HBM System
Interposer

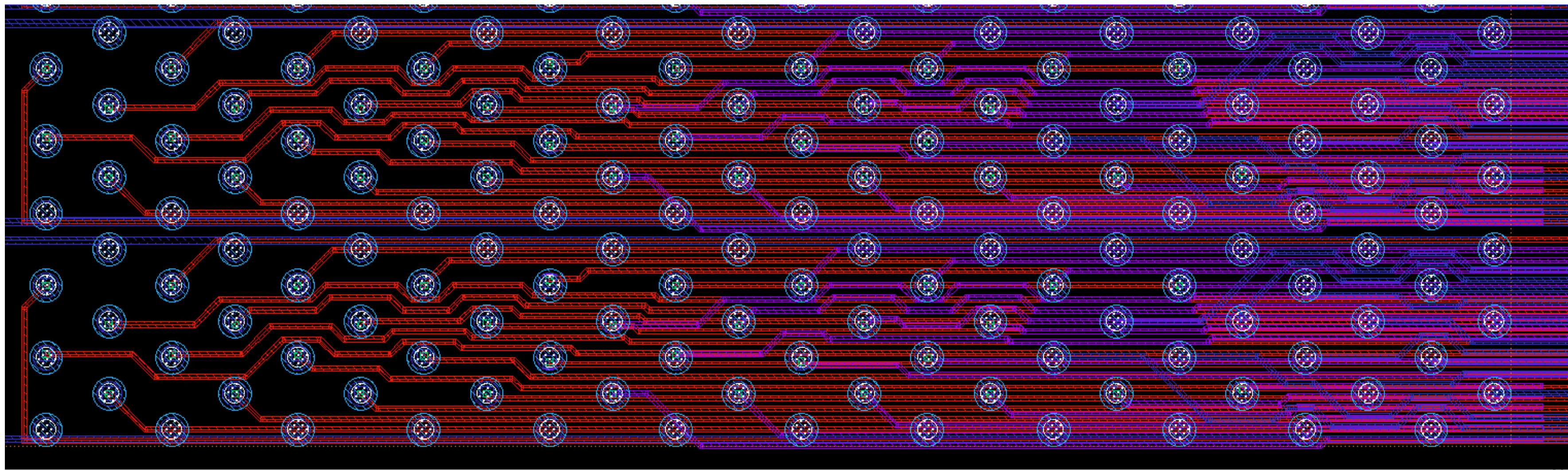
- High Bandwidt





System Description HBM System
Interposer Routing

- HBM Fanout Routing
  - Using 3 layers (W/S 4um)
  - One active area between P/G lines includes 48 balls
  - 13 top layer (same as HBM Bump Landing), 17 second layer, 19 on third layer; space for P&G connection between HBM and ASIC



Summary and Outlook

- Concept for 200GSample/s data rate by 6 bits resolution ADC 1Tbit/s
- Concept for dedicated communication ASIC between the ADC and FPGAs
- Communication between the ADC and the communication chip uses interfaces with slower data rate – reduced design cost, reduced area
- Communication between communication chip and FPGAs with standardized SERDES without calibration
- System with two communications ASICs on silicon interposer and two FPGAs on PCB
  - currently in production; testing to start after summer
- HBM Gen2
  - System with four HBM Dies and an ASIC
  - Design phase finished; production to start