Press Release

IMMEDIATE RELEASE

French Research Teams Demonstrate Hybrid Nanoelectronic Ising Machine for Combinatorial Optimization

Nature Communications Paper Opens Hardware Path Toward Energy-Efficient Optimization Accelerators, Combining ReRAM Devices

GRENOBLE, France - September 8, 2026 - Researchers from CEA-Leti and Spintec in Grenoble, and from C2N/Université Paris-Saclay, have demonstrated a hybrid nanoelectronic Ising machine that combines memristors implemented as hafnium-oxide resistive random-access memory (ReRAM) devices with stochastic magnetic tunnel junctions (SMTJs) to solve hard combinatorial optimization problems.

Reported in *Nature Communications*, the article, "Intrinsic Annealing in a Hybrid Memristor-Magnetic Tunnel Junction Ising Machine," introduces an intrinsic annealing mechanism that could pave the way for more compact, faster, and energy-efficient hardware accelerators. *(Note: Paper title kept as published.)*

Ising machines are specialized hardware accelerators designed to search for optimal solutions among vast numbers of possibilities. They operate by repeatedly updating binary variables until the system reaches a low-energy configuration that achieves a good compromise between the problem constraints.

Compared with conventional implementations of local-search optimization, the research team's architecture aims to reduce data movement and explicit digital-instruction overhead by implementing key operations with the physical properties of nanodevices.

"Optimization is a bit like guiding a marble toward a target pocket on a tilted maze board," said Louis Hutin, co-principal investigator of the project and senior scientist at CEA-Leti. "The tilt drives the marble downhill but downhill can sometimes lead to a dead end. A small shake gives it enough energy to escape and explore another route. In our system, that shake is provided by the natural fluctuations of magnetic tunnel junctions, and its strength can be controlled through their coupling with the memristor network."

Solving Hard Optimization Tasks

The research addresses combinatorial optimization—a critical computational task involving finding the best choice among countless combinations of possibilities. Efficiency gains in this area can translate into saved time, energy, and resources across industries. Relevant application domains include:

- Logistics and transport routing,
- Power-grid management,
- Industrial scheduling and chip design, and
- Hardware acceleration for scheduling and resource-allocation tasks in computing systems.

In this project, the machine implemented key operations of a local-search algorithm using dedicated hardware primitives, reducing the amount of data movement and the number of explicit digital instructions required to execute the algorithm.

The two first authors of the paper, Mohammed Akib Iftakher, a doctoral researcher at CNRS, C2N & Université Paris Saclay, and Hugo Levices, doctoral researcher at CEA-Leti, explained: "The challenge was to make two very different device technologies work together in a controlled computing loop. ReRAM devices store the problem structure, while stochastic magnetic tunnel junctions provide the

variables that fluctuate and update. Showing that this hybrid system can solve concrete graph-optimization benchmarks is an important step beyond isolated device demonstrations." *(Note: Adjusted technical term within quote to match PR terminology. Confirm with authors that this is acceptable.)*

The project also demonstrated that hybrid nanotechnologies can be combined into a working optimization accelerator, rather than treated as separate building blocks. Because ReRAM devices, magnetic tunnel junctions, and CMOS circuitry are compatible with advanced integration, the work points toward compact, fast, and energy-efficient hardware for local-search optimization.

Controlling Randomness with a Single Voltage

A primary challenge in optimization hardware is controlling "stochasticity"—the random fluctuations needed to explore possible solutions. Early stages require high randomness to avoid getting stuck in local minima, while later stages require stability to converge on a solution.

The team demonstrated a system in which the two nanotechnologies work together naturally. ReRAM devices store the problem graph–the links describing how variables influence each other–while SMTJs act as probabilistic yes/no variables that fluctuate due to thermal noise. Because these two elements are closely coupled, adjusting the read voltage of the ReRAM devices array progressively reduces randomness during the search, providing intrinsic annealing with minimal additional circuitry.

This close coupling provides a natural pathway for annealing without needing a separate, heavy control layer for every update step. While the current prototype utilizes external feedback for measurement, the underlying architecture points toward a fully integrated version that minimizes data movement and digital instruction overhead.

Prototype Results and Path to Parallelism

The prototype was tested on concrete graph-optimization benchmarks, consistently finding the global optimum for a 24-vertex weighted MAX-CUT problem and a 10-vertex, three-color graph-coloring problem. All measurements were performed at room temperature and zero magnetic field.

While the current device operates with sequential updates, the authors highlight significant potential for speed improvements in a fully integrated version. By exploiting massive parallelism, utilizing nanosecond-scale switching speeds, and enabling direct coupling between the crossbar and spins—eliminating analog-to-digital conversion delays—the approach could eventually be orders of magnitude faster than current electronic Ising machines.

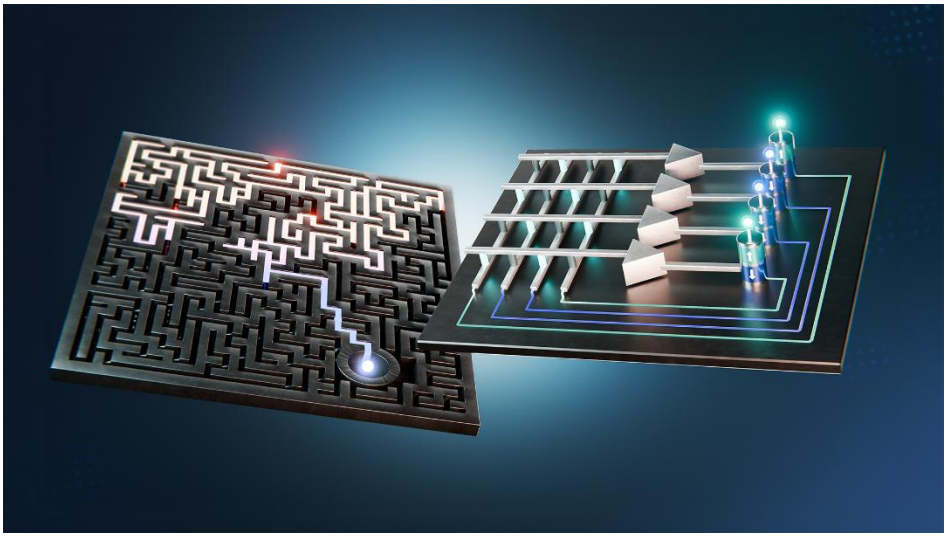
Integration and Scaling

This work bridges two complementary nanotechnologies—ReRAM for dense storage and SMTJs for thermally driven randomness—into a single computing architecture. Both components are CMOS-compatible and integrated in back-end-of-line (BEOL) layers, supporting the vertical 3D integration trends essential for scaling.

"The main point is not just that we put two nanotechnologies together," said Damien Querlioz, co-principal investigator of the project and research director at CNRS. "It is that they can interact directly and help guide the search, without forcing the machine to translate every update back and forth through digital electronics."

Next Steps

The team plans to move from proof-of-concept experiments to more scalable systems. Priority steps include integrating control electronics closer to the devices—ideally on the same chip or in 3D stacks—testing larger problem sizes, and exploiting true parallel operation. Future work will focus on benchmarking speed and energy consumption against conventional computing approaches to quantify performance gains.



Artist's view of intrinsic annealing in a hybrid ReRAM-SMTJ Ising machine. The maze on the left illustrates a search process in which fluctuations first help explore possible solutions. As the signal from the ReRAM array progressively dominates this randomness, the system settles into a stable configuration representing a good solution. The circuit schematic on the right evokes the hardware loop linking the ReRAM crossbar to stochastic magnetic tunnel junctions.
Credit: A.Faure/A.Lhomé/CEA

About the Institutions

CEA-Leti (Grenoble) is a technology research institute at CEA and a global leader in miniaturization technologies. **Spintec** (Grenoble) is a joint research unit of CEA, CNRS and Université Grenoble Alpes specializing in spintronics. **C2N** (Centre for Nanoscience and Nanotechnology, Palaiseau) is a joint CNRS / Université Paris-Saclay laboratory focused on nanoscience, photonics, and nanoelectronics.

About CEA-Leti (France)

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 2,000 talents, a portfolio of 3,200 patents, 14,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble (France) and has offices in San Francisco (United States), Brussels (Belgium), Tokyo (Japan), Seoul (South Korea) and Taipei (Taiwan). CEA-Leti has launched 80 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

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