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International Reliability Physics Symposium

CEA-Leti to Showcase Integrated Expertise In Microelectronics Reliability at IRPS 2026

Seven Papers Present Early-Stage Insights to Guide Technology Developers And Circuit Designers Toward Robust, Industrial-Grade Solutions

GRENOBLE, France — March 17, 2026 — At IRPS 2026, the premier forum for new and original research in microelectronics reliability, CEA-Leti will present seven papers that reflect a broad and integrated expertise across device physics, process integration, RF technologies, FD-SOI, GaN, BEOL reliability, and low-temperature platforms enabling 3D sequential integration. Institute research engineers also contributed to two other projects whose work will be presented.

The papers demonstrate the institute's ability to combine innovative characterization methods with physics-based modelling, delivering early-stage reliability insights that guide both technology developers and circuit designers toward robust, industrial-grade solutions.

"These presentations reflect CEA-Leti's depth in microelectronic reliability—from low-temperature integration and advanced materials analysis to physics-based modeling and design-level mitigation," said Olivier Faynot, director of CEA-Leti's Silicon Components Department and IEEE Fellow. "By deepening understanding of key degradation mechanisms and circuit-level constraints, our teams provide practical insight that accelerates the industrial readiness of GaN, FD-SOI, and 3D sequential technologies."

Presentations

Radio Frequency (Alexis Divay from CEA-Leti will chair the RF/mmW/5G session)

> **"*RF Aging Extensive Characterization & Modeling for Reliability-Aware Power Amplifier Design*"**
> Thursday, March 26, 1:35-2:00 PM
> Authors: Tarek Daher, Alexis Divay in collaboration with STMicroelectronics
> A novel methodology directly measures hot-carrier-induced (HCI) lifetime of standalone SOI power amplifiers under realistic RF stress, covering varied bias conditions and load-impedance mismatches. Empirical time-to-failure contour maps are generated, giving designers immediate visibility into performance-reliability trade-offs during early PA design for emerging mmWave 5G and beyond-5G applications.

> ***"Thermal Robustness of a CMOS-Compatible GaN-on-Si MIS-HEMT Technology"***
> Thursday, March 26, 3:25-3:50 PM
> Author: Luca Nyssens
> 1,400 h, up-to-375 °C unbiased storage tests on 0.15 µm SiN/InAlN/GaN MIS-HEMTs (CMOS-compatible) show only modest Vth shift (≈-200 mV), ~20 % contact-resistance rise, and small drops in Id and gm. Microscopy confirms no side-wall interdiffusion thanks to a refractory alloy gate. The devices remain electrically stable at extreme temperatures, proving GaN power blocks can be monolithically integrated on silicon for high-temperature automotive or aerospace electronics.

3D Sequential Integration & Low Temperature Technologies

> ***"Reaching the BTI 10-Year Lifetime for 2.5 V BEOL-Compatible (< 420 °C) High-Voltage Si-CMOS"***

Tuesday, March 24, 3:40-4:05 PM
Author: William Vandendaele
Using a Si-poly gate, UV-nanosecond laser anneal, and high-pressure passivation, 2.5 V BEOL-compatible transistors achieve the 10-year BTI target despite the low-temperature budget. TiN gates fail due to oxygen scavenging. Designers now have a proven low-temp flow for >2.5-rated CMOS that can be stacked in 3D sequential processes without exceeding 420 °C.

"Influence of Channel Doping on HCI Degradation in Analog SOI nMOSFETs"
Tuesday, March 24, 4:30-4:55 PM
Author: Abygaël Viey
TCAD simulations and experimental validation show that lower channel doping expands the impact-ionization region, increasing hot-carrier generation and interface-trap formation in nitrided SiO_2-gate SOI nMOSFETs. Incorporating the channel implantation dose into the Takeda model accurately predicts the observed rise in time-to-failure, providing a clear path for analog designers to mitigate HCI by tailoring doping profiles.

"Improving Electromigration Lifetime Through Power-Grid Segmentation: An Experimental Study"
Thursday, March 26, 2:00-2:25 PM
Authors: Robert Bloom (University of Minnesota) with contribution from Stéphane Moreau (CEA-Leti)
Silicon-level EM tests on segmented power-grid structures exploit the Blech effect: shorter segments reduce stress-migration-driven void formation, yielding markedly longer time-to-failure and smaller IR-drop shifts. Segmenting BEOL power grids becomes a practical, layout-level knob to boost EM robustness in advanced nodes carrying high currents.

"Ground-Plane Effect on Random Telegraph Noise in Mesa-Isolated SOI MOSFETs for 3D Sequential CISi"
Tuesday, March 24, 11:20-11:45 PM
Authors: Ahmed Machmach (STMicroelectronics) with contribution from Joris Lacord and Fabienne Ponthenier (CEA-Leti)
Increasing the substrate (ground-plane) bias reshapes the channel's electric field, pushing more oxide-trap events above the detection threshold and amplifying their current spikes. This controllable RTN boost helps designers predict and mitigate noise in 3-D sequential CMOS image sensors.

"Dit-Nt Correlation in pBTI Stressed SOI nMOSFET via Low Frequency Noise Measurements"
Tuesday, March 24, 2:00-2:25 PM
Author: Antoine Albouy
Low-frequency-noise measurements show that as pBTI stress progresses, oxide-trap density (Nt) rises in lockstep with interface-trap density (Dit). The tight correlation indicates that interface quality dominates stress-induced noise, emphasizing the need for robust interface engineering in future FD-SOI devices.

FD-SOI

"Spacer Trapping Effect on Hot-Carrier Degradation Dynamics for Advanced FD-SOI Nodes"
Wednesday, March 25, 2:00-2:25 PM
Author: Tadeu Mota Frutuoso
Comparing high- vs. low-trapping SiCO spacers reveals that trapped charge in spacers dominates early HCI wear but saturates quickly; low-trapping spacers completely suppress this early degradation. Spacer material selection is a decisive lever for extending device lifetime in forthcoming GAA and CFET platforms.

"Modeling the Impact of HK Thickness Scaling (Down to 1.1 nm) on Gate Leakage and PBTI in Advanced FD-SOI Devices"
Tuesday, March 24, 4:05-4:30 PM
Author: Elhadji Alhousseyni Diallo
Using direct-tunnelling physics and Comphy simulations, this study quantifies how ultra-thin high-k (HK) layers affect gate leakage and positive-bias-temperature-instability (PBTI). A higher tunnel mass in sub-2 nm oxides indicates a microstructural shift, while reduced HK thickness simultaneously lowers leakage and improves PBTI endurance. The results provide a calibrated model that designers can employ when pushing HK scaling for next-generation FD-SOI technologies.

About CEA-Leti (France)

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 2,000 talents, a portfolio of 3,200 patents, 14,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble (France) and has offices in San Francisco (United States), Brussels (Belgium), Tokyo (Japan), Seoul (South Korea) and Taipei (Taiwan). CEA-Leti has launched 80 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

Technological expertise

CEA has a key role in transferring scientific knowledge and innovation from research to industry. This high-level technological research is carried out in particular in electronic and integrated systems, from microscale to nanoscale. It has a wide range of industrial applications in the fields of transport, health, safety and telecommunications, contributing to the creation of high-quality and competitive products.

For more information: www.cea.fr/english

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