

Electronic Components and Technology Conference

CEA-Leti Will Present Its Latest Advances On Next-Generation Chip Integration at ECTC 2026

*Focus of Seven Papers and Posters Includes Hybrid Bonding
And Low-Temperature Processing*

GRENOBLE, France – April 28, 2026 – CEA-Leti will present seven papers and posters on technologies shaping the next decade of advanced heterogeneous integration at the Electronic Components and Technology Conference (ECTC) May 26-29 in Orlando, Fla.

These developments cover a variety of technologies, including reducing interconnect pitches through hybrid bonding interconnection, for low-temperature processes, superconducting interconnects and fan-out wafer-level packaging.

Hybrid bonding, which is based on direct copper-to-copper and dielectric-to-dielectric connection technology, enables ultra-fine pitch vertical interconnects. It is emerging as the primary path for high-density 3D integration, as micro-bump approaches reach their scaling limits.

For example, in the paper “**Die-To-Wafer Hybrid Bonding Technology down to 1 μm pitch for Multi-Die Stacking Integration**” CEA-Leti will present its first demonstration of a die-to-wafer hybrid bonding test vehicle with a pitch as small as 1 μm .

Low-temperature processing enables heterogeneous integration in which temperature-sensitive materials (polymers, certain semiconductors) must coexist with standard CMOS processes. The ability to form robust interconnects below typical thermal budgets opens pathways for stacking previously incompatible technologies. The first time successful direct hybrid bonding annealed at ultra-low temperatures down to 100 °C will be presented.

As transistor gate-scaling slows, system-level integration through advanced packaging delivers the performance, power, and form-factor improvements that end-users expect. CEA-Leti’s research on hybrid bonding that will be presented at ECTC 2026 reflects growing industry alignment around hybrid bonding as a key enabler of next-generation, high-performance packaging.

Specialized Applications

Beyond foundational process development, CEA-Leti researchers will also present application-specific integration advances:

- **Quantum Systems:** The superconducting 3D interconnect work signals packaging infrastructure development for quantum computing, where thermal resistance and electromagnetic isolation are significant constraints.
- **RF/Wireless:** The RADAR system-in-package with integrated antennas demonstrates continued innovation in fan-out wafer-level packaging for millimeter-wave applications, critical for 5G/6G and automotive radar.

Papers & Posters

- “**Hybrid Bonding with Ultra-Low Temperature Annealing: Morphological and Electrical Validations**”
Author: Margot Faure
Session 3
Wednesday, May 27 from 9:30 AM – 9:50 AM

- **“Enabling Low-Temperature Fine-Pitch Hybrid Bonding: Role of Nanocrystalline Copper Microstructures and Pre-Bond Surface Treatments”**
Session 3
Author: Mathieu Loyer (in collaboration with STMicroelectronics)
Wednesday, May 27 from 11:35 AM – 11:55 AM
- **“RADAR System-in-Package with Integrated Antennas based on Fan-Out Wafer-Level Packaging RDL-First”**
Session 39 (Poster)
Author: Arnaud Garnier, presented by Jean Charles Souriau
Wednesday, May 27 from 2:30 PM – 4:30 PM
- **“Electroplated Indium Micro-Bumps: Toward Scalable Low Temperature Ultra-Fine Pitch Interconnects”**
Session 40
Author: Maria-Luisa Calvo-Munoz
Wednesday, May 27 from 4:45 PM – 5:05 PM
- **“Impact of Copper Density on Via-to-Via Hybrid Bonding: Morphological and Electrical Characterizations”**
Session 39 (Poster)
Author: Agathe Lerat
Thursday, May 28 from 10:00 AM – 12:00 PM
- **“Fine-Pitch Thermally Resistive Superconducting 3D Interconnects for Quantum Systems”**
Session 39, (Poster)
Author: Pablo Renaud
Thursday, May 28 from 10:00 AM – 12:00 PM
- **“Die-To-Wafer Hybrid Bonding Technology down to 1 μm pitch for Multi-Die Stacking Integration”**
Session 31
Author: Melissa Najem
Friday, May 29 from 2:00 PM – 2:20 PM

About CEA-Leti (France)

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro- & nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 2,000 talents, a portfolio of 3,200 patents, 14,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble (France) and has offices in San Francisco (United States), Brussels (Belgium), Tokyo (Japan), Seoul (South Korea) and Taipei (Taiwan). CEA-Leti has launched 80 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

Technological expertise

CEA has a key role in transferring scientific knowledge and innovation from research to industry. This high-level technological research is carried out in particular in electronic and integrated systems, from microscale to nanoscale. It has a wide range of industrial applications in the fields of transport, health, safety and telecommunications, contributing to the creation of high-quality and competitive products. For more information: www.cea.fr/english

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