Press Release

IMMEDIATE RELEASE

CEA-Leti Presents Die-to-Wafer Hybrid Bonding At 1 µm Pitch, Removing Bottleneck for AI Hardware

ECTC 2026 Paper Reports Breakthrough in 3D Integration for High-Performance Computing, Advanced Smart Vision and Artificial Intelligence

ORLANDO, Fla. – May 29, 2026 – CEA-Leti today announced a major milestone in the evolution of 3D integration for high-performance computing (HPC), advanced smart-vision systems and artificial intelligence (AI), demonstrating a functional test vehicle utilizing die-to-wafer (D2W) hybrid bonding with pitches down to 1 µm. The findings were presented at the Electronic Components and Technology Conference (ECTC) 2026.

As Moore's Law reaches physical limits, the semiconductor industry is increasingly relying on 3D stacking to enhance performance and energy efficiency. This D2W technology addresses a critical bottleneck in AI accelerator design: interconnect density and bandwidth. By vertically stacking device layers with ultra-fine pitches, the technology shortens interconnect paths, significantly increasing data transfer speeds while reducing power consumption.

"This successful electrical testing of structures with up to 100,000 links confirms the viability of this technology for high-density interconnects," said Melissa Najem, CEA-Leti research engineer and lead author of the paper, ***"Die-to-Wafer Hybrid Bonding Technology Down to 1 µm Pitch for Multi-Die Stacking Integration."***

"Combining multi-fine pitch D2W with inter-die gap filling, high-density through-silicon vias, and through-oxide vias paves the route toward multi-die stacking. These developments represent a vital step toward overcoming the physical limitations of current semiconductor scaling, enabling more compact, powerful, and energy-efficient electronic systems," she added. "This 1-µm fine-pitch Cu-Cu interconnect in D2W is a world first, to the best of our knowledge."

Overcoming Alignment and Planarization Challenges

Achieving a 1 µm pitch required the team to engineer very precise alignment accuracy, the primary challenge for the D2W building block. Additionally, the wafer reconstruction process involving inter-die gap filling (IDGF) demanded optimized chemical mechanical planarization (CMP) to ensure compatibility with subsequent vertical interconnects.

Electrical characterization of daisy-chain structures confirmed expected performance and yields for pitches ranging from 5 µm down to 2 µm. While the yield at 1 µm is limited by the alignment accuracy of existing bonding tools, the team anticipates significant improvements with the introduction of next-generation tools featuring 0.5 µm (3σ) alignment capabilities.

Roadmap to 0.5 µm Pitch and Beyond

This demonstration serves as a transitional proof of concept, laying the groundwork for a second-generation test vehicle. The immediate next steps include integrating the D2W technology with vertical interconnections—specifically high density through-silicon vias (HD TSV) and through-oxide vias (TOV)—facilitated by the intermediate inter-die gap filling (IDGF) process step.

"In the future, we will target a D2W hybrid-bonding test vehicle with a pitch of 0.5 µm to further improve interconnect density for advanced AI applications," explained Jean-Charles Souriau, scientific director

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at CEA-Leti. "This advancement aims to cater to the escalating demands of next-generation AI accelerators and CMOS image sensors."

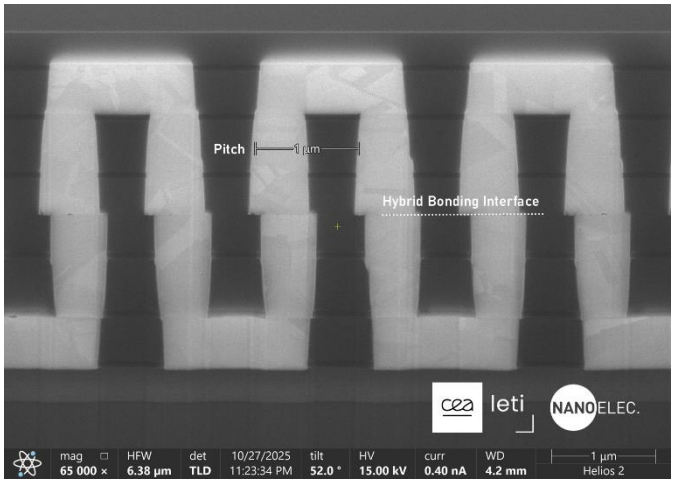
Roadmap to Multi-die Stacking Architectures

The building blocks related to IDGF, TOV and HD TSV will enable the integration of different dies and functions with dense vertical interconnections.

“These technologies enable advanced wafer reconstruction and complex multi-die stacking for innovative architectures. Moreover, the combination of D2W and W2W technologies is of high interest to address both performance and cost requirements for future digital devices and systems,” said Eric Ollier, director of the Smart Imager and Advanced Smart Vision programs at IRT Nanoelec.

The D2W research was carried out within the framework of the FAMES Pilot Line and the ANR NextGen project (France 2030 initiative). Related IDGF, TOV and HD TSV studies were supported by IRT Nanoelec.

A CEA-Leti team has focused for more than 15 years on the key enabling technology of hybrid bonding (W2W and D2W) and HD TSV for the three-layer CMOS image sensors under development at IRT Nanoelec, and it publishes several papers at every ECTC conference. The institute received a highlighted-paper recognition at ECTC 2024 for demonstrating a three-layer test vehicle that featured two embedded Cu-Cu hybrid-bonding interfaces, face-to-face (F2F) and face-to-back (F2B), and one wafer containing HD TSVs.



Cross-section of a 1µm-pitch D2W hybrid-bonded test vehicle
Photo credit: Anthony ZAZA_CEA-Leti

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About CEA-Leti (France)

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti

pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups. CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities. With a staff of more than 2,000 talents, a portfolio of 3,200 patents, 14,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble (France) and has offices in San Francisco (United States), Brussels (Belgium), Tokyo (Japan), Seoul (South Korea) and Taipei (Taiwan). CEA-Leti has launched 80 startups and is a member of the Carnot Institutes network. Follow us on www.leti-cea.com and @CEA_Leti.

Technological expertise

CEA has a key role in transferring scientific knowledge and innovation from research to industry. This high-level technological research is carried out in particular in electronic and integrated systems, from microscale to nanoscale. It has a wide range of industrial applications in the fields of transport, health, safety and telecommunications, contributing to the creation of high-quality and competitive products.

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