SILICON PHOTONIC: PDK AND EDA TOOLS

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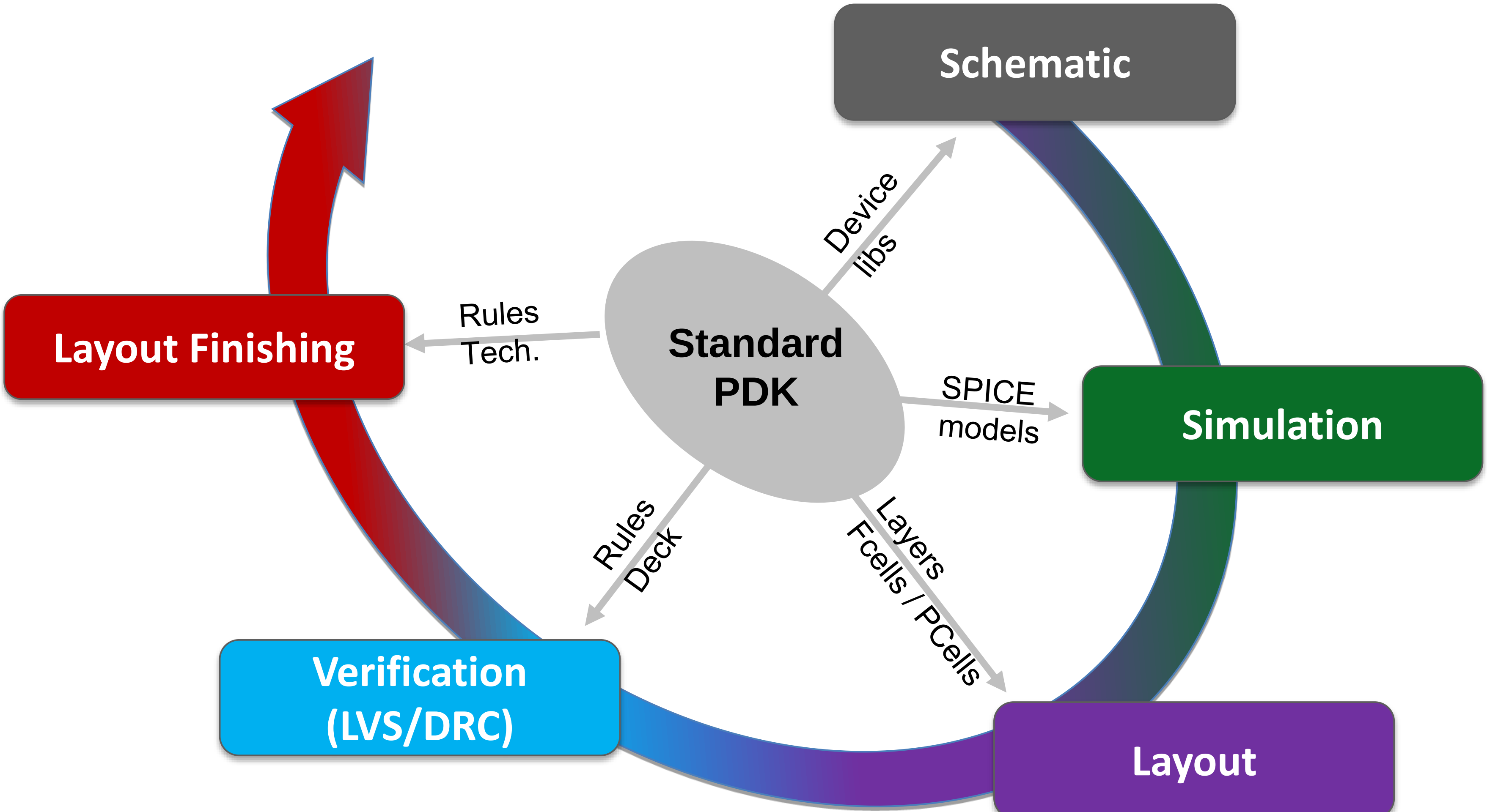
OUTLINE

- PDK environment for Si photonic technologies
- Simulation of photonic integrated circuits
- Silicon photonic device models
- Example of simulations
- Layout of photonic integrated circuits
- Conclusion

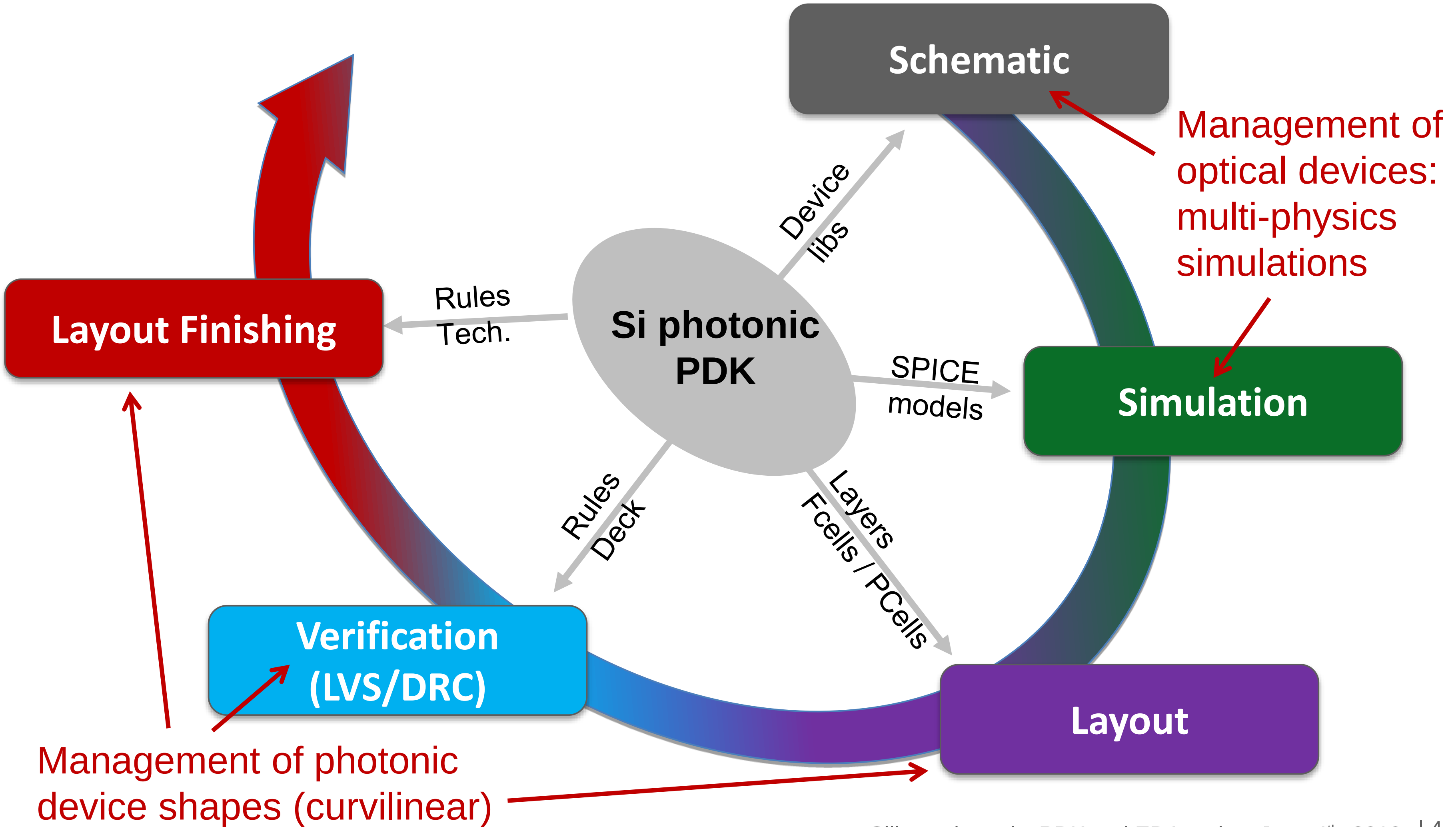
PDK ENVIRONMENT FOR SI PHOTONIC TECHNOLOGIES

- Overview of standard PDK environment



PDK ENVIRONMENT FOR SI PHOTONIC TECHNOLOGIES

- Overview of our photonic design flow (CMOS-like)



PDK ENVIRONMENT FOR SI PHOTONIC TECHNOLOGIES

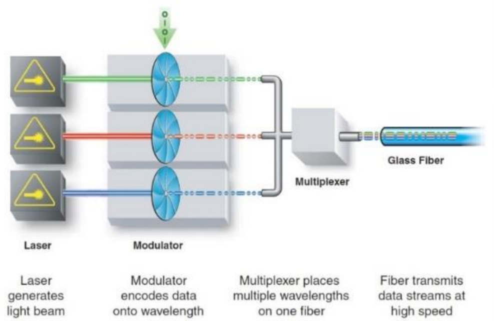
- **EDA tools for Si photonic: various existing CAD tools**

IC design requires multi-physics optimization using dedicated software

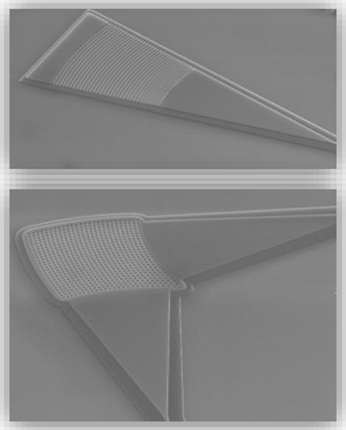
Our approach is an adaptation of standard EDA tools for photonic applications

SIMULATION OF PHOTONIC INTEGRATED CIRCUITS

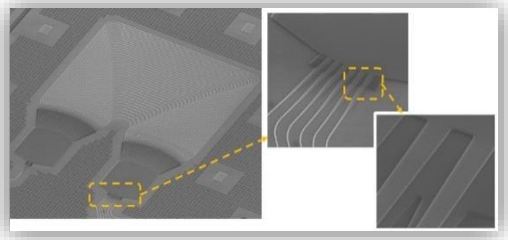
- **Devices in Si photonic circuits**



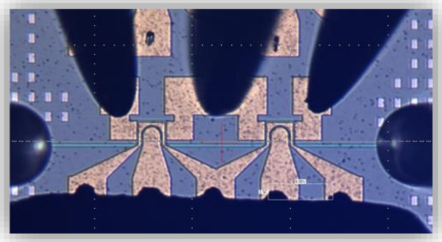
Emitter

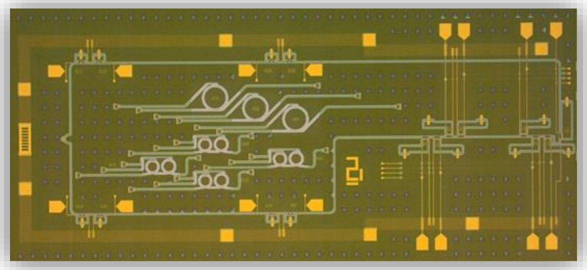


Fiber coupler

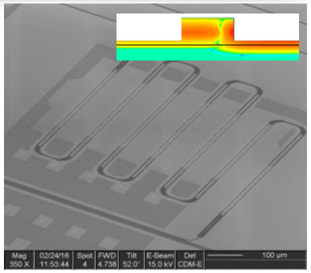


Wavelength multiplexer

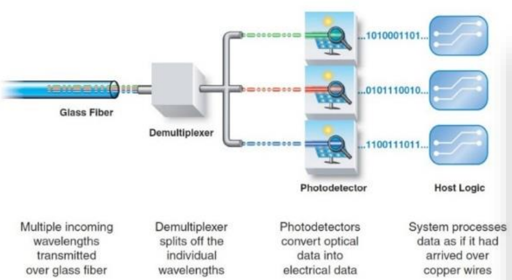




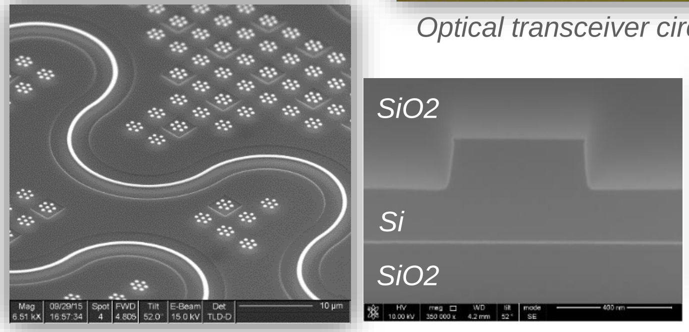
Optical transceiver circuit



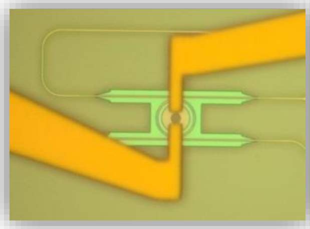
High speed modulator



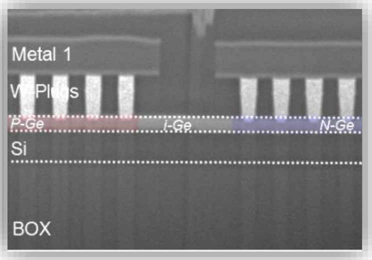
Receiver



Highly confined waveguides



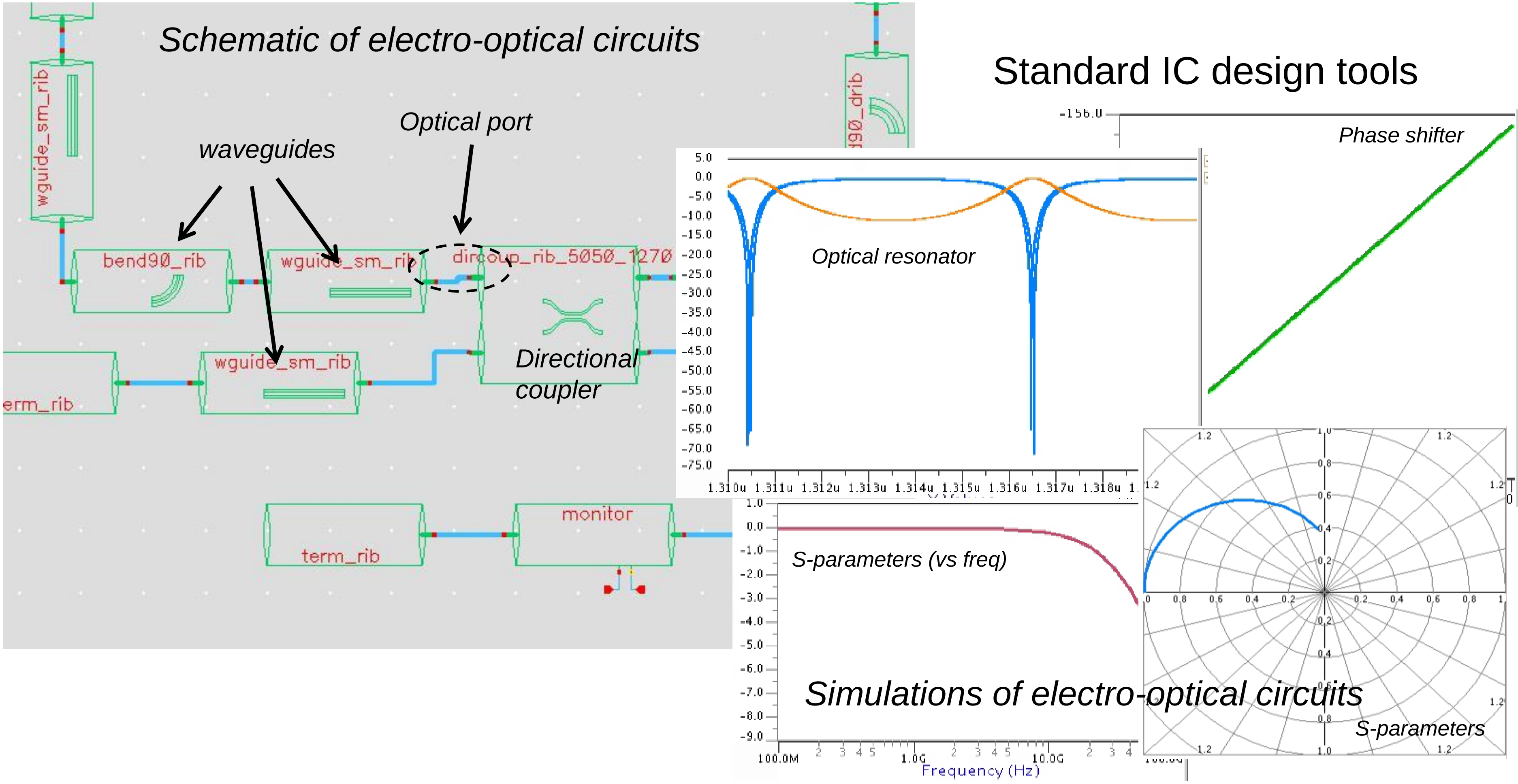
Tunable filter



High speed photodetector

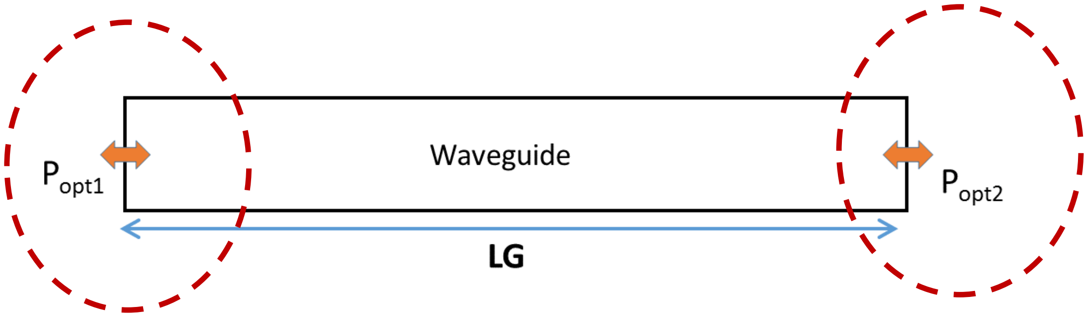
SIMULATION OF PHOTONIC INTEGRATED CIRCUITS

- **Electro-optical co-optimization: schematic to simulation**



SIMULATION OF PHOTONIC INTEGRATED CIRCUITS

- **Introduction to the optical bus: optical fields**



In this case: 2 optical ports device

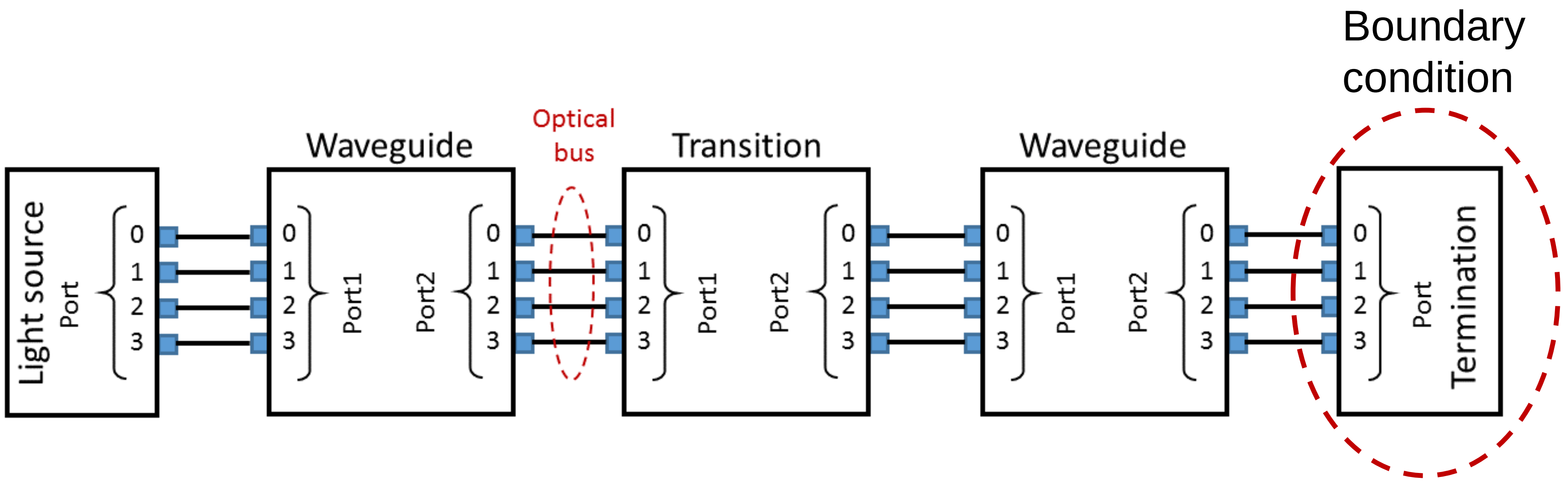
- Each optical port must be bi-directional because the position of the source light is unknown: symmetrical model topology
- Each port must contain information of module and phase of TM and TE fields: 4 analog values
- The wavelength information is managed as instance parameter

SIMULATION OF PHOTONIC INTEGRATED CIRCUITS

- **Introduction to the optical bus: optical fields**

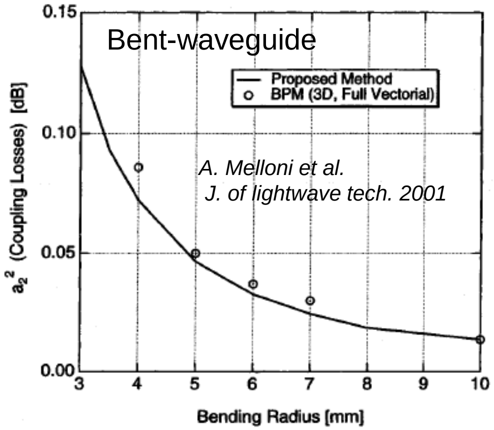
❑ Each optical port consist to a bus of 4 nodes:

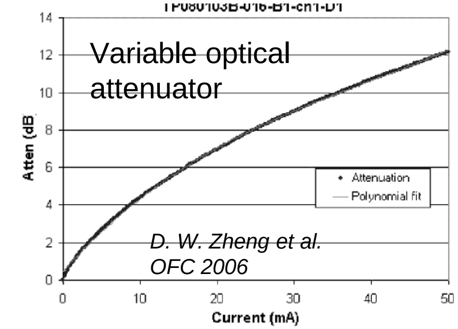
- Real part of the optical TE field
- Imaginary part of the optical TE field
- Real part of the optical TM field
- Imaginary part of the optical TM field

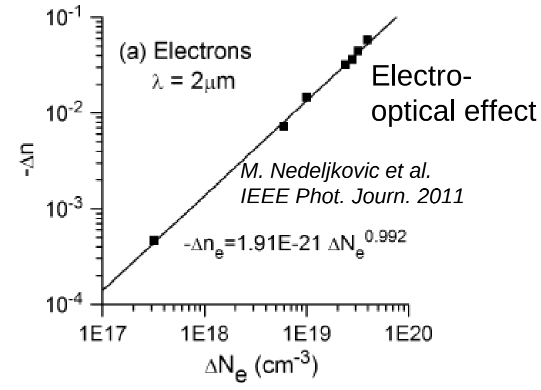


SILICON PHOTONIC DEVICE MODELS

- **SPICE modeling: major physical effects**
  - ❑ Optical effects:
    - ❑ wave propagation (loss, phase shift) : waveguide
    - ❑ coupling effect: directional coupler, micro-ring
    - ❑ split effect: Y-junction, interferometer
  - ❑ Thermo-optical effect: heater to change the group index
  - ❑ Thermo-electrical effect: thermal resistance and capacitance
  - ❑ Electro-optical effect: modulator using junction, photodetector



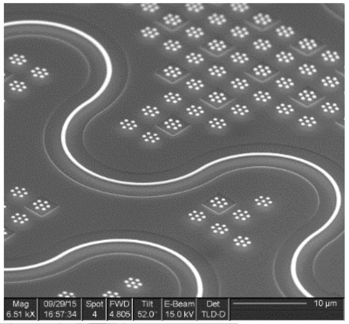


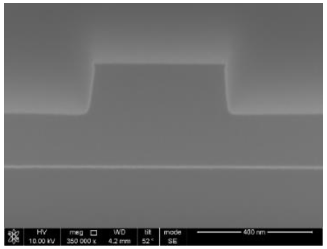


SILICON PHOTONIC DEVICE MODELS

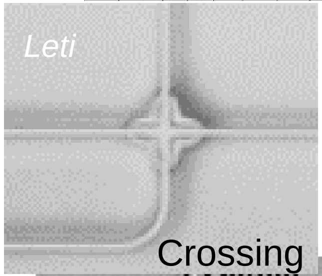
- **Passive devices**

  - Waveguides: straight, bent, S-bent, taper, transition, crossing, etc.
  - Splitters: Y-junctions, multi-mode interferometers, directional couplers
  - Filters: micro-ring resonators
  - Optical IO: grating couplers

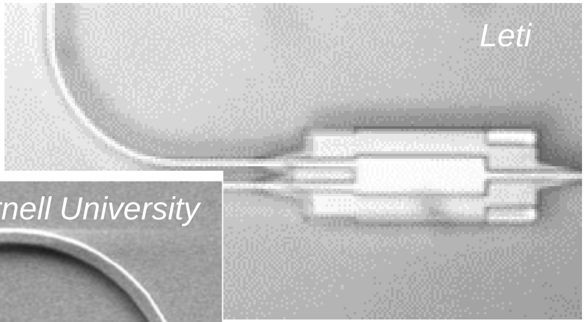




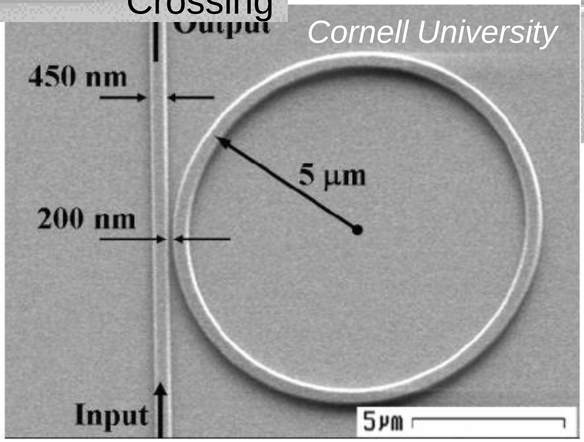
Waveguide



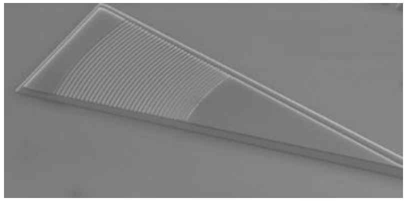
Crossing



MMI



Micro-ring filter



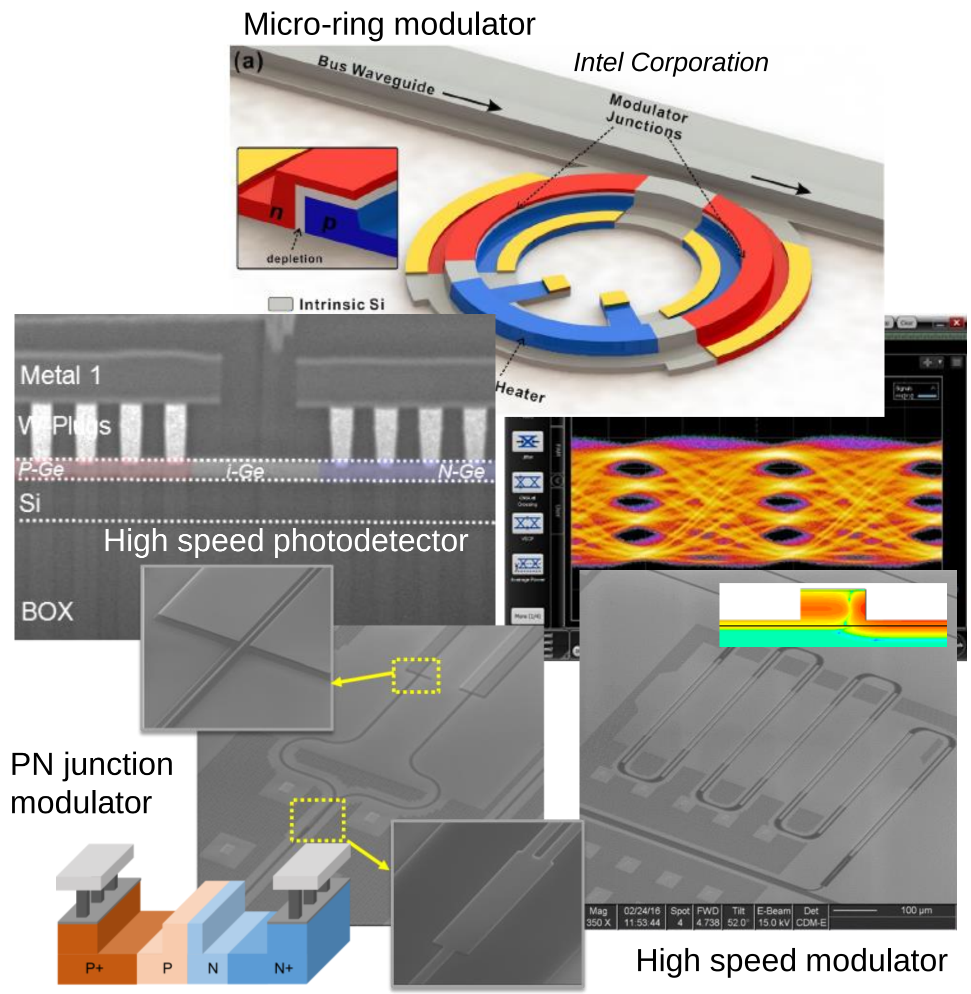
Grating coupler

Passive devices are modeled by considering optical fields only

SILICON PHOTONIC DEVICES MODELS

- **Active devices**

  - Phase-shifter waveguide
  - Modulator: micro-ring, Mach-Zehnder modulator
  - Heater: tunable waveguide
  - Photodetector: Ge junction



Active devices are modeled by considering optical fields and electrical nodes

SILICON PHOTONIC DEVICES MODELS

- **Photonic model suite (PMS) v1.0.0: Verilog-A codes**

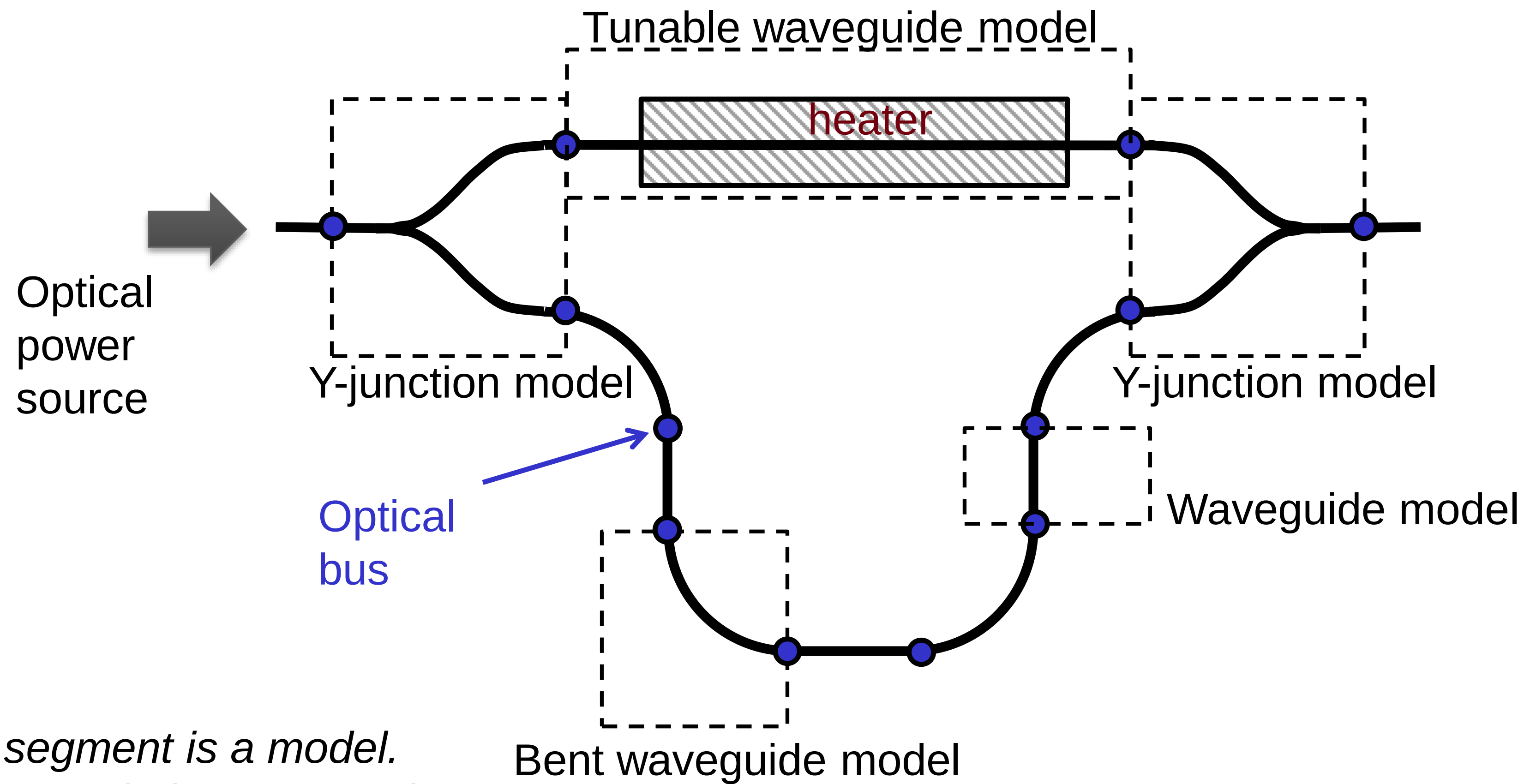
❑ Wide-ranging set of models (22 models at present):

Model type	Device
Waveguides	Straight, bend, S-bend, transition, tapers, crossing, etc.
Splitters	Y-junction, directional coupler, multi-mode interferometers
I/O devices	Grating couplers
Filters	Micro-ring resonator
Active devices	Tunable waveguide, phase shifter, modulators, photodiodes
Tools	Voltage controlled light source, optical power monitoring

❑ All IC simulators with the capability to manage Verilog-A models can use these models

EXAMPLE OF SIMULATIONS

- **Example of basic circuit: Mach-Zehnder interferometer**



Each segment is a model.
This example is composed of 10 photonic devices

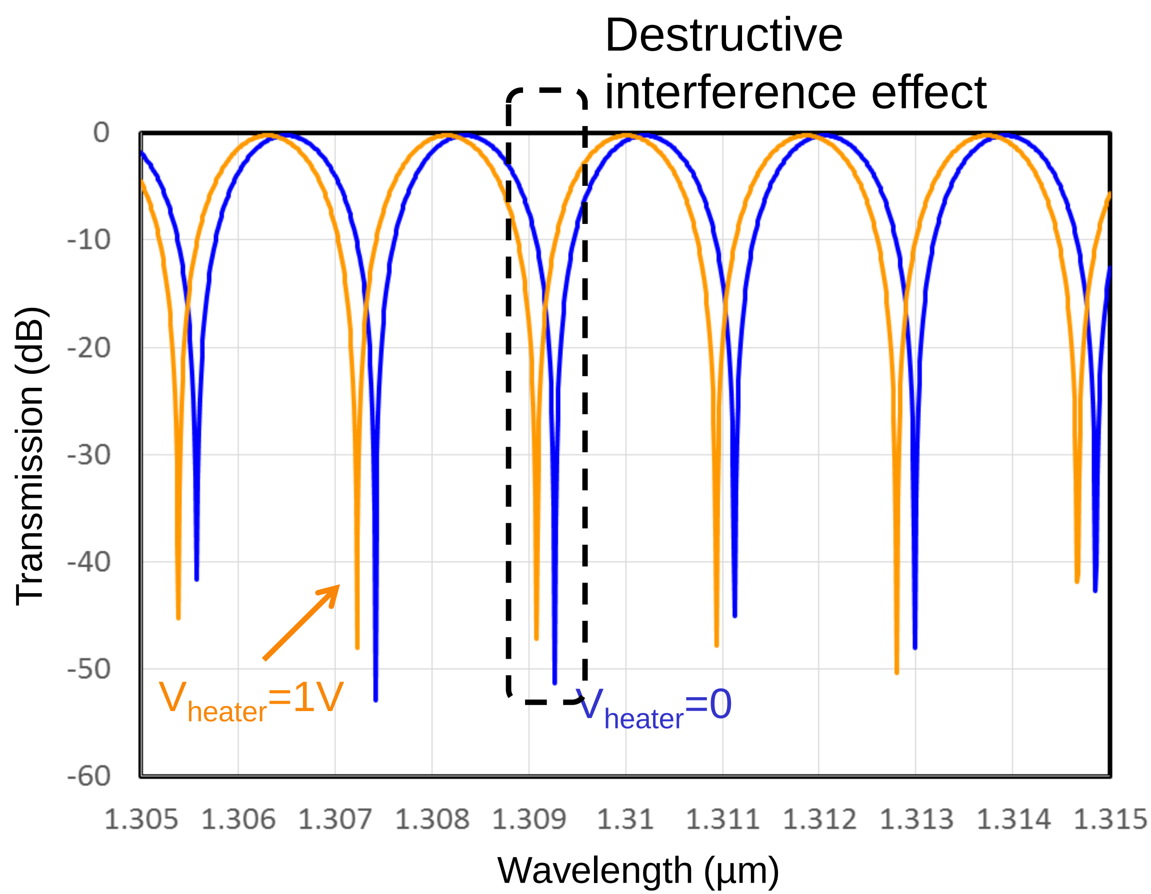
EXAMPLE OF SIMULATIONS

- **Example of basic circuit: Mach-Zehnder interferometer**

Interference effect: due to the length difference of the two optical paths (phase)

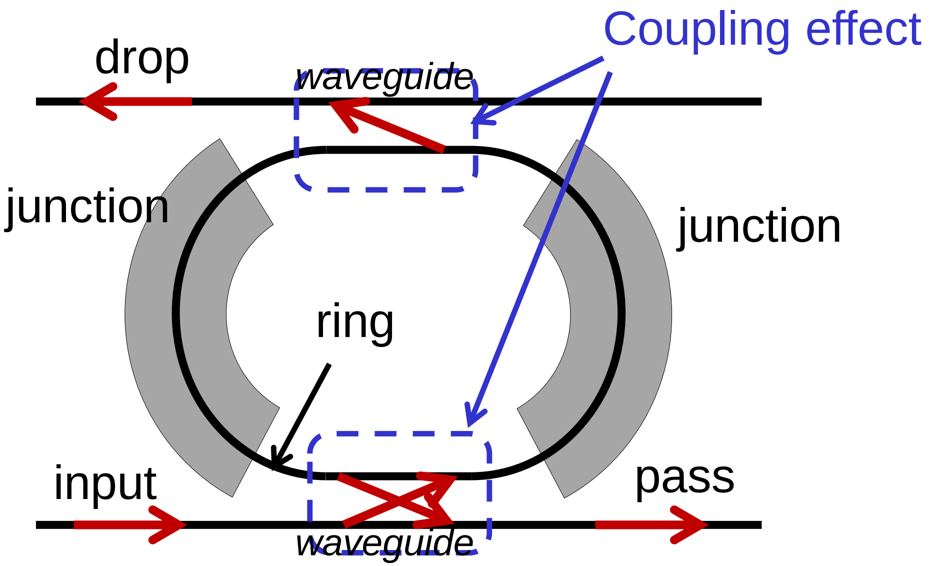
Biasing the heater, temperature increases: induces a phase variation to an optical path

Tunable destructive interference



EXAMPLE OF SIMULATIONS

- **Example of SPICE model: micro-ring modulator**



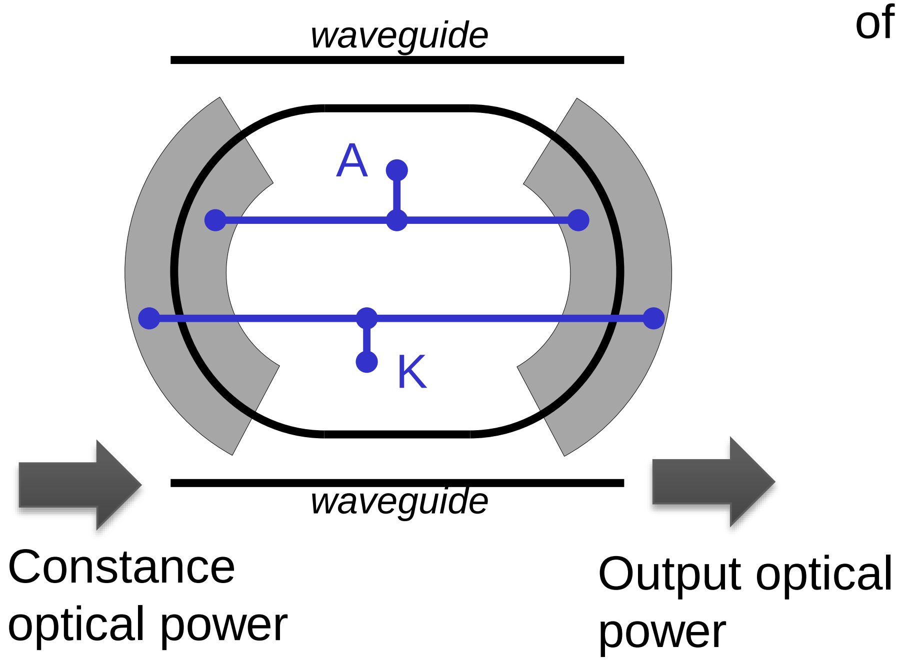
4-ports micro-ring

As example, 2 test cases:

1. Evaluation of the resonant wavelength
2. Simulation of the modulation effect

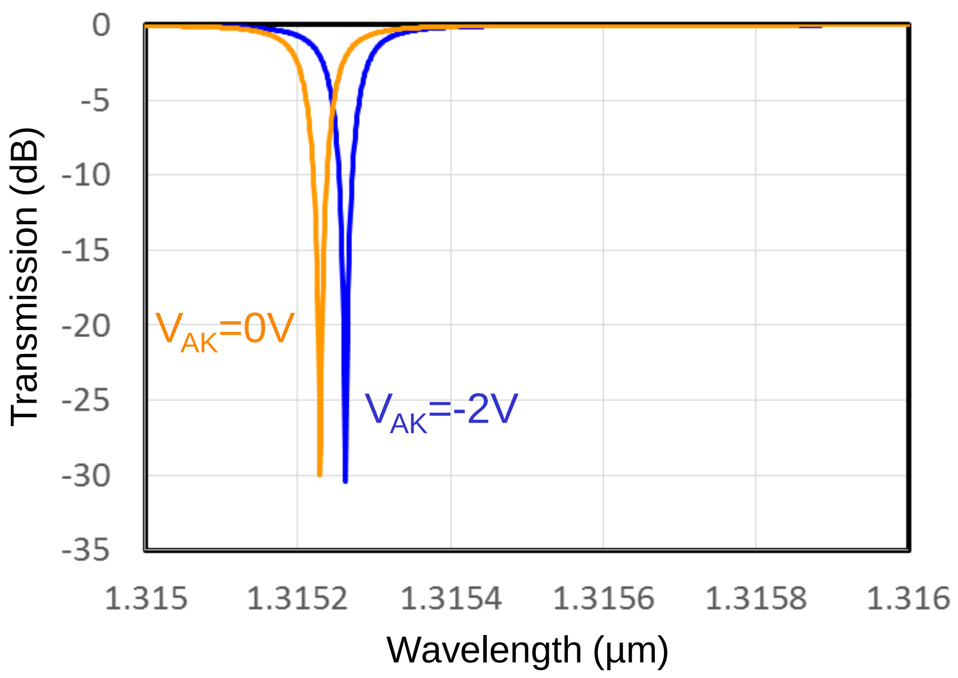
EXAMPLE OF SIMULATIONS

- **Example of SPICE model: resonant wavelength of modulator**



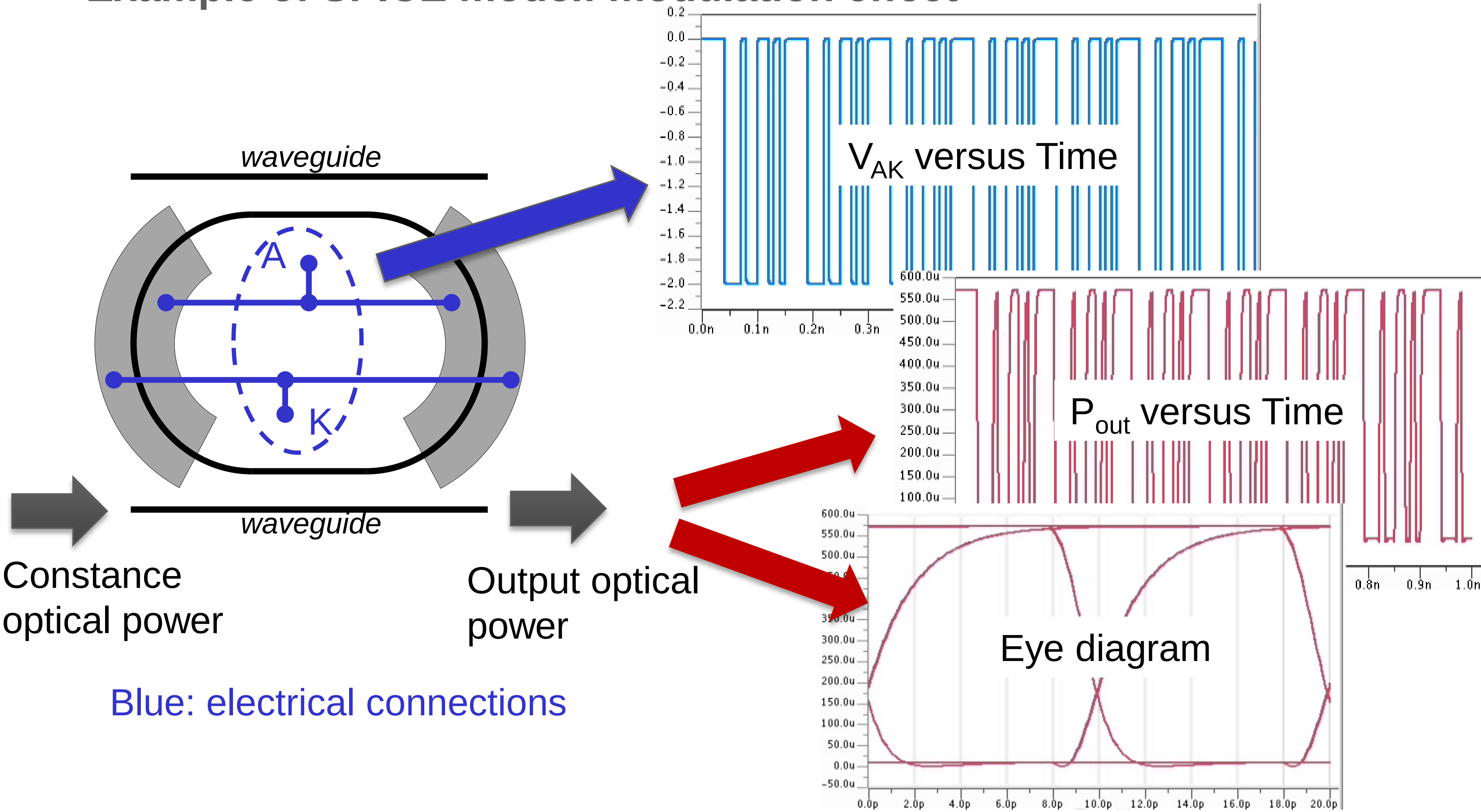
Blue: electrical connections

Test case: DC voltage on junction, sweep of the wavelength



EXAMPLE OF SIMULATIONS

- **Example of SPICE model: modulation effect**

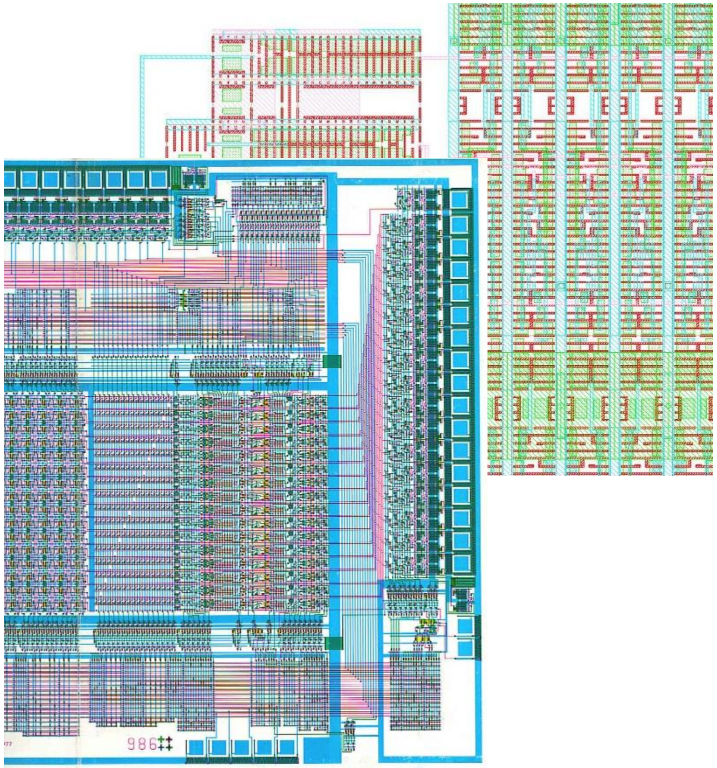


Blue: electrical connections

LAYOUT OF PHOTONIC INTEGRATED CIRCUITS

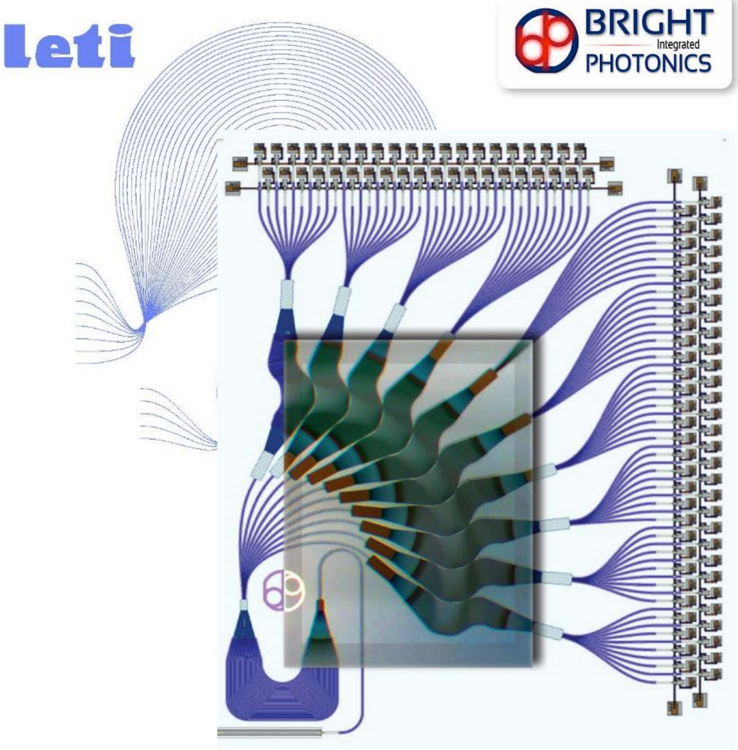
- **CMOS IC design versus Si photonic IC design:**

CMOS IC layout



Orthogonal layout

Si photonic IC layout

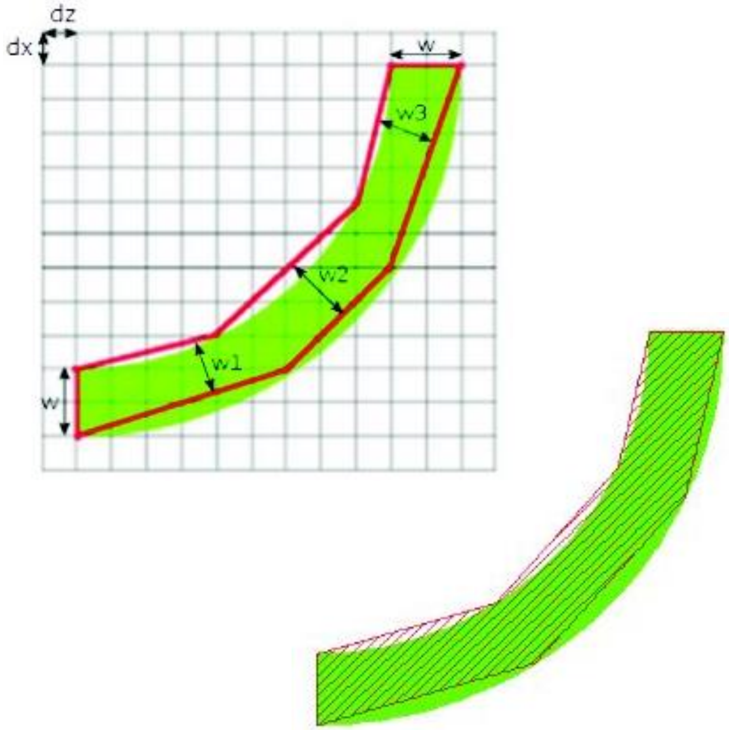


Curvilinear layout

LAYOUT OF PHOTONIC INTEGRATED CIRCUITS

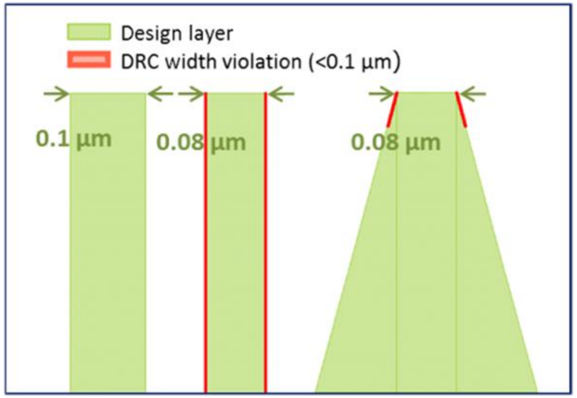
- **Challenges:**

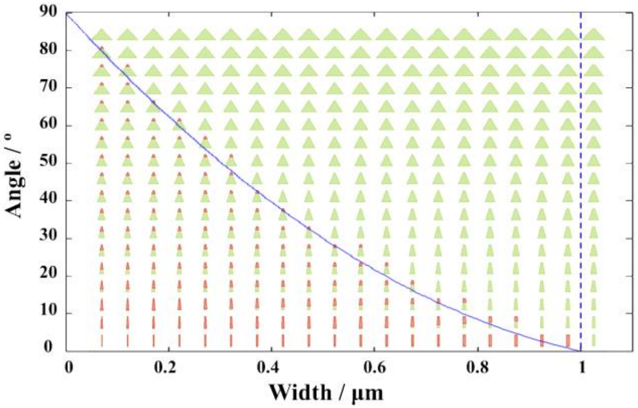
  - ❑ Skew edges are widely used to draw photonic layout component
  - ❑ Layouts of photonic devices require dedicated methods to generate curvilinear and all angle designs
  - ❑ The challenge is to control the discretization of all curvilinear shapes into polygons with the "snapping grid effect" constraint (~nm)



LAYOUT OF PHOTONIC INTEGRATED CIRCUITS

- **Verification tools:**
  - ❑ LVS: the shapes of photonic devices are not compatible with existing tools. LVS requires dedicated markers for each device and extraction methodologies
  - ❑ DRC: it must be adapted due to curvilinear design. Traditional IC DRC tools are incompatible with these geometries. It requires equation-based DRC (eqDRC)





False error filtering with post-processing using additional geometrical information and user-defined criteria such as tolerance

LAYOUT OF PHOTONIC INTEGRATED CIRCUITS

- **Layout finishing: dummies and Cad 2 Mask**

  - ❑ Si photonic process requires to generate dummies
  - ❑ Due to the shape of photonic devices: runtime for dummies generation is a significant issue (complex boundaries)
  - ❑ New approach has been validated to address photonic layout specificities :
    - Post processing of photonic layers before sizing
    - Optimizing settings for hierarchy distribution
    - Tune the parallel processing on multi-CPU

Tiled Photonic layout

CONCLUSION

- The use of standard IC design tools requires several significant developments.
- Schematic and models:
  - new models with their associated symbols for passive (waveguides, splitters, etc) and active (modulator) photonic devices.
  - Several physical effects must be included: wave propagation and phase shift, wave splits, electro-optical effects, temperature effects, heating effects, etc.
- Layout, verification and finishing: curvilinear shapes of photonic devices imply to introduce small grids in layout environment, equation-based DRC, additional layers for LVS.

Thank You

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