A VERSATILE SILICON PHOTONICS PLATFORM WITH ADVANCED COMPONENTS

Silicon Photonics Integration Lab | CEA-Leti

L. Virot

OUTLINE

1. Silicon photonic : 200mm CMOS core technology towards 300mm
2. Emergent needs vs core process
3. Technological add-on #1 : 3D packaging
4. Technological add-on #2 : Silicon Nitride circuits
5. Technological add-on #3 : Hybrid III-V on silicon laser

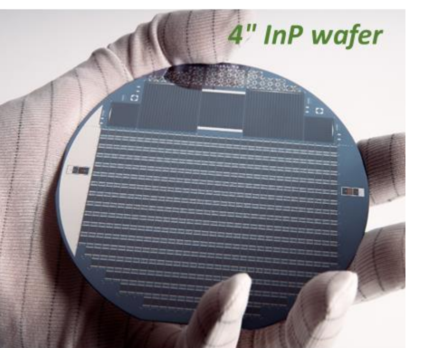
WHAT IS SILICON PHOTONIC ?

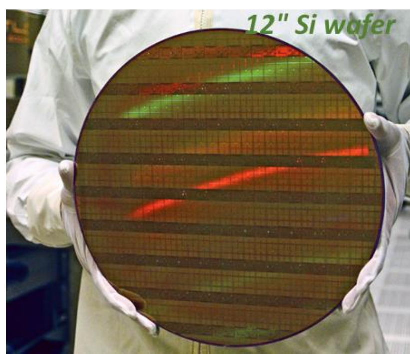
- Silicon photonic aims at integrating in the **silicon microelectronic CMOS technology circuits** and modules initially based on other technologies (InP, InGaAs, LNbO3, SiO2, …)

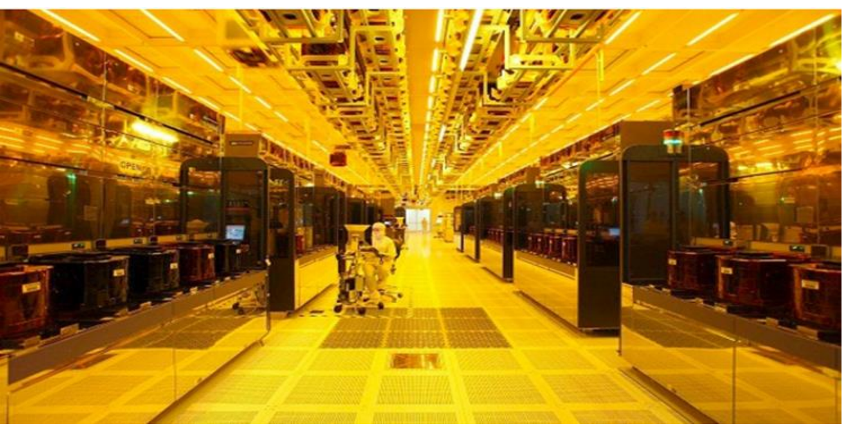
- Making photonic integrated circuits on Silicon using **CMOS process** technology in a **CMOS fab**.

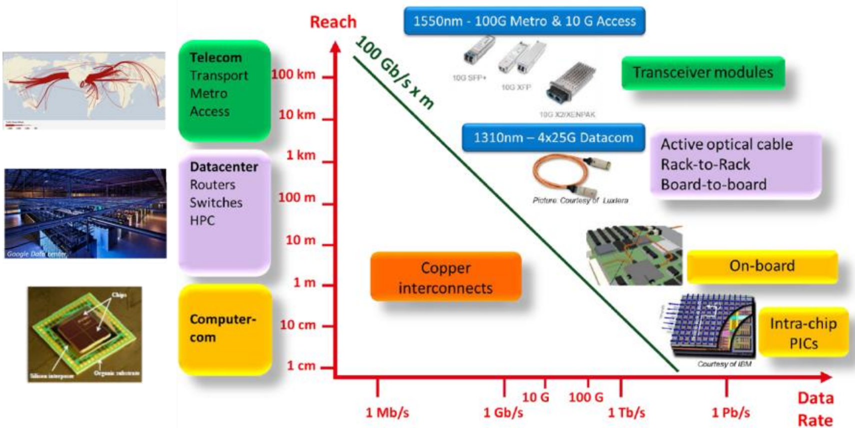
- Merging photonics and CMOS.

- **Expected benefits:**
  - Higher integration level
  - Low cost, high volume facilities
  - Access to mature packaging and EDA tools
  - WDM and scaling to >1 Tb/s
  - Solving electrical interconnect limits in Data centers, Supercomputers and ICs with higher capacity, lower cost optical interconnects









BUILDING BLOCKS FOR OPTICAL DATA TRANSMISSION

Photo-detector:
E to O conversion

De-Multiplexer:
Signal separation

Electrical
Data Out

Detector
Detector
Detector
Detector

De-Multiplexer

Optical
Data In

Fiber Coupler

Driver

Electrical
Data In

Laser λ4
Laser λ3
Laser λ2
Laser λ1

Modulator
Modulator
Modulator
Modulator

Multiplexer

Optical
Data Out

Fiber Coupler

Fiber coupler:
PIC to fiber interface

Modulator:
E to O conversion

Multiplexer:
Signal combining

SILICON PHOTONIC CORE TECHNOLOGY DESCRIPTION

Metal2
W-Via
Metal1
W-Plugs
Heater
NiSi
Grating Coupler
Wave Guides
Shallow Rib
Strip
Deep Rib
PN Junction Modulator
Ge PhotoDiode
BOX
Si Substrate

- 310nm SOI
- 193nm DUV lithography
- Multilevel silicon patterning
- Selective Germanium epitaxy
- Silicide

- Metal heater
- Planarized BEOL
- 2 AlCu routing levels
- UBM for Cu pillar assembly

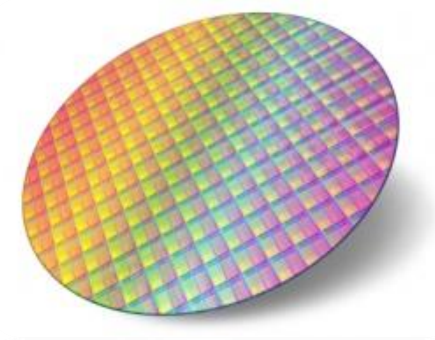
SILICON PHOTONIC CORE TECHNOLOGY DESCRIPTION

Silicon Photonic Process Flow

Step	Description
Silicon Implantation	○ Modulator junction formation & activation
Silicon Patterning	○ Define all the photonic devices ○ Various waveguide architectures
Germanium Epitaxy	○ Photodetector patterning ○ Germanium selective epitaxy
Germanium Implantation	○ Photodetector contact formation
Silicidation	○ Si Modulator contact silicidation
BEOL	○ Metal interconnection ○ Metal heater definition for λ tuning

CMOS-based process with photonic dedicated optimizations (Silicon Implantation through Germanium Implantation)

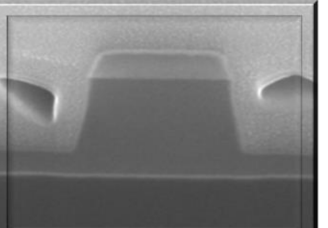
CMOS standard process (Silicidation and BEOL)



O-BAND DEVICE LIBRARY - EXAMPLE

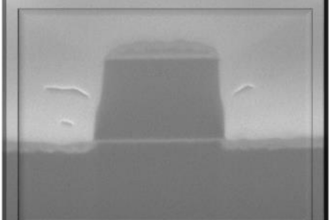
Rib WG

Width	400 nm
Prop. loss	**0.2dB/cm**



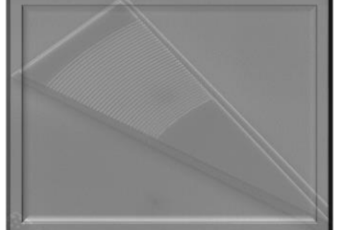
Deep rib WG

Width	320nm
Prop. loss	**0.7dB/cm**



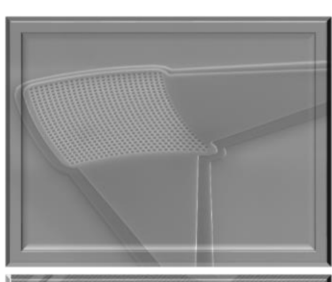
Strip WG

Width	350nm
Prop. loss	**1.1 dB/cm**



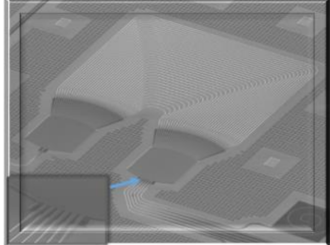
1D GC

Ins. Loss	<2.5dB
1dB BW	30 nm



2D GC

Ins. Loss	< 4dB
1dB BW	30 nm



AWG

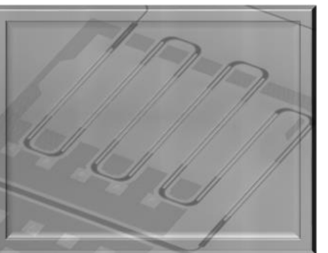
Ins. Loss	2-3dB
Xtalk	>20dB
1dB BW	1.5nm

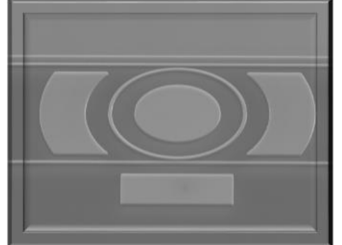
Crossing

Loss	< 0.25dB
Xtalk	>35dB

MMI

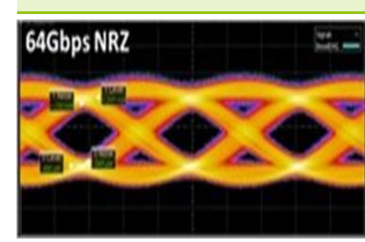
Loss	< 0.5dB
balance	$\pm$3%



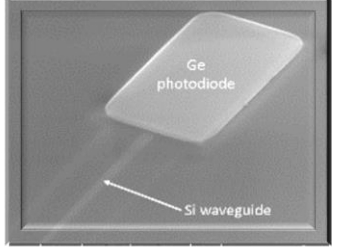


Si modulators

Length	2mm
$V\pi L\pi \approx$ @ -2V	1.5V.cm
Loss @ -0V	0.8dB/mm
NRZ modulation	



ER>4.5dB
SNR>7

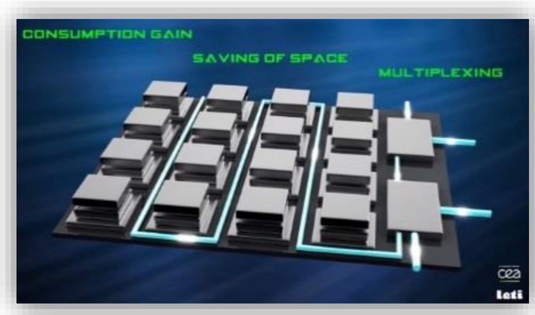


Ge photodiodes

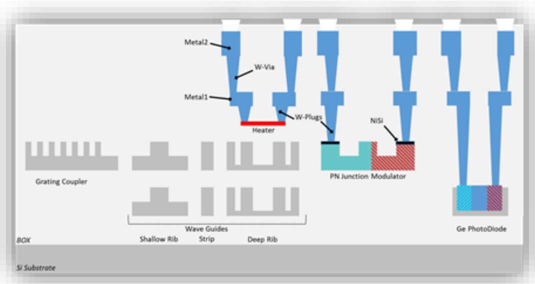
Width	**0.8µm**
Length	15µm
Responsivity	> 1.05A/W
Dark current @ -2V	5 nA
BW @ -2V	> 40GHz

EMERGENT NEEDS VS CORE PROCESS

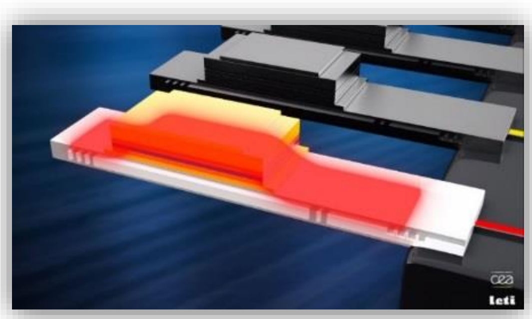
- **Co-integration with complex « hos chips »**
  - FPGA or switches with opti
  - Manycore
- add-on #1 : 3D packaging



- **Silicon Photonics address circuits of increasing complexity**
  - Hundreds of optical functions on a chip
  - Ease routing using multilay
  - Requires ded
  - Broadband quired for WDM modules
  - Thermal constraints
- add-on #2: Silicon-nitride



- **Laser source integration**
  - Several competing techn
  - Direct bond MOS compatibility
- add-on #3: III-V Integration

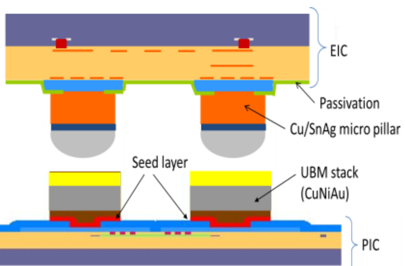


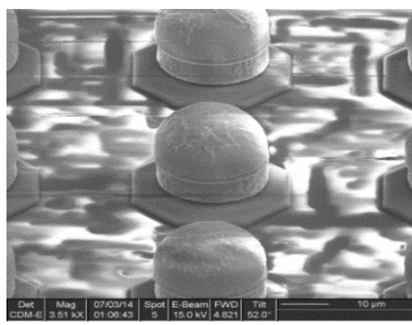
ADD-ON #1 : 3D PACKAGING

- **High data rate silicon photonics based module must be considered as an RF module with an E/O or O/E convertor: RF packaging solutions are needed**
  - ⇒ Si photonic platform must integrate Microbumps/Micropillars and/or TSV

MicroBump/Micropillars

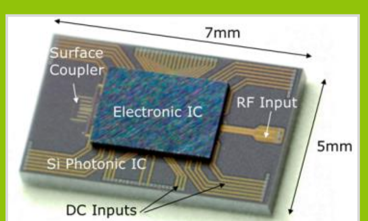
- 50 µm pitch
- Copper pillar with eutectic solder
- C2W or C2C assembly
- Low parasitics

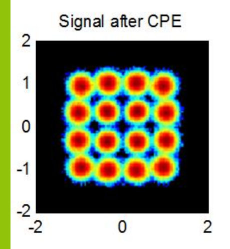




High Datarate Modules

Reflective Tx for FTTH (EU FABULOUS project)

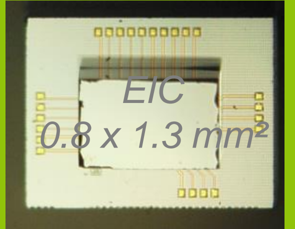


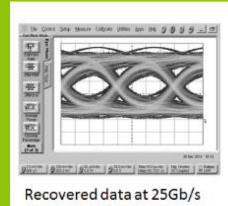


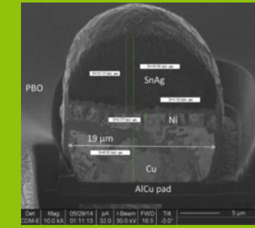
- QAM16 transmission on a single fiber
- Dedicated MZM segmented CMOS driver

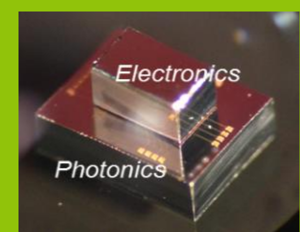
Straullu et al., ECOC PDP, 2016
Menezo et al., JLT, 34,10,2016

Low power 25Gbps photoreceiver





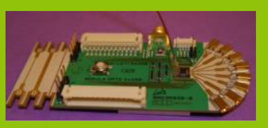


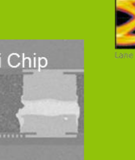


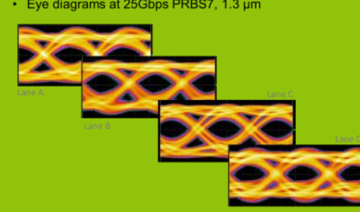
- 50µm pitch microbump
- 170 fJ/bit
- -15 dBm sensitivity
- TIA design : Caltech

Saaedi et al.. J. Lightwave Tech., 2015

4 × 25Gbps receiver module







- WDM and SDM versions
- < -12dBm sensitivity at 10^{-9} BER
- EIC with 4pJ/bit consumption
- TIA design : ST microelectronics

Bernabé et al., OIC 2016, Paper MB3
Castany et al., ESTC 2016

ADD-ON #1 : 3D PACKAGING

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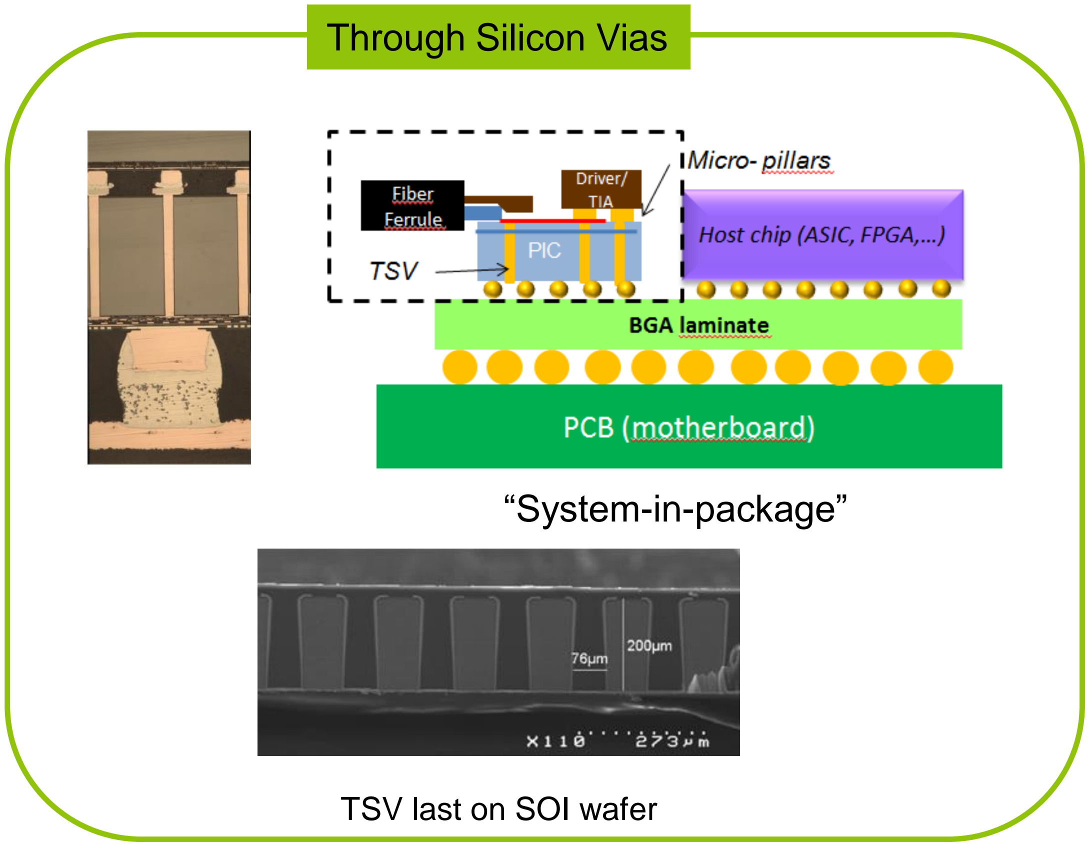
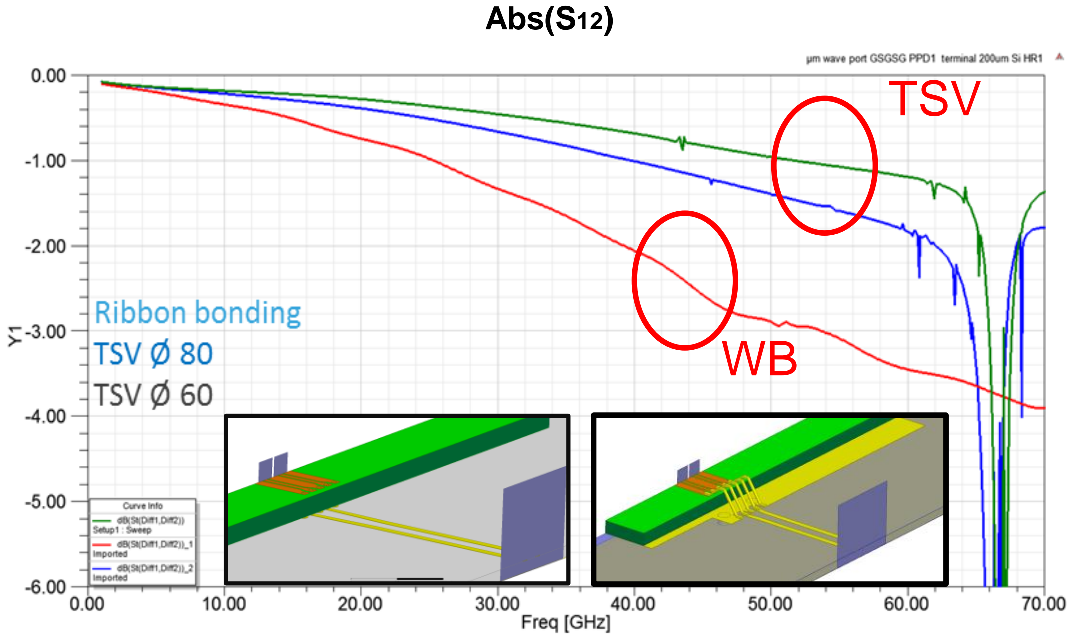
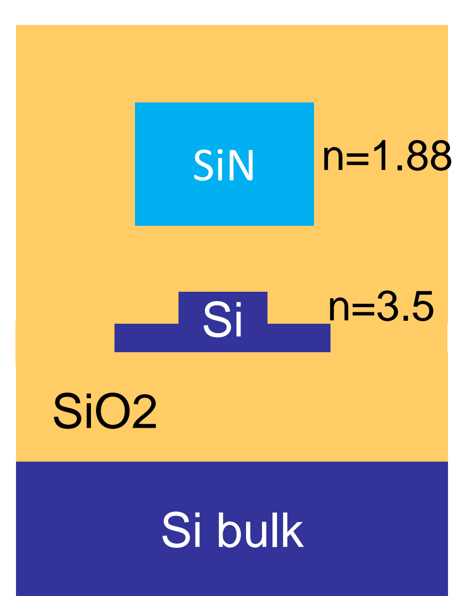




TSV vs WB on Transmission performances

S. Bernabé, K. Rida, S. Menezo, *IEEE Trans. Comp. Mfg and Pkg, 2016*
L. Fourneaud, *Internal report*

ADD-ON #2: SILICON-NITRIDE AS A PHOTONIC LAYER



Why Silicon nitride:

- Low refractive index (n_{SiN} = 1.88)

→ less sensitive to roughness and fabrication imperfections

→ lower propagation losses

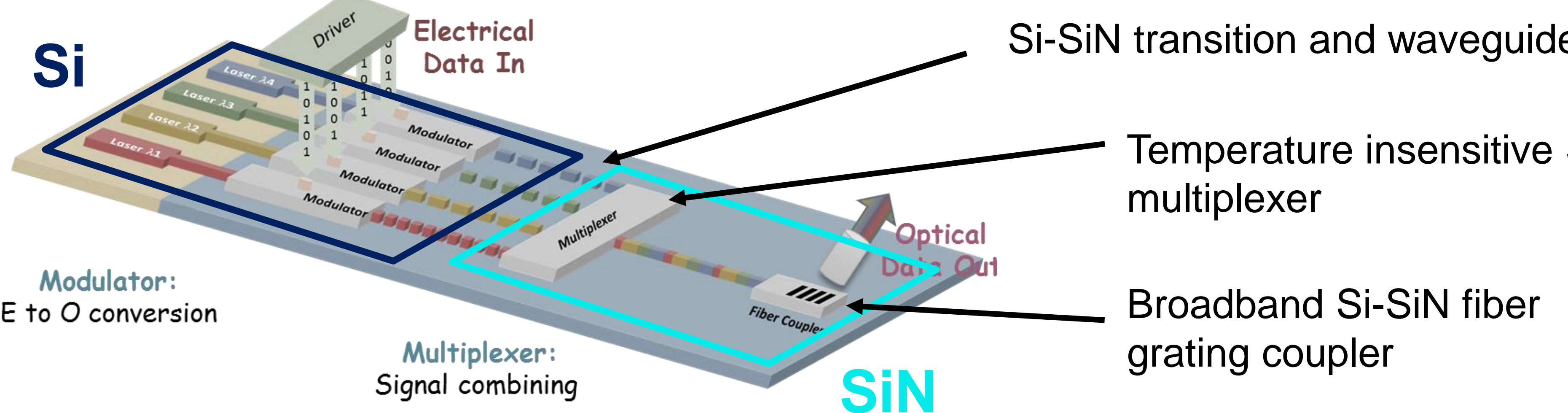
- Low thermo-optic coefficient (~$2x10^{-5}$ K^{-1})

→ Temperature quasi-insensitive devices for data center environment

Objective: CWDM transceiver in the O-band (1260-1340nm)

CWDM: Coarse Wavelength Division Multiplexing. 4 channels (= 4λ) with 20nm spacing.
No temperature control of the lasers.

Si-SiN platform: Active properties of Si and passive properties of SiN



Q. Wilmart *el al., in Proc.* of SPIE Phot. West 2018

SI-SIN FABRICATION & PERFORMANCE

SOI 300nm
BOX 2µm

SiO2
Si

1st encapsulation

SiO2
Si

Planarization
CMP stop on HM

SiO2
Si

SiO2
Si

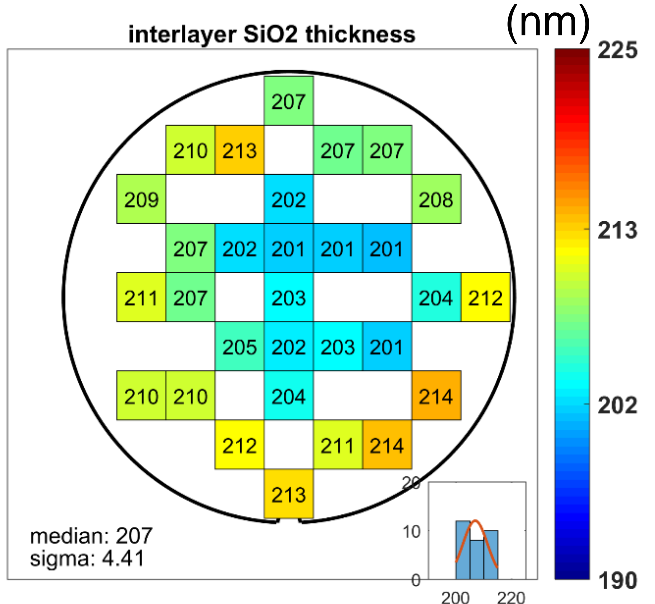
Oxide deposition 200nm

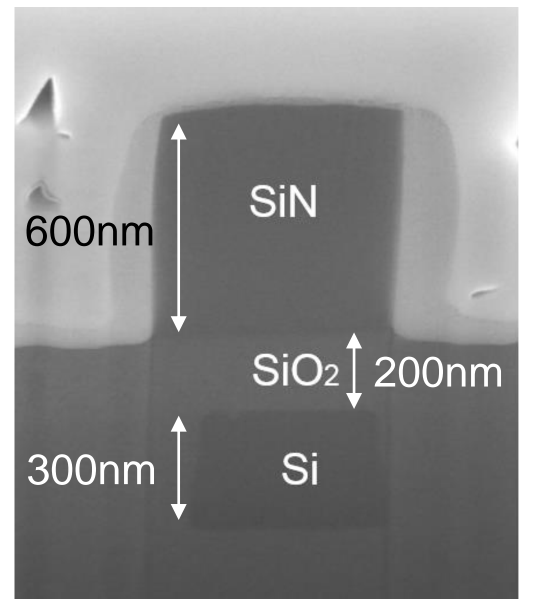
SiN
SiO2
Si

SiN deposition (600nm PECVD 300°C)
+ patterning (DUV 248nm)

SiN
SiO2
Si

Final encapsulation

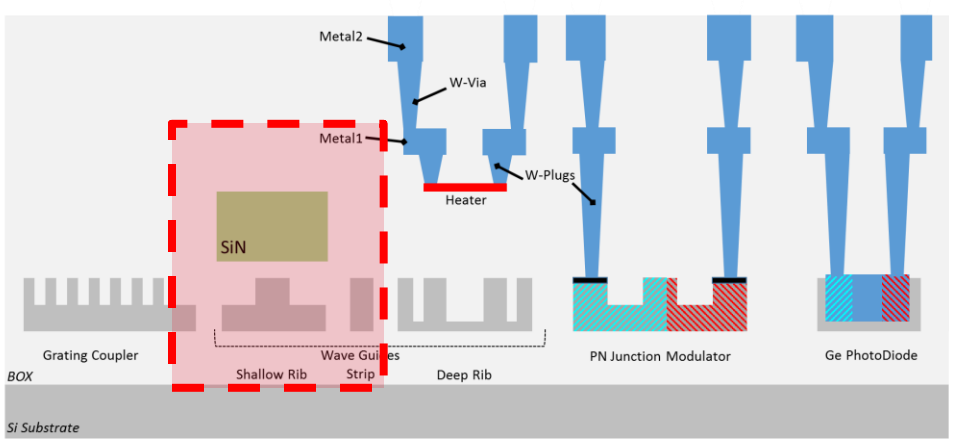




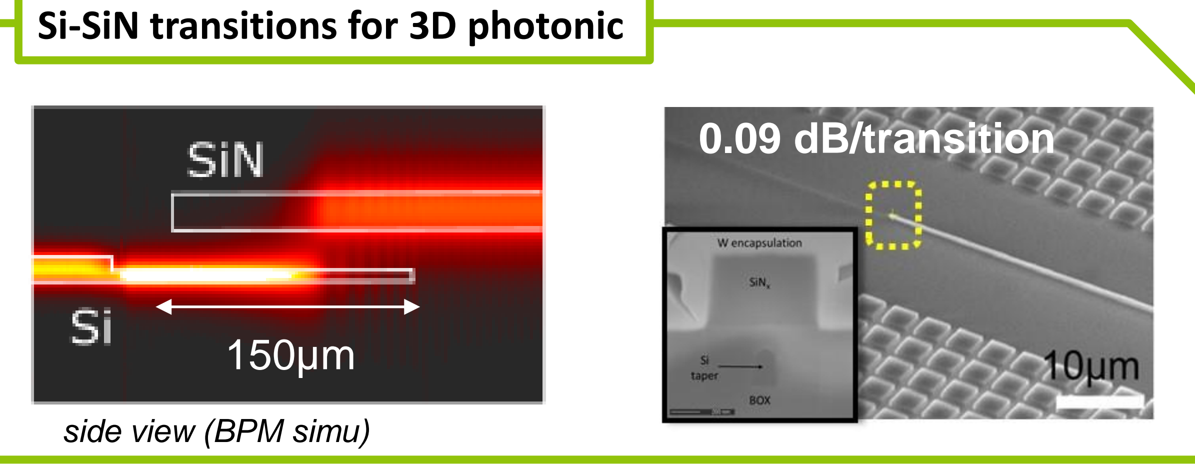
- Low temperature deposition of SiN → Si doping compatibility
- SiN waveguide propagation loss : 0.8 dB/cm
- SiN thermo-optic coeff. : 1.7×10^{-5} K^{-1} (in Si 2×10^{-4} K^{-1})

Q. Wilmart *el al., in Proc.* of SPIE Phot. West 2018

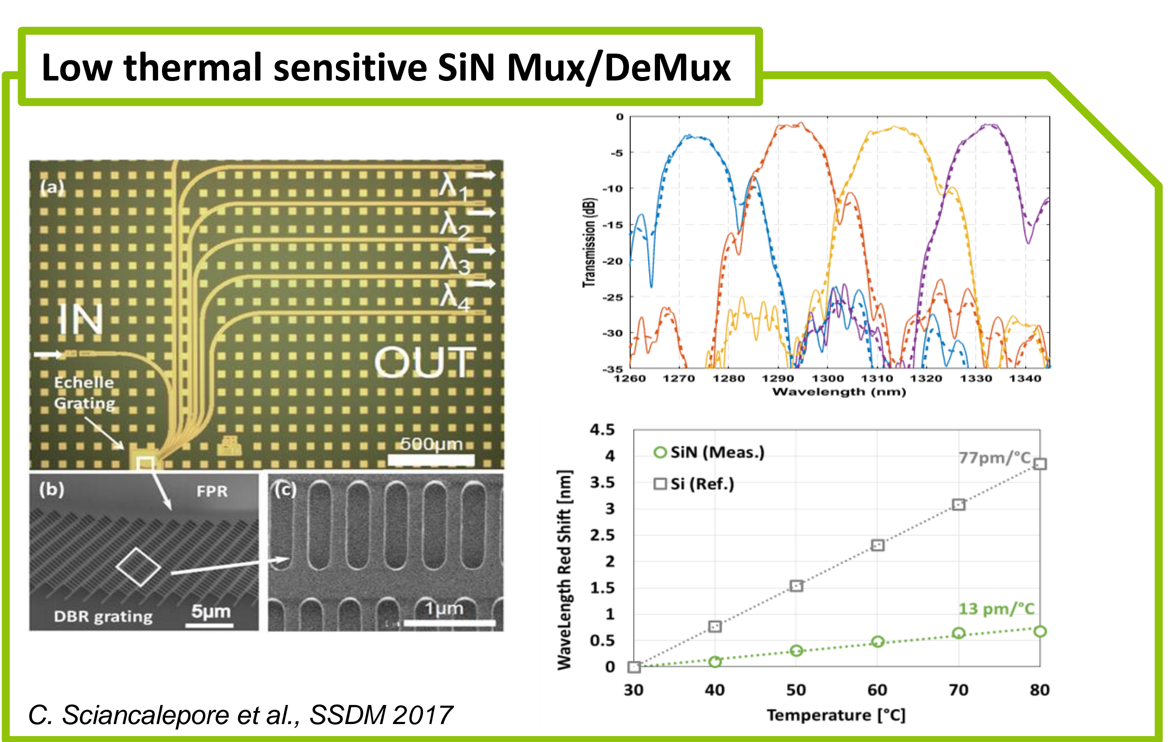
MULTIPLE PHOTONIC LAYER INTEGRATION



Si-SiN transitions for 3D photonic

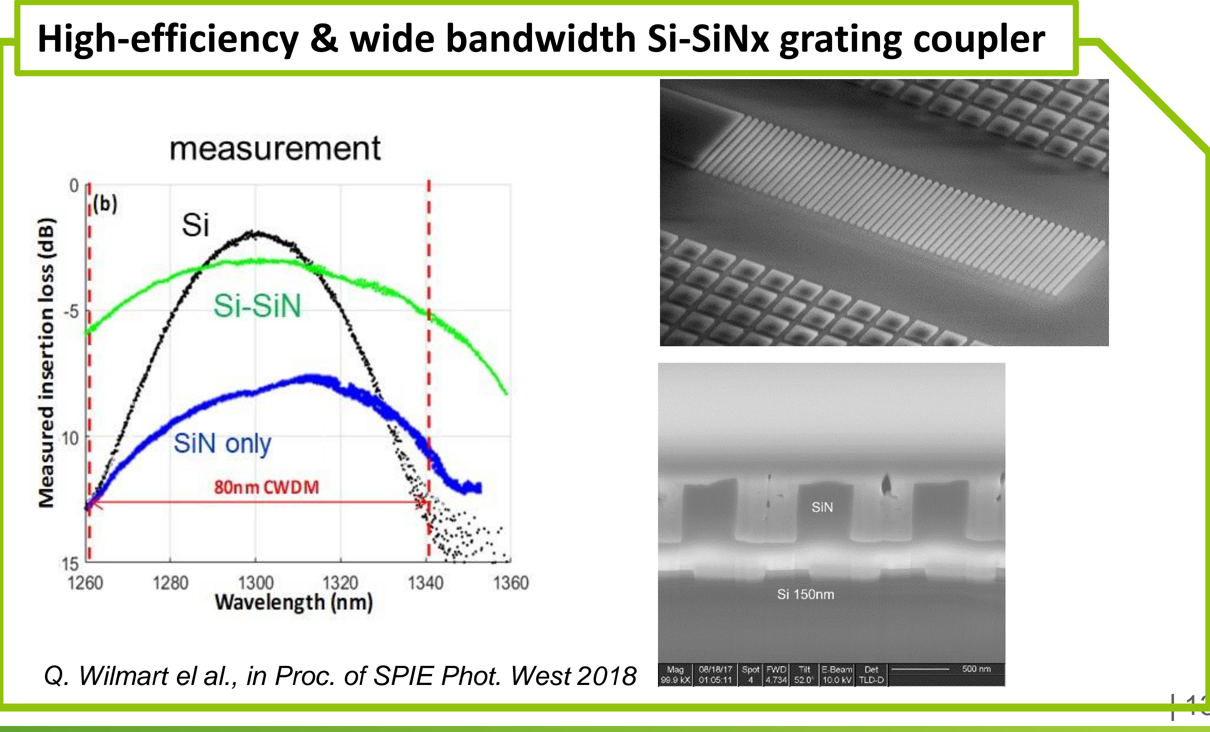


Low thermal sensitive SiN Mux/DeMux



C. Sciancalepore et al., SSDM 2017

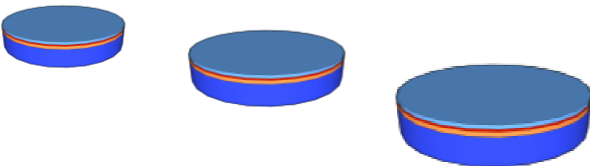
High-efficiency & wide bandwidth Si-SiNx grating coupler



Q. Wilmart el al., in Proc. of SPIE Phot. West 2018

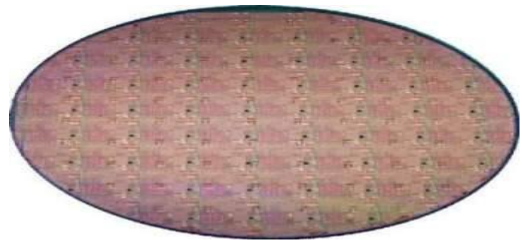
ADD-ON #3: III-V INTEGRATION ON SI-PHOTONIC CHIP

- Growth of the III-V wafers (2'', 3'', 4'')

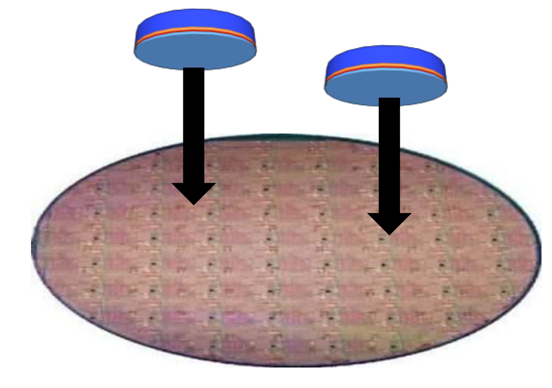


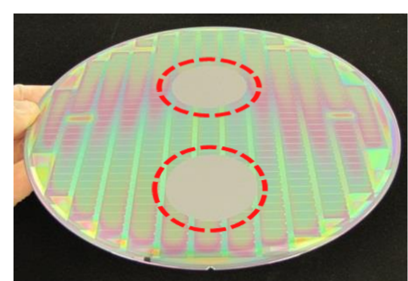
- Processing of SOI wafers 8'' or 12''

(modulators, detectors, passive devices, etc.)



III-V bonding on processed SOI
& InP substrate removal





- III-V material patterning,
- Metallization of lasers, modulators and detectors

CMOS fab compatible processes needed to avoid wafer downsizing and maximize the functional SOI wafer surface.

HETEROGENEOUS III-V INTEGRATION

Components

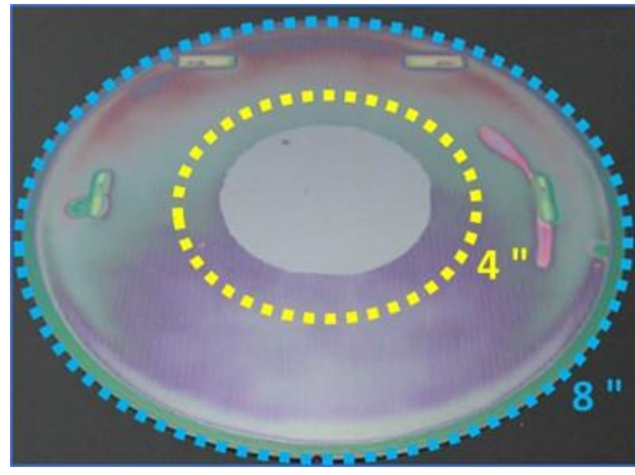
- Laser
- Electro-absorption modulator
- Semiconductor optical amplifier

To use the advantage of each material properties:

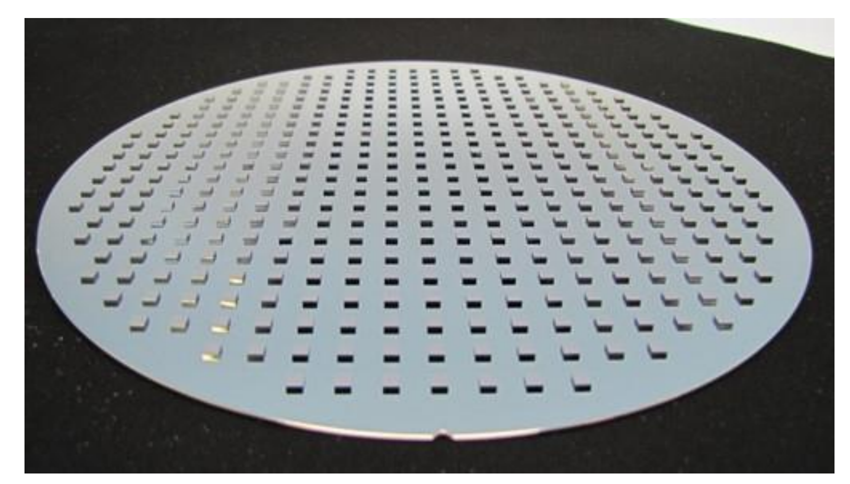
- Optical gain is provided by the III-V (InP/InGaAsP –QWs or AlGaInAs)
- The high resolution laser cavity as well as the PIC is fabricated in a 200/300mm Silicon platform (CMOS planar technology)

To localize III-V by die-to-wafer bonding

- Highly flexible approach (multiple laser-λ in the O+C+L bands / PD / EAM)
- Equivalent to multiple localized epitaxies



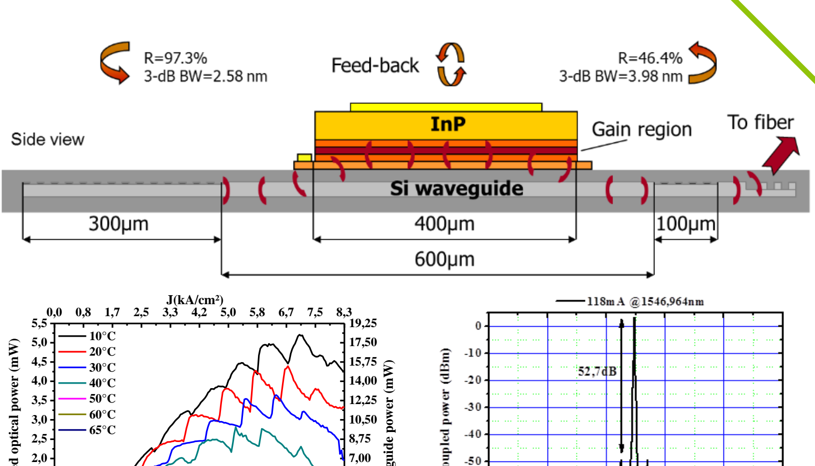
III-V wafer bonding



Die bonding

INTEGRATED HYBRID III-V/SI LASER PAST RESULTS

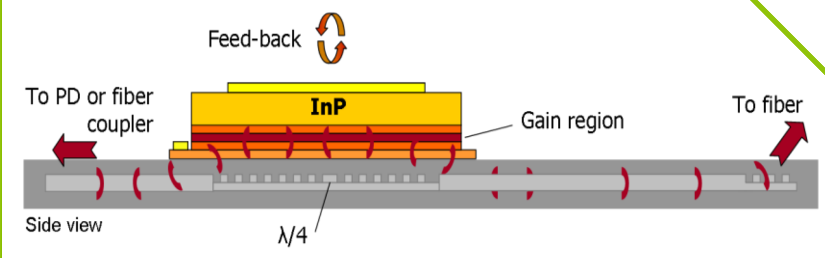
Hybrid DBR @ 1,55µm

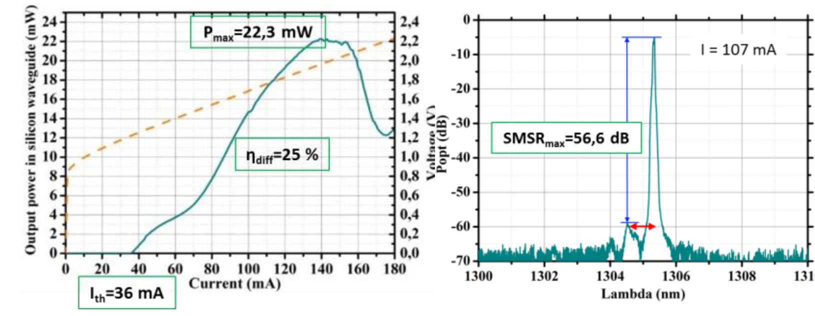


- CW operation (>60°C)
- I_{th}: 17-60mA (0.8-2.5 kA.cm^{-2})
  - for T: 10 to 60°C
- Rs= 7.5 Ω
- Lasing turn-on voltage : 1.0 V
- **P**$_{\text{-Si-waveguide}}$ > 14 mW (20°C)
- **P**$_{\text{-fiber}}$ > 4 mW (20°C)
- SMSR > 40 dB

A.Descos *et al.*, ECOC 2013

Hybrid DFB @ 1,31µm

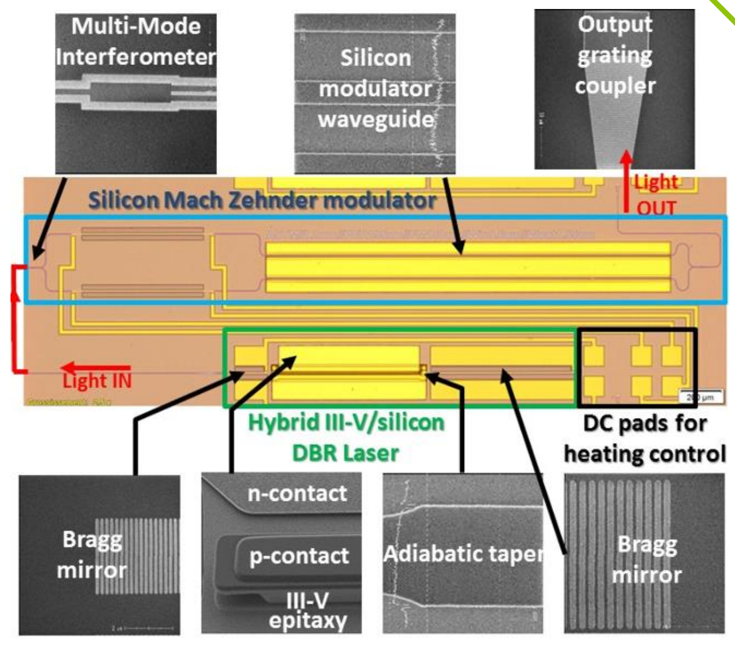


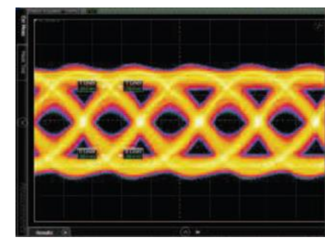


- CW operation (>55°C)
- Ith: 30-50mA
- Rs= 15 Ω
- Lasing turn-on voltage : 1.2 V
- P-Si-waveguide > 20 mW (20°C)
- P-fiber > 3 mW (20°C)
- SMSR > 40 dB

H. Duprez *et al.*, Opt. Express 23(7), 8489 (2015)

25Gb/s laser + MZM transmitter



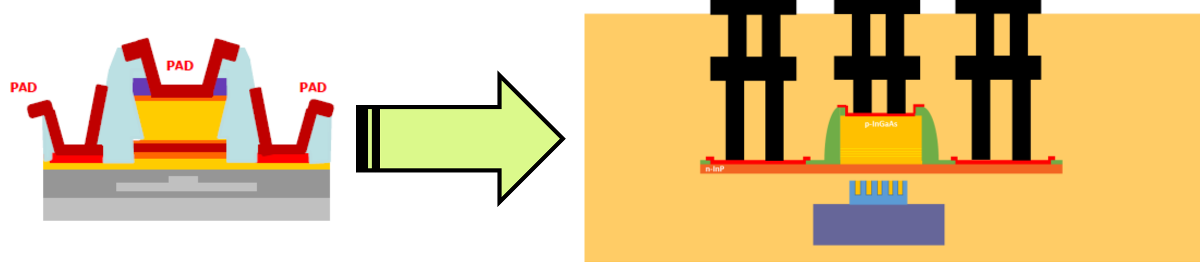


- Co-integration hybrid IIIV/Silicon DBR laser + silicon Mach-Zehnder modulator.
- 25Gb/s transmission at 1.3µm up to 10km.

T. Ferrotti et al. , SSDM, (2016)

III-V INTEGRATION ON SI: TOWARD LSI CMOS COMPATIBLE PROCESS

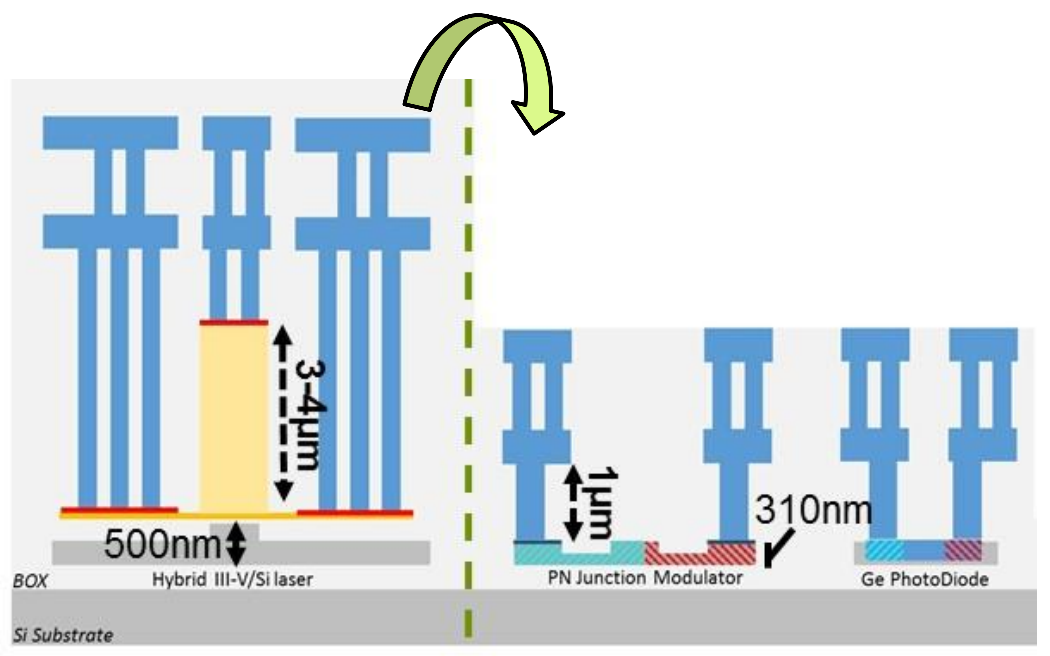
1. Process & Materials
   - Patterning
   - Contact on III-V
   - Multi level BEOL
   - III-V Die Bonding



2. Laser Topography
   - III-V stack thickness=4µm vs. PMD thickness=1µm

3. SOI Substrate
   - SOI for laser: 500nm vs. SOI platform: 310nm

4. Laser integration impact on other devices



LARGE SCALE INTEGRATION CMOS FRIENDLY PROCESS

Multilevel planar BEOL

Ohmic contacts on III-V materials

III-V patterning

Collective III-V die bonding

Localized silicon thickening

B. Szelag et al., IEDM 2017

LARGE SCALE INTEGRATION CMOS FRIENDLY PROCESS

Ohmic contacts on III-V materials

p-InGaAs

Specific Contact Resistivity [Ohm.cm²]

III-V fab POR

5.7 x 10⁻⁶ · 4.6 x 10⁻⁵ · SCHOTTKY · SCHOTTKY · 8.8 x 10⁻⁶ · 1.9 x 10⁻⁵ · 7.5 x 10⁻⁶ · 5.6 x 10⁻⁶ · 2.0 x 10⁻⁴ · SCHOTTKY · 1.2 x 10⁻⁵ · 1.1 x 10⁻⁵ · 8.8 x 10⁻⁵ · 2.4 x 10⁻⁵

n-InP

Specific contact resistivity [Ohm.cm²]

III-V fab POR

1.5 x 10⁻⁵ · SCHOTTKY · 2.5 x 10⁻⁵ · 1.9 x 10⁻⁵ · 2.3 x 10⁻⁵ · SCHOTTKY · 5.9 x 10⁻⁵ · 2.3 x 10⁻⁵ · 2.6 x 10⁻⁵ · SCHOTTKY · 4.3 x 10⁻⁶ · 7.3 x 10⁻⁶ · SCHOTTKY · 1.3 x 10⁻⁵

Au/Pt/Ti - lift-off · Au/Pt/Ti - planar integration · Ti - As deposited · Ti - T = 250 °C · Ti - T = 350 °C · Ti - T = 550 °C · Ni - As deposited · Ni - T = 340 °C · Ni - T = 350 °C · Ni - T = 450 °C · Ni_xP with PC - As deposited · Ni_xP with PC - T = 350 °C · Ni_xP without PC - As deposited · Ni_xP without PC - T = 350 °C

Multilevel planar BEOL

III-V patterning

SiN (hard mask)
InGaAs (P-type contact)
InP
MQW
InP (N-type contact)
Gain
n-InP (Mesa)
Si waveguide
SiO2

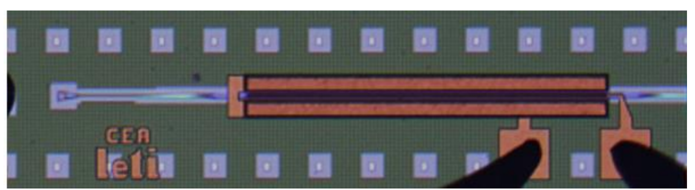
Silicon localized thickening

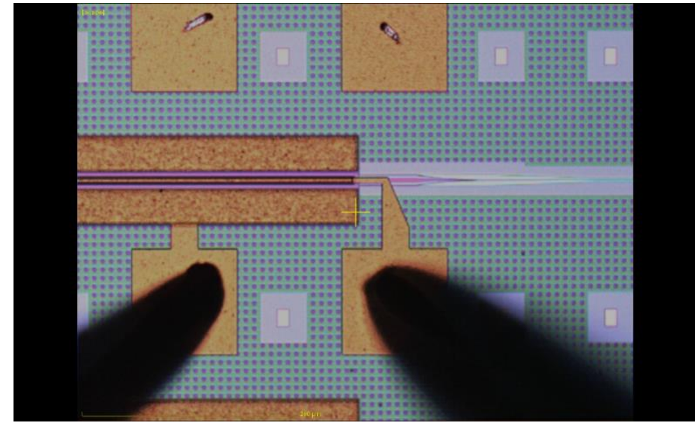
Amorphous Silicon
SiO2
Bulk Silicon
62nm
103nm
94nm

NANOELEC

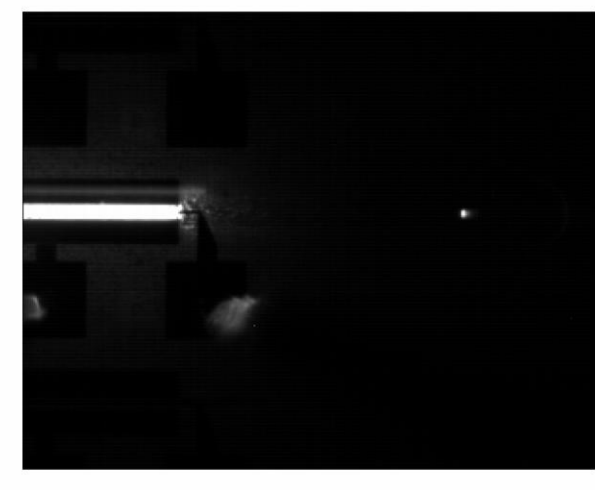
Institut de recherche Technologique Nanoelec

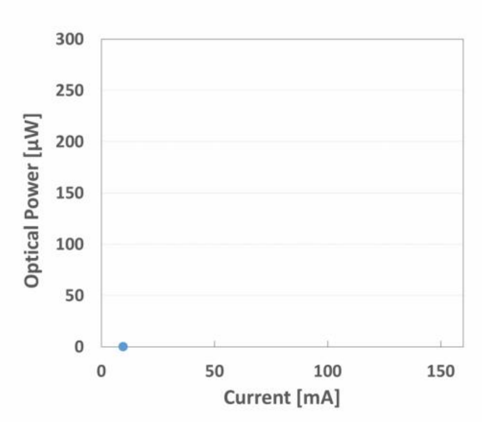
FIRST DEMO ON 200MM SOI WAFER OPTICAL CHARACTERIZATION

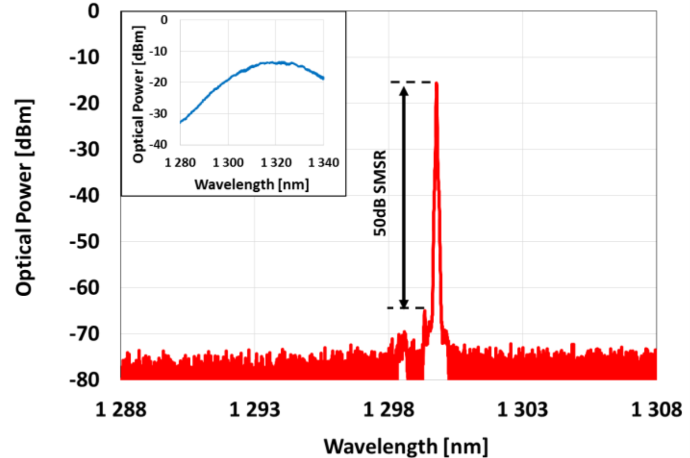




- Only 1 metal layer for this design
- Ni-based N & P contacts







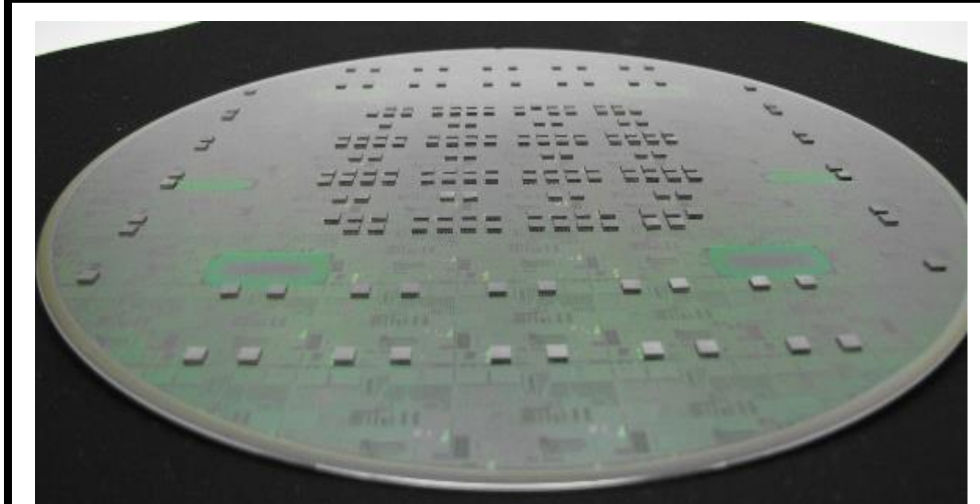
- Ith: 55-65mA
- Rs= 10 Ω
- Max P-Si-waveguide > 3 mW
- Max P-fiber ≈ 1 mW
- SMSR > 40 dB (best 50dB)

@room temperature

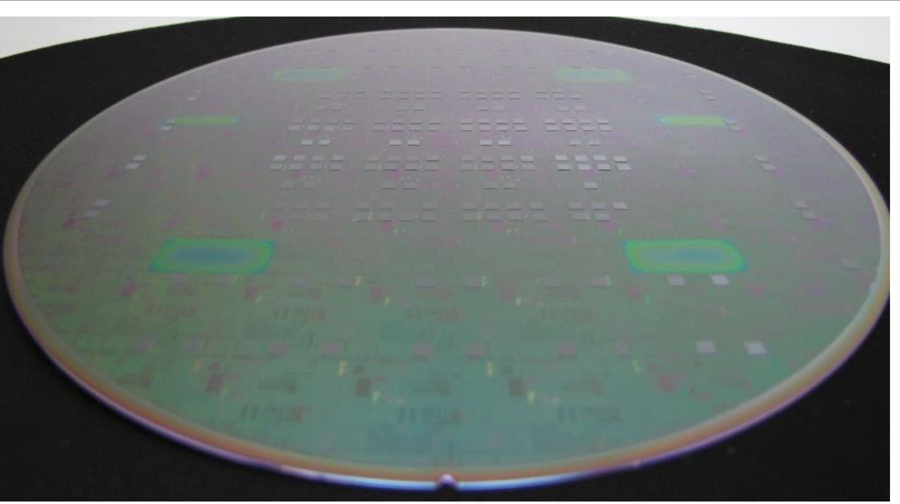
COLLECTIVE DIE BONDING WITH SILICON HOLDERS

- + Efficient cleaning
- + Very high transfer rate >95%
- + Bonding Yield~100%
- + CAD2MASK Holder mask generation during PIC design
- - Additional cost for holder fabrication

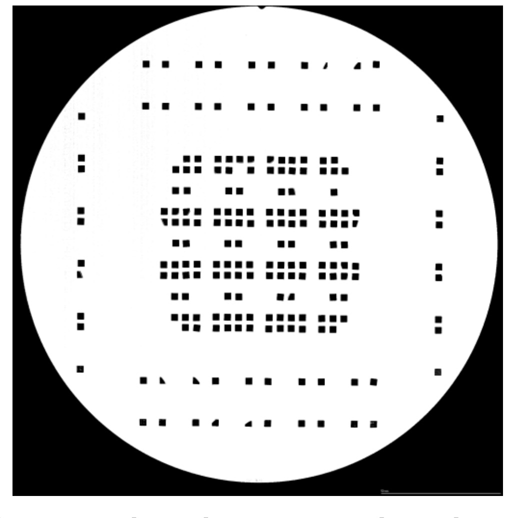
COLLECTIVE DIE BONDING WITH SI HOLDER - EXAMPLE



After die Bonding



After InP grinding



Acoustic characterization

	P01	P02	P03	P04
○ Transferred die:	99 %	99%	99%	70%
○ Transferred die without defects:	75 %	73%	73%	52%
○ Transferred die & bonded on more than 99% of their surface:	87 %	84%	88%	62%
○ Transferred die & bonded on more than 95% of their surface :	91 %	85%	90%	64%

BACKSIDE INTEGRATION (BSI) CONCEPT

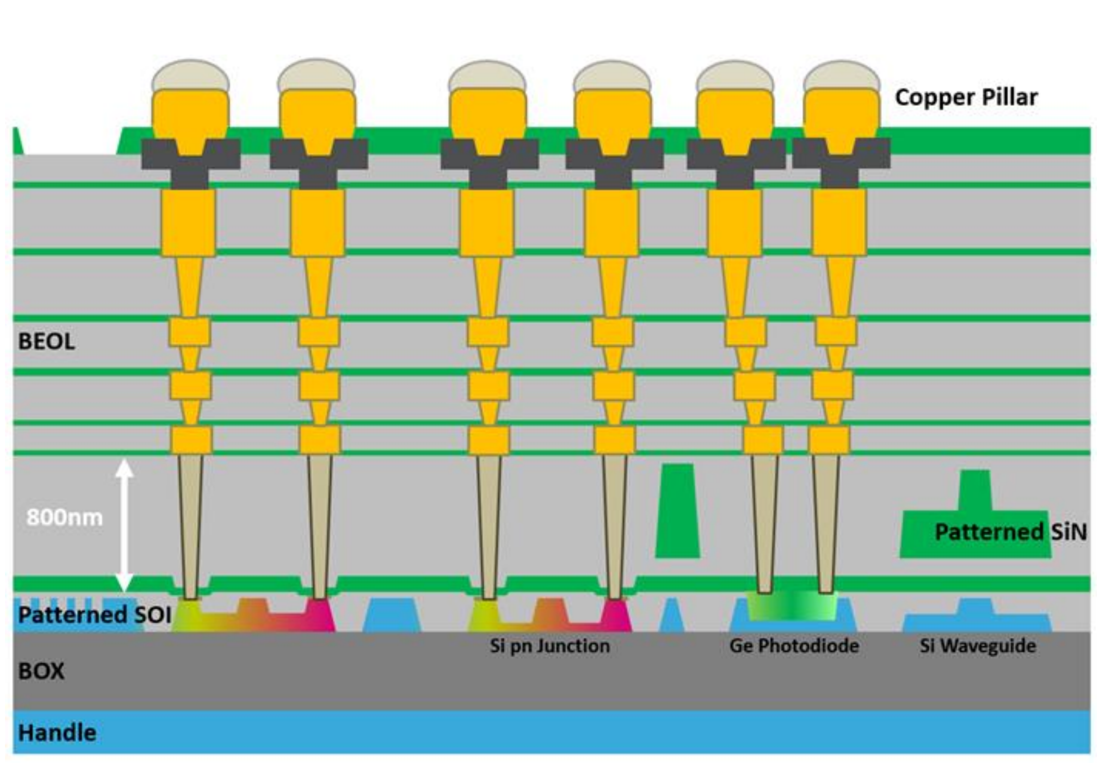
Problems:

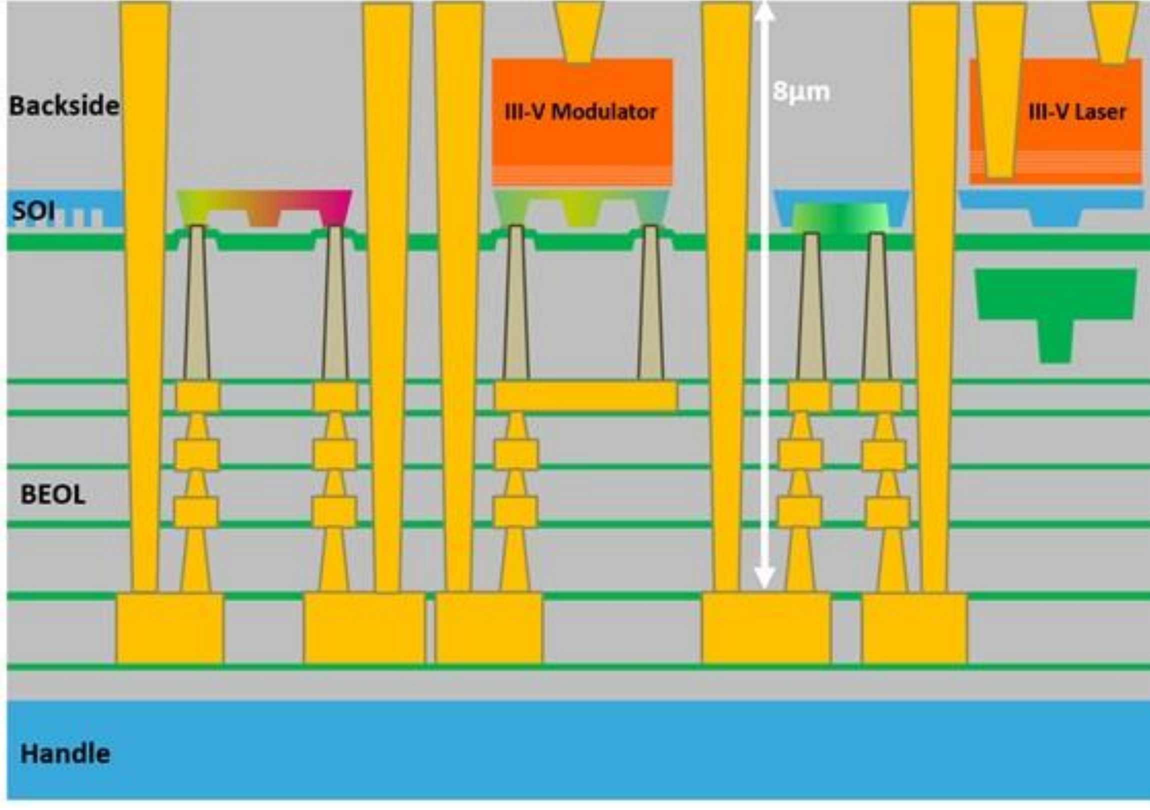
1. III-V based device integration with not change on the baseline photonic platform (BEOL)
2. III-V based device integration compatible with a co-integration of SiN devices

Solution:

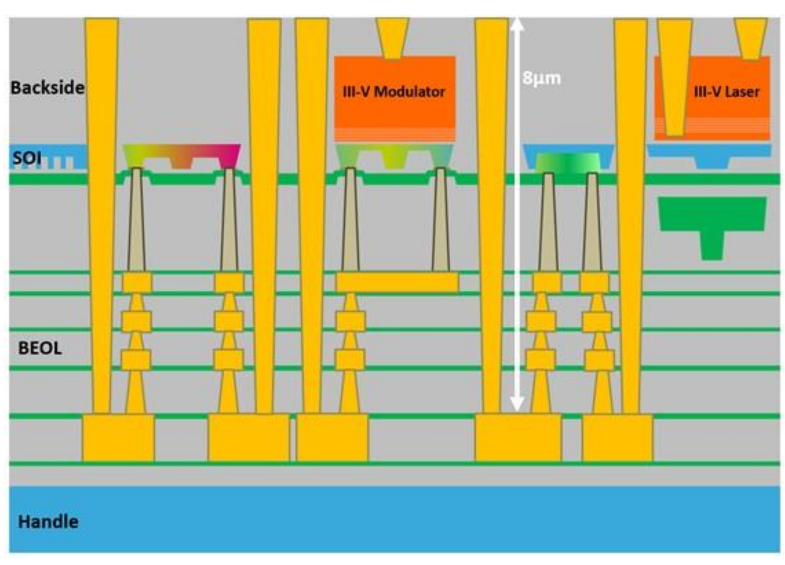
⇒ III-V post processing on the backside of the full silicon photonic platform

life.augmented





HYBRID LASER BSI DEMONSTRATION



- Integration scheme compatible with any photonic platform
- No impact on the Silicon photonic platform
- Modular integration
- Si photonic platform and laser integration can be done in 2 different fabs
- Only way to have ‘3D photonic’ (SiN or Si level on top of SOI) and laser on the same die
- EIC and Laser @ opposite sides of the PIC
- Demo: Passive + BSI DBR laser done with 100mm process (J. Durel et Al, IEDM 2016)

CONCLUSION

Silicon Photonics CORE process

- 3D Photonics (SiN/Si, Si/Si)
- III-V on Silicon (FSI or BSI)
  - 200mm III-V CMOS compatible process
  - Large scale die to wafer bonding
- 3D packaging

Thank you

Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
www.leti-cea.com