



Leti D43D Workshop

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Operations, engineering and technology management. Tool selection, start up and ramp of HVM lines for 200/300mm. Technology transfer from/to US/ASIA.

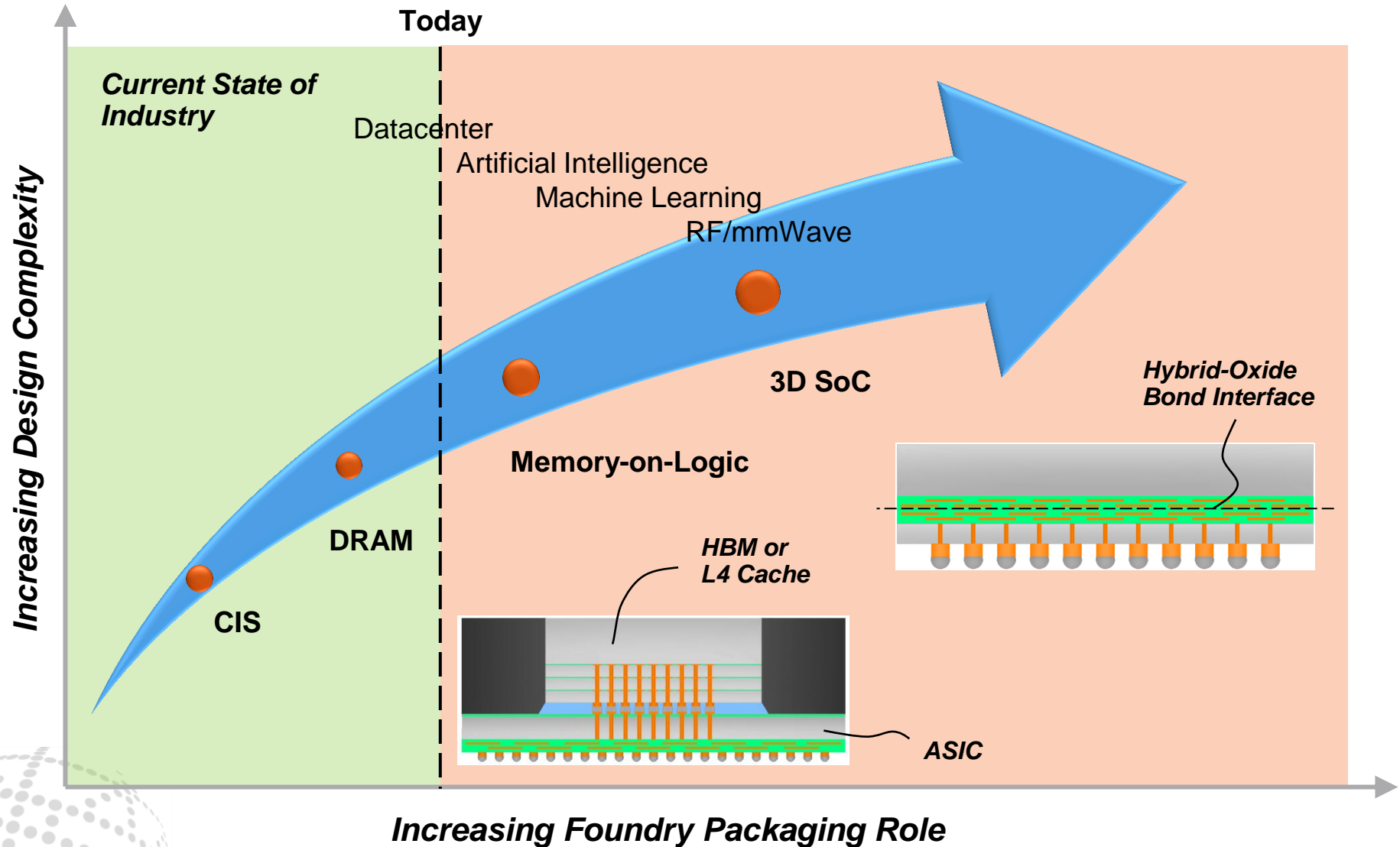
Development of bump interconnects (lead free, copper pillar, micro pillar).

RF/MMW package design and verification methodology with chip to package co-design/simulation. EDA integration 3D WLP.

Technology selection and manufacturing of high volume semiconductor lines. Technology and product qualification for outsourced manufacturing.

Design automation for mixed signal RF/Digital nodes (22FDX/45RFSOI). Millimeter wave test site design and characterization

3D Packaging: Increasing Levels of Integration



Advanced Packaging Industry Landscape

- Industry is moving toward increasing levels of heterogeneous integration and memory density in package.
- Scalable compute packaging is an emerging trend:
 - Single small die is used for low end needs; many small dies are packaged in parallel for high performance needs.
- Datacenter bandwidth and performance needs are driving photonic packaging.

Application	Package Types
Data Center	<ul style="list-style-type: none">• Large 2.5D packages with HBM and ASIC w/ 3D SRAM.• 3D ASIC with L3 cache partitioned as separate die.• SiPh MCMs with multiple fiber arrays.
Artificial Intelligence (AI) & Machine Learning (ML)	<ul style="list-style-type: none">• ASIC w/ 3D SRAM.• Scalable computing systems dependent on end application.
Internet of Things (IoT)	<ul style="list-style-type: none">• System level packages with many different device types and process nodes (i.e. CMOS, GaN, MEMS, etc).• Multi-chip Fan Out or Si Interposer.
RF & mmWave	<ul style="list-style-type: none">• Multi-chip modules with several heterogeneous dies (i.e. LNA, PA, Switch, Filter, etc).• 3D integration w/ TSV Last processing.• Integrated antennae and passives key need.

Thank you



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