



FACE-TO-FACE INTEGRATION OF AN ELECTRO-OPTICAL LINK WITH CMOS DRIVERS AND THERMAL CONTROL

D43D Workshop – Leti Innovation Days 2018 | Yvain Thonnart



SILICON PHOTONICS FOR SHORT-RANGE COMMUNICATION

Silicon Photonics moves forward for long distance optical wireline transceiver

• 100 / 400 Gigabit Ethernet

Large-scale electronics longs for low-latency low-energy dense communication

Optical short-range communication has been a long-term target for years

- Needs compact optical devices to maximize bandwidth per mm²
 - Microring optical resonators





MICRORING MODULATOR BASED LINK





MICRORING: OPTICAL RESONANT CAVITY

Compact optical devices

• Highly resonant: Q-factor 10,000–30,000

Any refractive index change shifts the resonant wavelength

PN or PIN diode junction can be created inside the ring for electrical control

- Different uses depending on diode
 - PN rings can be used as modulators (> 10 Gbps)
 - PIN rings can be used as filters (<500 MHz) for routing and wavelength demultiplexing

But Subject to Temperature variations

➔ Low-frequency resonance shift

 $\lambda_{res} = \frac{P \, n_{eff}}{r}$ Phase= $(2k+\epsilon)\pi$ Phase=2kπ

MODULATOR PRINCIPLE, THERMAL SENSITIVITY DA/DV & DA/DT MEASUREMENTS



Ceatech



— T 27°C — T 40°C — T 60°C



<u>Ceatech</u>

HEATER EFFICIENCY & DA/DP MEASUREMENTS



Heating using doped Silicon

Resistive path inside the ring

Average ring temperature increase:

- Simulation: dT/dP ~ 2K/mW
- Measurements: $d\lambda/dP \sim 40pm/mW$



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RING MODULATOR OPERATION (TUNING+MODULATION)

Ring resonant wavelength unpredictible at design time

1 nm thickness variation

 ≈ 1 nm resonance shift

 But finesse, free-spectral-range & amplitudes are well-controlled

Thermal tuning is used to align ring resonance on laser source

• Low-frequency control

Voltage is used to modulate light

High frequency modulation





LOCKING ON REFERENCE CURRENT LEVEL VIA USE OF DROP PORT & PHOTODIODE

Ring resonance can be tracked by transmission on drop port

- Setpoint on through port corresponds to a power value on drop port
- Photodiode converts this to photocurrent
- Analog control used to match
 photocurrent with reference
- Joule heating by resulting heater driver current





PHOTONIC LAYOUT





LONG-TERM INTEGRATION PLAN





SHORT-TERM INTEGRATION: 3D TECHNOLOGICAL STACK

Copper-pillar Face-to-face assembly

- CMOS: STMicro. 65nm LP
- Photonic: STMicro. Internal 100nm SiPho

Wire-bonding on Photonic die

Vertical Fiber array on grating couplers







ELECTRONIC DIE



Functional area per λ

- Heater control
 - 40×40μm²/λ
 - 40×40µm²/WDM
- Tx Driver
 - 40×40µm²
- Rx Driver
 - 80×40µm²

Dominated by 6 Cu-Pillar area

- Pitch 40µm
- 2 for Modulator
- 2 for Photodiode
- 2 for Heater



PHOTONIC DIE



Functional area per λ

1 ring + 1 photodiode
120×80μm²/λ

Dominated by 6 Cu-Pillar area

- Pitch 40µm
- 2 for Modulator
- 2 for Photodiode
- 2 for Heater



FACE-TO-FACE MICROBUMP ASSEMBLY





BOARD INTEGRATION

RF out







FIBER POSITIONING ON GRATING COUPLERS











EXPERIMENTAL SETUP









CIRCUIT OBJECTIVE: PRESERVE COMMUNICATION DESPITE ENVIRONMENTAL PERTURBATION

Experiment: 4Gbps modulation under laser wavelength wobulation 30pm_{pp} at 100Hz
 Simulate thermal effect of workload changes on package (~1-10ms time constant)





THERMAL LOCKING AND STABILITY





ROBUST ELECTRO-OPTICAL LINK OPERATION UNDER PERTURBATION





ROBUST ELECTRO-OPTICAL LINK OPERATION UNDER PERTURBATION





ROBUST ELECTRO-OPTICAL LINK OPERATION UNDER PERTURBATION





3D-stacked CMOS / SiPho for short-range optical communication

- 10Gbps transceiver chip presented at ISSCC'18
- Wavelength locking achieved in 120µs
- Stability maintained under 900Hz environmental fluctuation
- Total CMOS footprint 0.01mm² / microring → up to 1Tbps/mm²

Perspective

• all-to-all optical network on chip architecture on interposer for high-density optical communication in high-performance computing systems



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