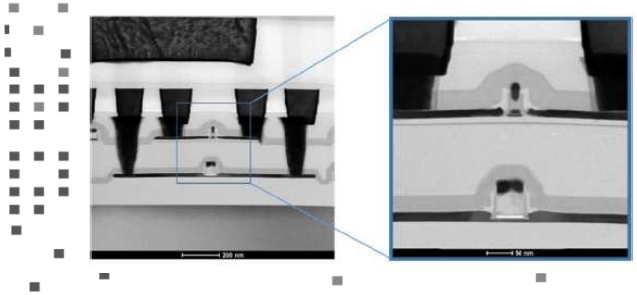
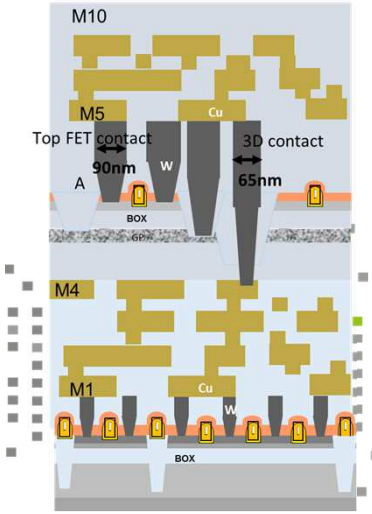
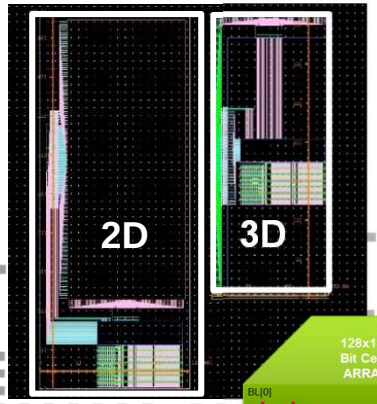
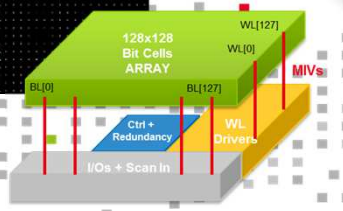
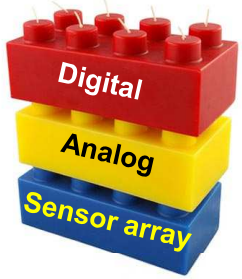


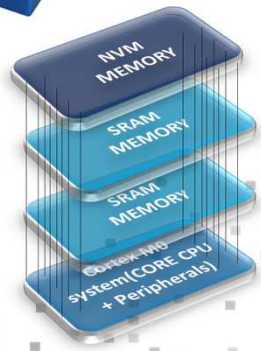








SinC
System in Cube



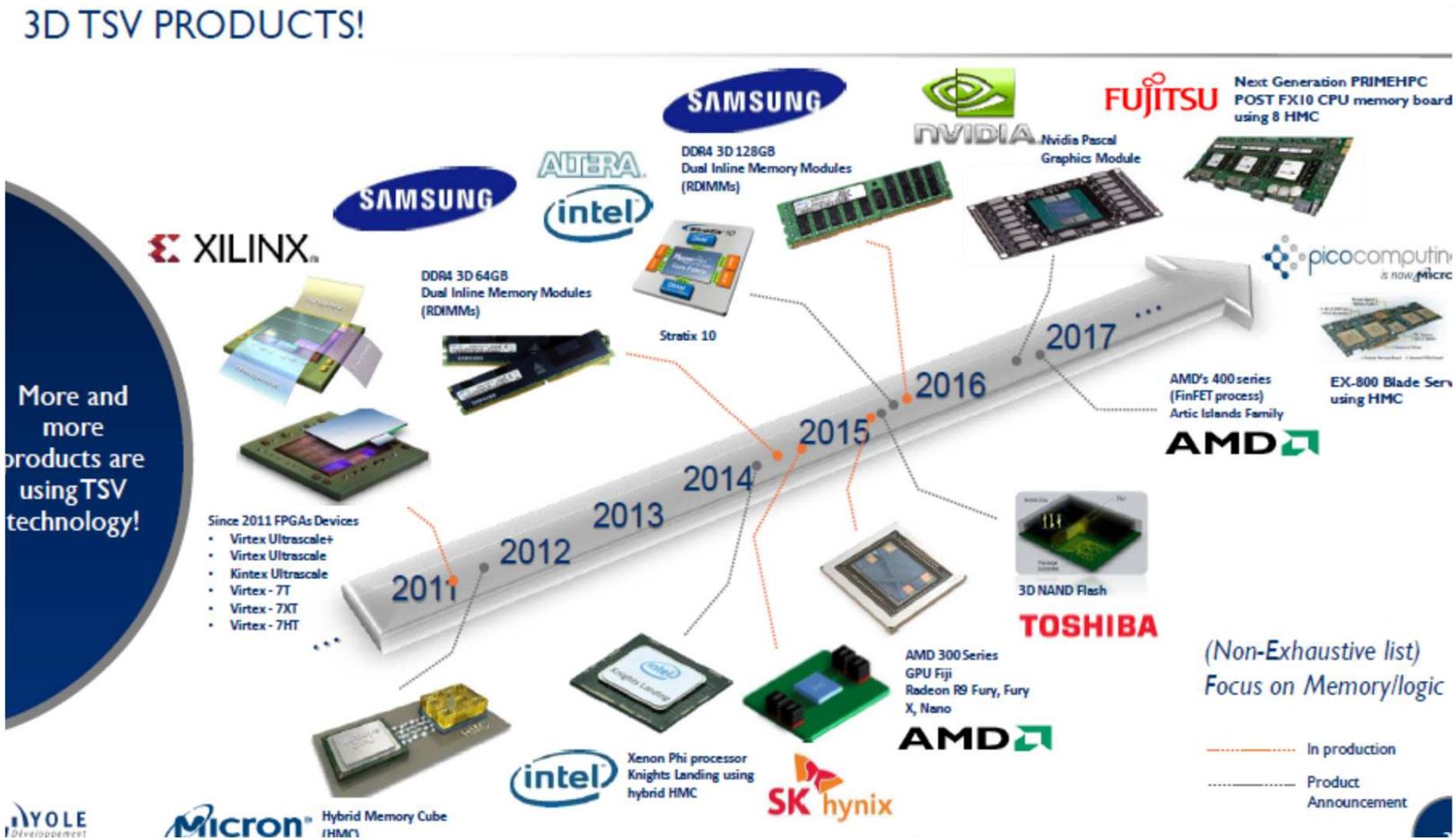
3D SEQUENTIAL INTEGRATION : OVERVIEW OF 65 NM ON 28 NM FDSOI MPW ARCHITECTURE AND DESIGN CONTRIBUTIONS

Sébastien THURIES, Olivier Billoint, Adam Makosiej, Pascal Vivet, Edith Beigné, Francois Andrieu, Claire Fenouillet-Beranger, Laurent Brunet, Perrine Batude, Didier Lattard, Mehdi Mouhdach, Sebastien Martinie, Joris Lacord, Gerald Cibrario, Maud Vinet, Fabien Clermidy

sebastien.thuries@cea.fr

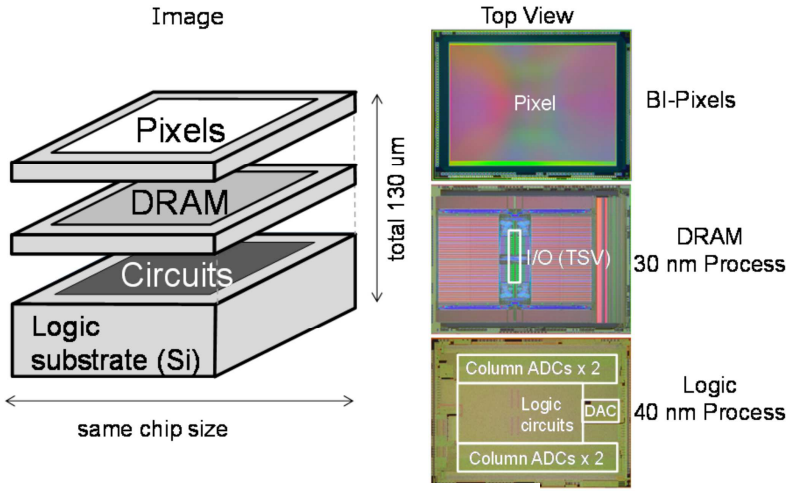
D43D Workshop – 2018 July 3rd

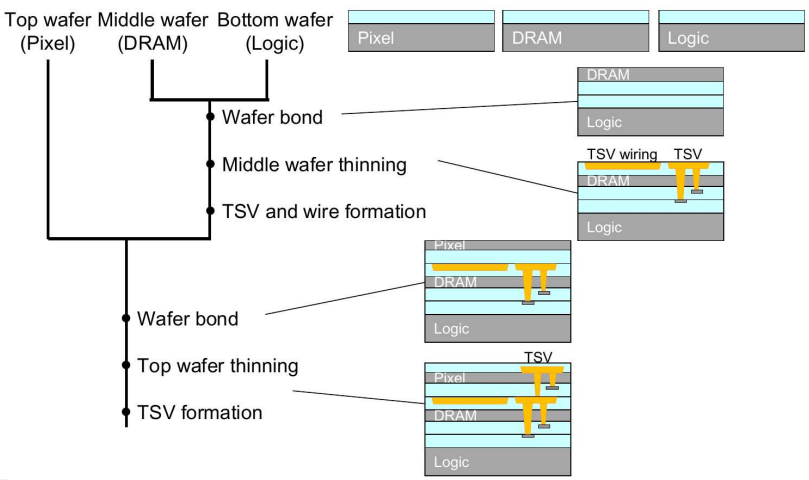
3D TSV IN PRODUCTION TODAY!

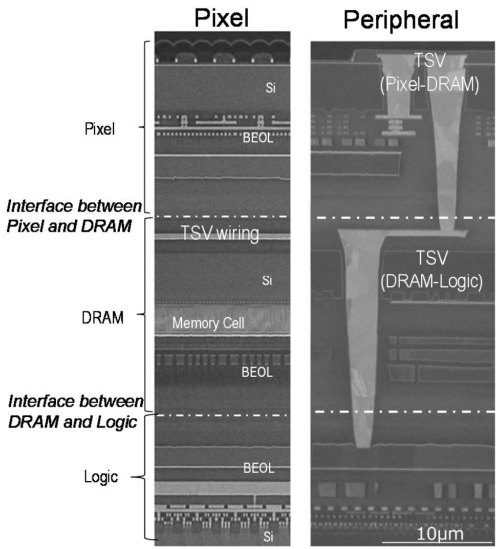


<u>C2W - Computing</u> : HBM, HMC Memory Cube, passive interposer
… Coarse grain 3D (2.5D) – TSV & Cu-Pillars – 20-10 µm pitch

3D TSV IN PRODUCTION TODAY!



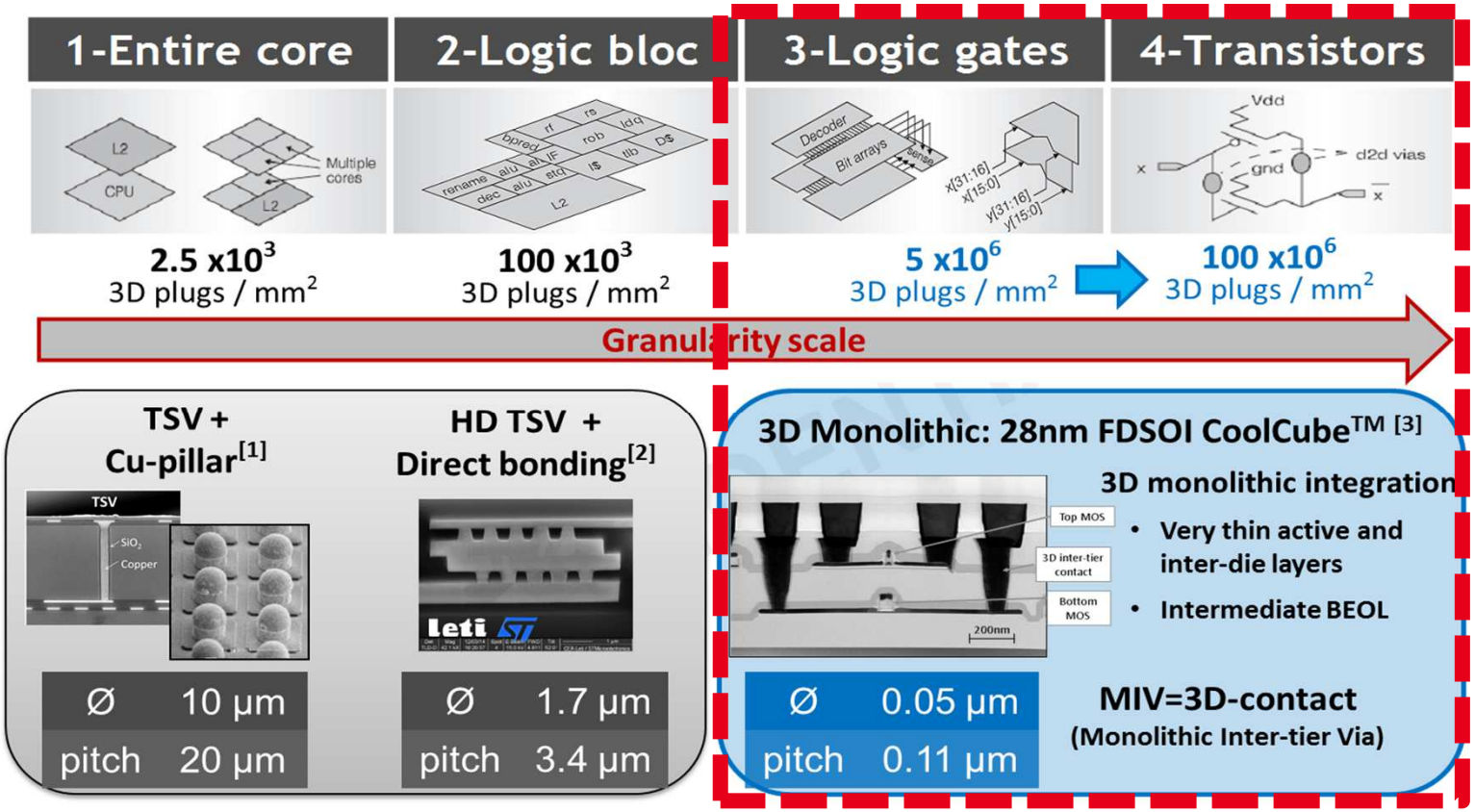




W2W - 3 Layers Stacked <u>Imagers</u>
19.3M pixels and a 1 Gbit DRAM
TSV 2.5 µm diameter - 6.3 µm pitch [1]
→ 3D Pitch scales down

[1] SONY, ISSCC 2017

3D TECHNOLOGIES PORTFOLIO



Pitch Scale

TSV & Cu-Pillar > 10 µm

7µm > D2W > 3 µm

5 µm > W2W < 1 µm

Nano Scale
3D contact

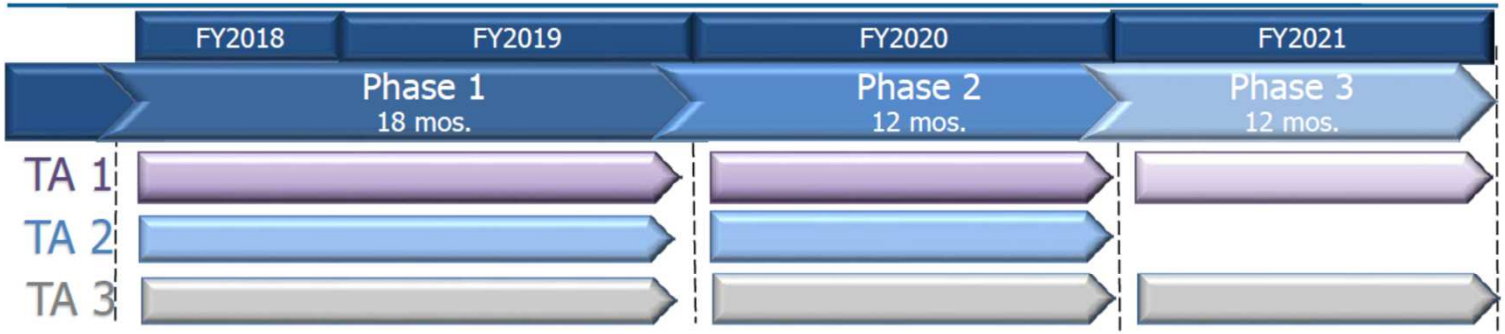
3D Sequential ==
3D Monolithic ==
CoolCube™ …
and 3DSoC in US…

150 nm > 3D Monolithic

3D SEQUENTIAL WORLDWIDE

Results coming soon

3DSoC Program Schedule



Phase 1 Outcomes
- Initial 3DSoC process defined
- PDK V0.5 defined
- 3DSoC technology benefits simulated
- First pass DEC fabricated and tested
- Initial 3DSoC EDA tools released

Phase 2 Outcomes
- 3DSoC process demonstrated
- PDK V1.0 released for design
- 3DSoC benefits demonstrated
- Final DEC design fabricated
- 3DSoC EDA tools released for targeted designs

Phase 3 Outcomes
- 3DSoC process used for external designs
- Final PDK released for design
- MPW runs successfully yielded
- 3DSoC EDA tools released for general designs

- TA-1: Developing the 3DSoC fabrication process
  - Establish unit processes and flow integration
  - Define the 3DSoC technology PDK
- TA-2: Designing and Implementing the DEC
  - Design 1st and 2nd pass DEC design
  - Foster use of the DEC to drive development and yield
- TA-3: Developing the 3DSoC EDA design flow
  - Develop EDA tools for 3DSoC compute/memory designs
  - Support tools for advanced 3DSoC designs

Metric	Goal
3DSoC Capability	> 50X 7nm 2D PaP
Hardware Accuracy	< 2% deviation from3DSoC technology targets
Yield	> 30% for full 3DSoC designs
EDA Tools	Successful use of EDA flow for a > 500M gate/4GB memory design

3D Seq. to challenge scaling

EDA Tools to upgrade

CEA-LETI 3D CIRCUITS ROADMAP

Computing in Memory Cube & Smart Sensors

Design Early Exploration

1st MPW Q2 2017
PDKit v1,
SRAM test chip
Early EDA Tools

2nd MPW Q1 2019
PDKit v2,
SoC test chip,
Signoff EDA Tools

Heterogeneous & Configurable computing
Non Volatile Memory based Computing Cube

3D Seq.

50 nm Pitch

3D early PDKIT, Thermal study
Partitioning evaluation (CoC, CoB, NoP)
Device silicon demo.

Cortical Column

Bio-inspired 3D archi
Heterogeneous computing
3DHD and 3D Seq.

Smart Imager

4 layer ISP
Analog & computing
HB - CuCu 1 µm

Imager & Neuro Applications

Smart Imager

2 layer ISP
SIMD array
130nm, CuCu 7µm

Neural Network

2 layer Neural Network
Neuron & Memory array
130nm, CuCu 7µm

3D HD

10-1 µm Pitch

Photonic Interposer

Optical NoC
96 cores prototype
FDSOI 28nm + µbump 40µm

Photonic System

3D TSV & Photonic convergence
Photonic Memory-interface

Passive & Active Interposer

Logic-on-Logic

Manycore

Homogeneous & Heterogeneous Manycore

Manycore & Computing Roadmap

2.5D/3D

20-10 µm Pitch

Async robust links
DFT & Fault Tol.
CMOS 65nm
µbump 40µm pitch

96 cores (32bit MIPS)
cache-coherent memory
FDSOI 28nm + CMOS 65nm
µbump 20µm pitch

High-end server compute node
Heterogeneous chiplets
FDSOI 28nm + CMOS 65nm
µbump 20 µm pitch

2015 2016 2017 2018 2019 2020

AGENDA

28 nm FDSOI 3D Sequential process

PDKit content & evolution

Multi Layers SRAM - 1st Silicon Testchip (MPW#1)

Digital Design Methodologies

Architecture & Design Perspectives – 2nd Silicon Testchip (MPW#2)

Conclusion

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28 nm FDSOI 3D Sequential process

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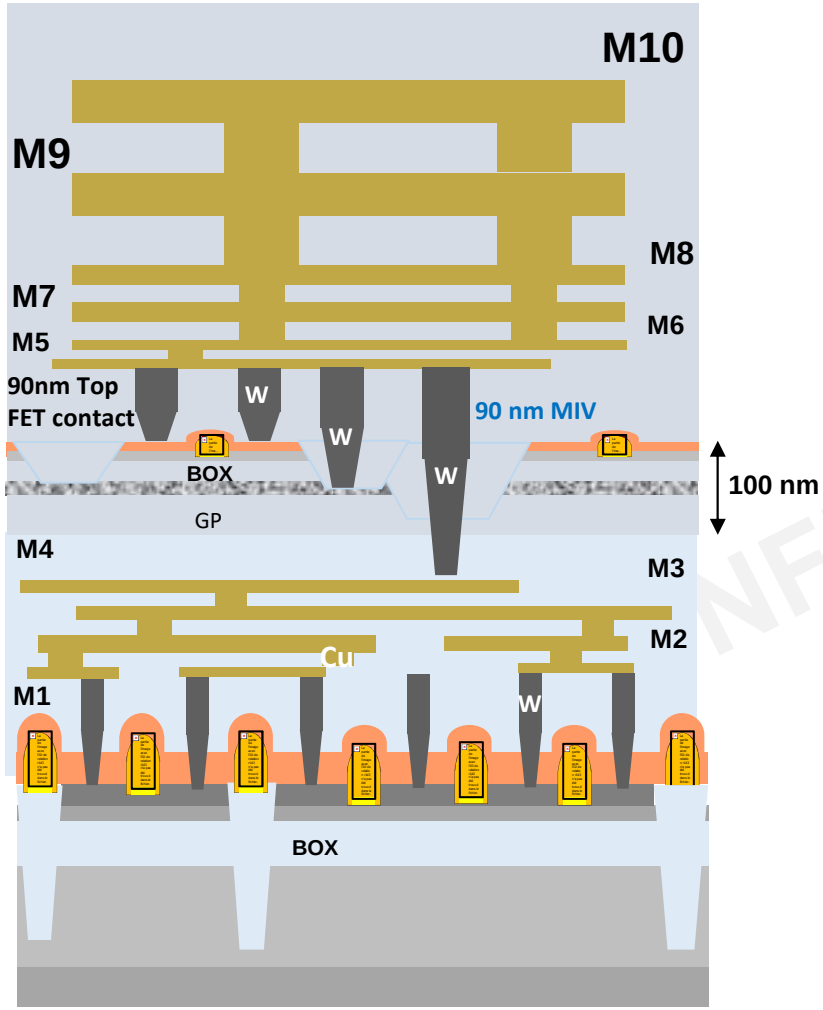
3D SEQUENTIAL 28 NM FDSOI BASED MPW PROCESS



Top BEOL M5 to M10 (+AluCap)

28nm pitch processed back to foundry for BEOL finishing

Top tier (Cold Process):

28nm like density 65nm like **Processed at leti**

→ Via4 becomes Monolithic Inter-tier Via (MIV)

Bottom tier:

FDSOI 28nm foundry baseline process

4 metal layers in Copper

without any modification

AGENDA

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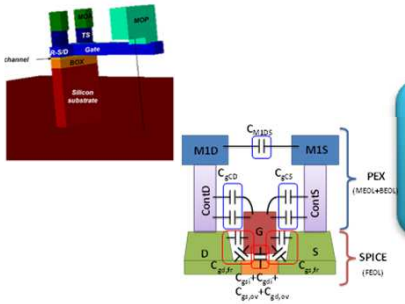
FULL CUSTOM DESIGN FLOW & CAD TOOLS

cadence

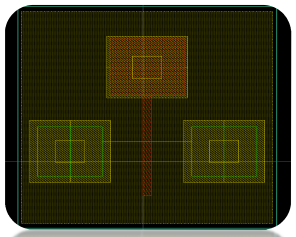
→ Parasitic extraction (PEX)
→ RC Simulation



Technology

Post-Layout Simulation

Layout



Parameterized Cells
(MOS Pcells)

PDF

DRM, Reference manuals

Added on PDKit v2

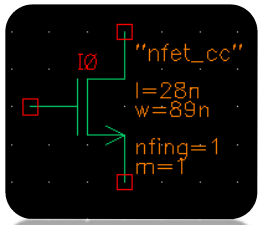
PDKit v1

Mentor Graphics

Design Library & Simulation

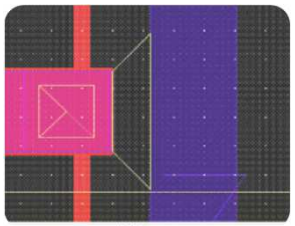
Verification (3D DRC/LVS)

synopsys



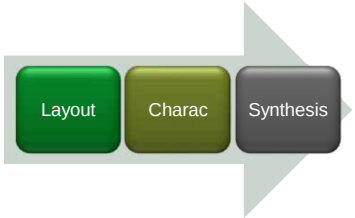
Top Devices Library:
→ N/P FET (VT)
→ Spice Modeling
(LETI UTSOI model)

Mentor Graphics

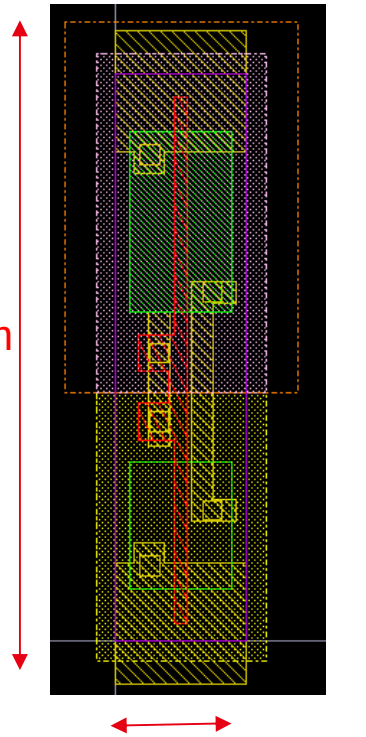


→ Design Rules Checking
→ Devices & connectivity extraction

DIGITAL DESIGN FLOW & CAD TOOLS



- **Digital flow & CAD tools:**
  - **Synthesis** flow: Synopsys DC Compiler
    - **LIB & DB** files (function/timing):
    - → cell characterization based on spice simulation with layout (PEX)
  - **PnR** flow: Cadence Innovus
    - **LEF techno**: techno and routing information **including MIV rules**
    - **QRC** techfile: 3D stacking definition, RC data (generated from ICT file)
    - **LEF** files: SC layout abstract view
- **Standard cells library:**
  - Preliminary Design Platform for top level:
    - A set of ~40 standard cells for synthesis and P&R
    - Layout based on 65nm design rules (layout migration)
  - Cell on Cell approach:
    - Bottom level: standard 28FD DP from STm
    - Top level: preliminary 28CC DP from Leti – 65 nm footprint



Added on PDKit v2

Next Step : IO Pads for MPW#2

AGENDA

28 nm FDSOI 3D Sequential process

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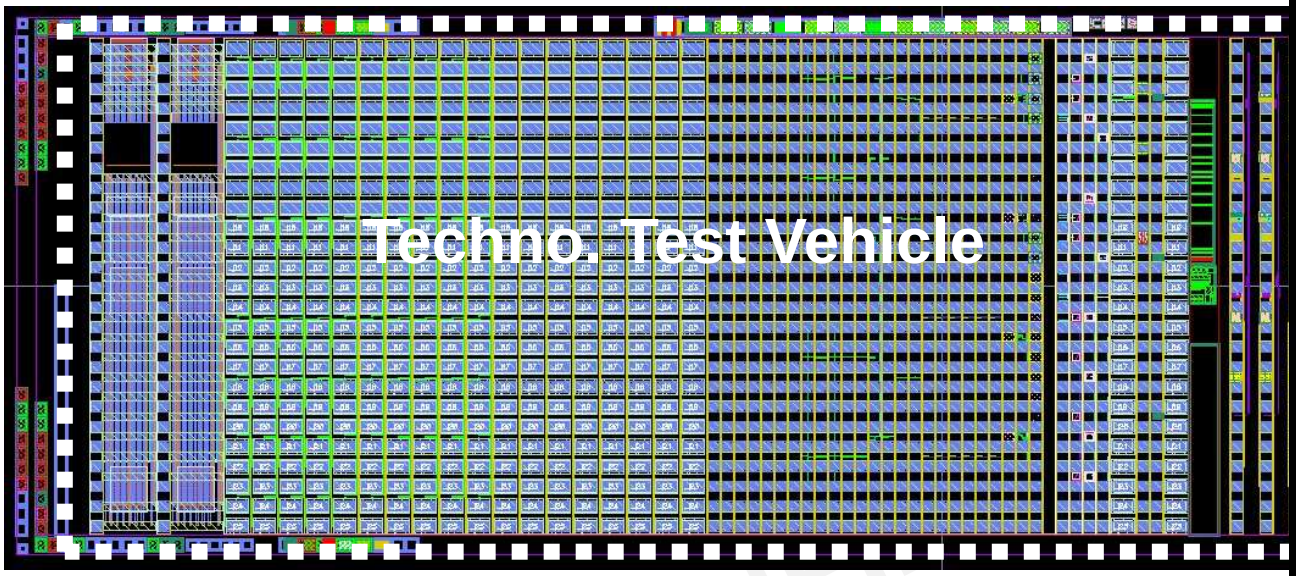
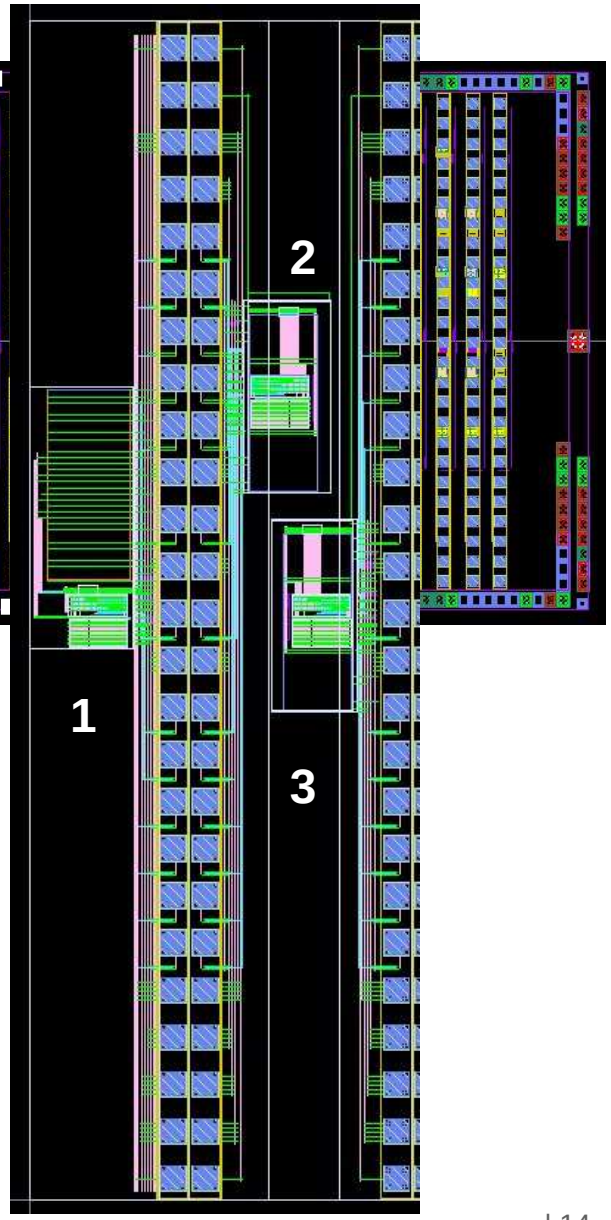
MPW#1 GDS (30 MM²) - ZOOM ON 2D & 3D SRAM





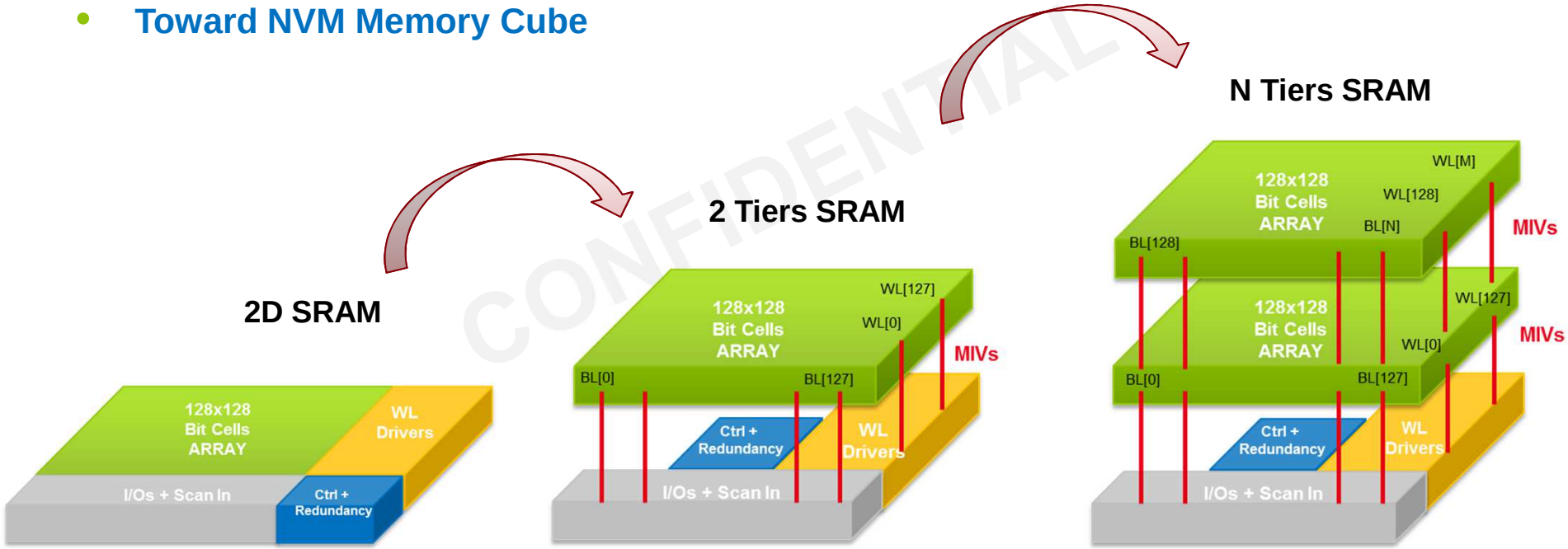
- **Scribe 1**: 2D reference 16kb SRAM with 32 word redundancy block (3D design rules used)

- **Scribe 2**: 3D 16kb SRAM with 32 word redundancy block with 33 MIVs :
  - Standard design with single 128x128 SRAM array on top layer

- **Scribe 3**: 3D 16kb SRAM with 32 word redundancy block with single 3D vias
  - Snake path between top and bottom layers to emulate 33 stacked arrays on top of bottom layer

MULTI TIERS SRAM CONCEPT & ARCHITECTURE

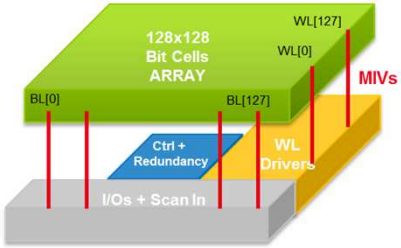
- **Objective : Multi Tiers embedded Memory → Multiple Array on Periphery Partitioning :**
  - Bottom level: all decoding logic, drivers, I/Os and redundancy
  - Top level is a 128x128 SRAM array connected thanks to MIVs
  - **Toward NVM Memory Cube**



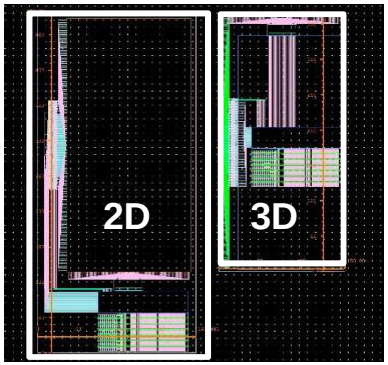
→ **~2x reduced footprint target**
→ **Reduced BEOL layers (#4) on Top process**

→ **~Nx reduced foorptint**
→ **Top mask set reuse**

2 TIERS SRAM MPW#1 TAPED OUT



- **Objective:**
  - first tape out at IP level (building block)
- **Partitioning:**
  - Bottom die for IO, periphery & redundancy
  - Top die : bit cell array 128x128.



- **Early Results**
  - 128x128x6T = 98304 Transistors on top process
  - 2D Area : 193um x 478um= 92475um2 (same design rules than 3D)
  - 3D Area : 153um x 360um= 55421um2
  - Done on PDKit v1 → Perf. Power simulation on going with PDKit v2

1. **40% Footprint reduction**
2. **~100000 Transistors on Top (Cold) Process**

AGENDA

28 nm FDSOI 3D Sequential process

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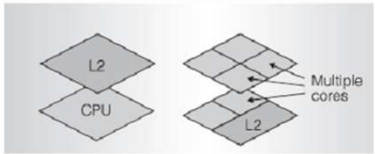
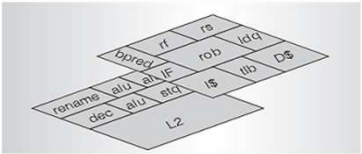
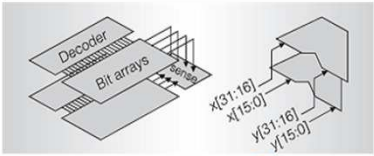
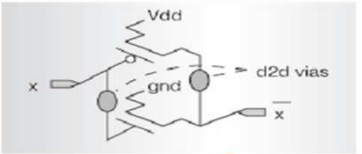
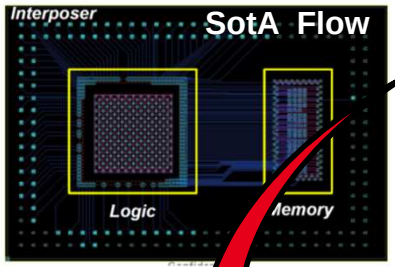
3D SEQUENTIAL : DESIGN CHALLENGE

1-Entire core	2-Logic bloc	3-Logic gates	4-Transistors
			
2.5×10^3 3D plugs / mm^2	100×10^3 3D plugs / mm^2	5×10^6 3D plugs / mm^2	100×10^6 3D plugs / mm^2

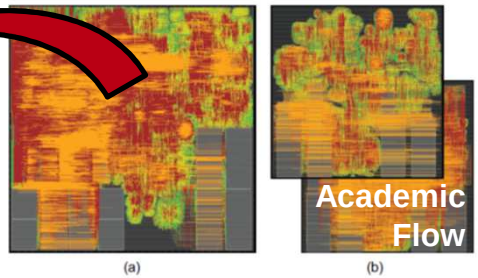
Granularity scale

3D Packaging



TSV & Cu-Pillar > 10 µm

3D Design



Pitch Scale

Georgia Tech DARPA leti ceatech ARM GLOBAL FOUNDRIES

Design flow needs to be upgraded for optimal PPAC

HD 3D fine pitch (> 5 µm) Hybrid Bonding reused Design Methodology

Nano Scale 3D contact

150 nm > 3D Monolithic

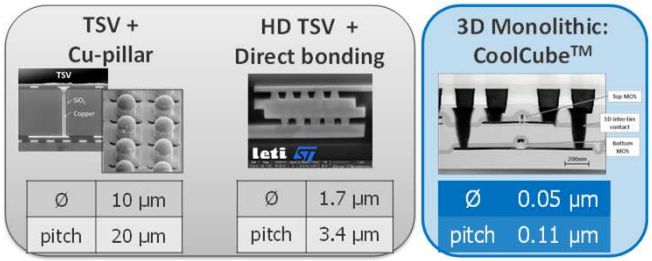
3D SEQUENTIAL : DESIGN CHALLENGE

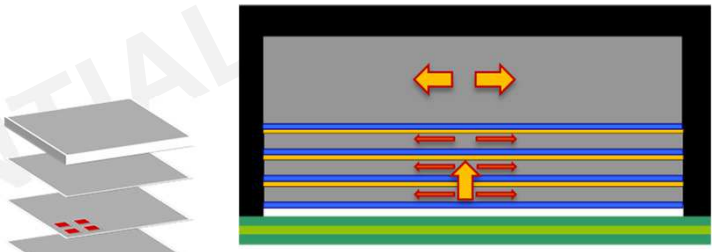
- **CEA-Leti has developed a signoff Place and Route methodology to manage 2 or more active layers and insert MIVs automatically like classical vias in EDA vendors Tool (CADENCE Foundation Flow based)**

- **Confidential activity but can be discussed under NDA agreement**

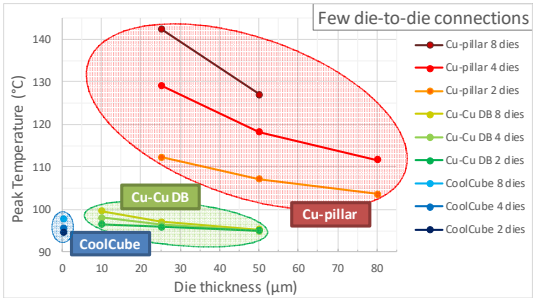
3D TECHNOLOGIES THERMAL COMPARISON[1]

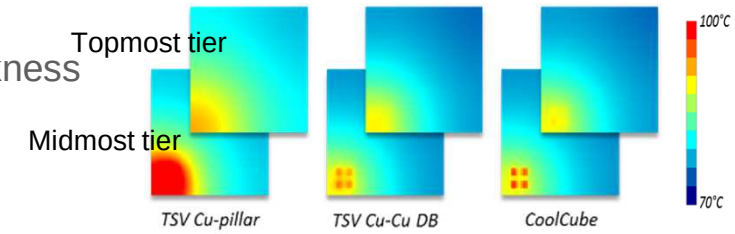
- **Objective**
  - Compare thermal performances of different 3D technologies
    - TSV + µ-bumps
    - Hybrid Bonding
    - Monolithic 3D (CoolCubeTM)
- **Method**
  - Define a Set of Experiments
    - Different technology parameters (#layers, 3D interco pitch, materials, etc)
    - Different power scenerio
    - Different thermal dissipation, etc
  - Thermal model using SAHARA tool
  - + scripting for automation
- **Results**
  - Better thermal coupling for Hybrid Bonding & CoolCube
  - Reduced hot spot effect
  - Strong sensitivity to interconnect density, adn die thickness





Hot spot dissipation





[1] C. Santos et. al. , 3DIC'16

AGENDA

28 nm FDSOI 3D Sequential process

PDKit content & evolution

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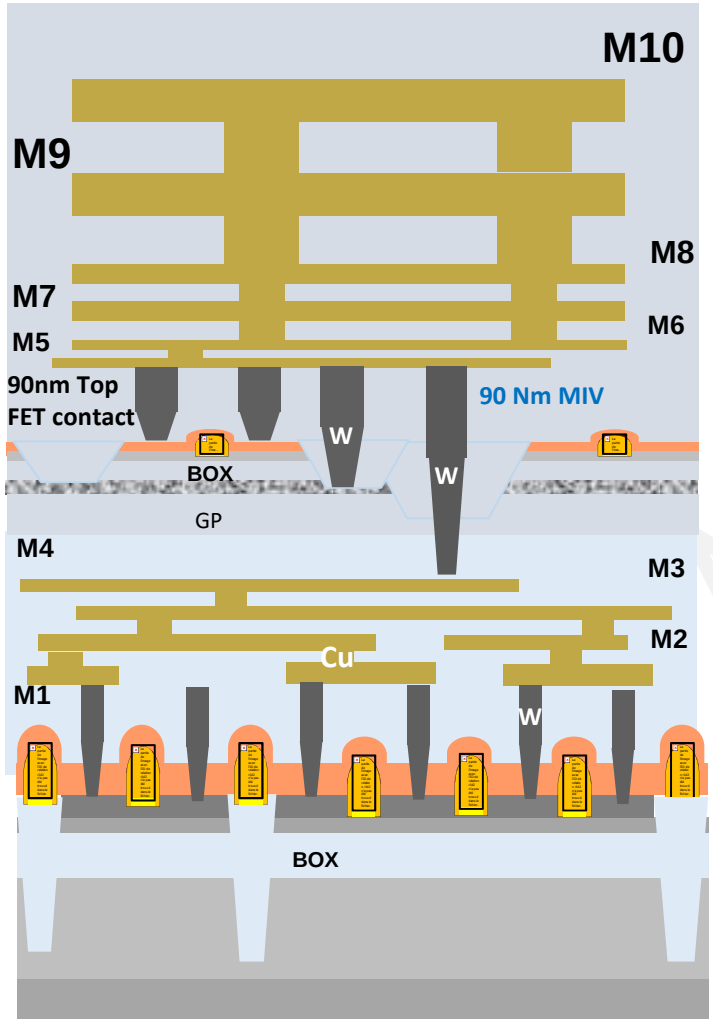
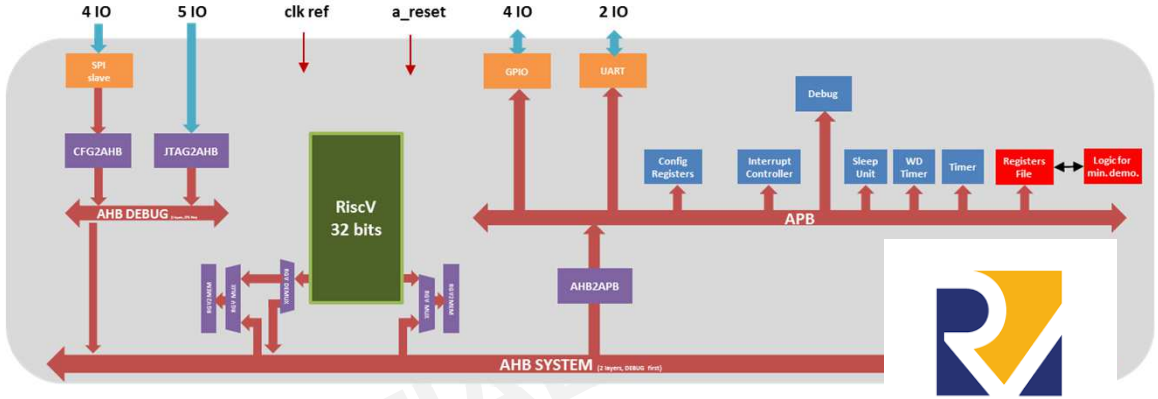
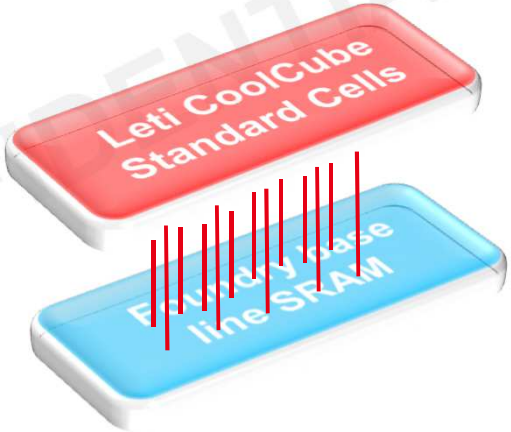
Conclusion

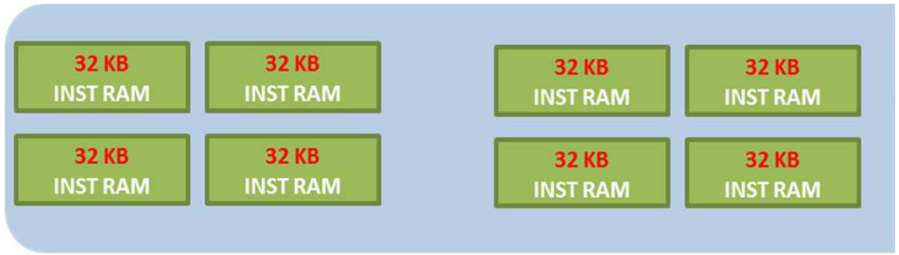
2ND SILICON TESTCHIP (MPW#2) – 32 BITS RISCV SOC TARGET







Silicon Demo. at SoC level complexity



AGENDA

28 nm FDSOI 3D Sequential process

PDKit content & evolution

Multi Layers SRAM - 1st Silicon Testchip (MPW#1)

Digital Design Methodologies

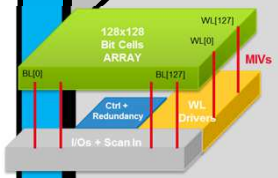
Architecture & Design Perspectives – 2nd Silicon Testchip (MPW#2)

Conclusion

CONCLUSION & PERSPECTIVES

3D Seq. Architectures breakthrough

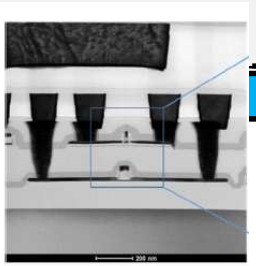
- Ultra Dense in **Memory Computing Cube** (**NVM & M3D**)
- Multi Layers stacked BSI (**Smart Imagers**)
- **High memory BW DNN** Archi.
- **Heterogeneity** & **Configurability**



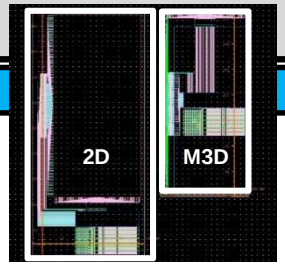
- 2 Layers Memory Cube
- Logic on Memory
- DNN Architectures
- Smart Sensor Array

- ➢ **BeoL (ReRAM) NVM Memory**
- ➢ **BeoL top beg. with M1**

- Silicon demo at device level
- Design methodology based on 2D tools ready
- Thermal & Cost are good
- Early PDKit

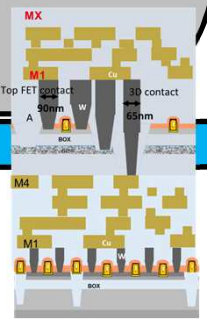


- IP Level Silicon demo. & measurements
- Advanced Device Maturity
- Prelim. Design Platform



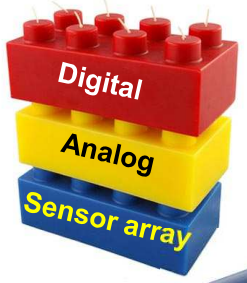
we are here

- SoC Level Silicon demo.
- Advanced Techno. maturity
- Full Design Platform to plug on customer technology targeted

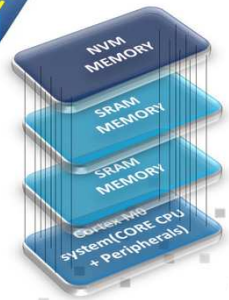


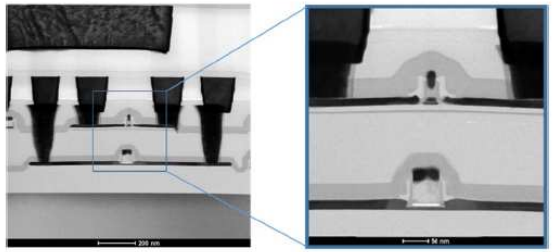
Silicon Readiness

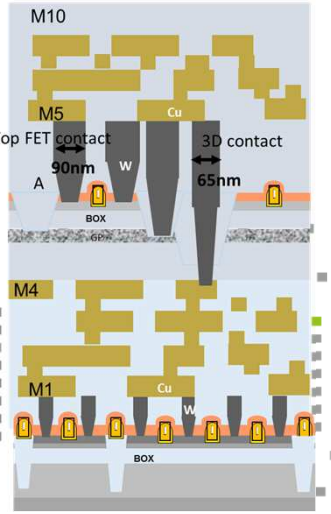
Thank you for your attention

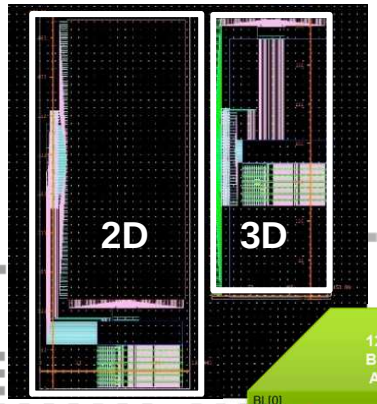


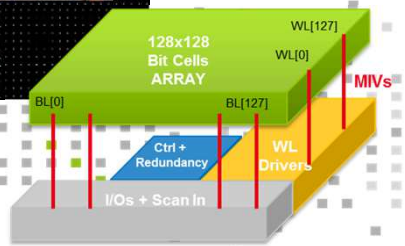
SinC
System in Cube











3D SEQUENTIAL INTEGRATION : OVERVIEW OF 65 NM ON 28 NM FDSOI MPW ARCHITECTURE AND DESIGN CONTRIBUTIONS

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