

CAD Flow methodologies for 3D Hybrid sub-systems

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STMicroelectronics



Who We Are

- A global semiconductor leader
- 2017 revenues of **\$8.35B** with year-on-year growth of **19.7%**
- Listed: NYSE, Euronext Paris and Borsa Italiana, Milan

- Research & Development
- Main Sales & Marketing
- Front-End
- Back-End

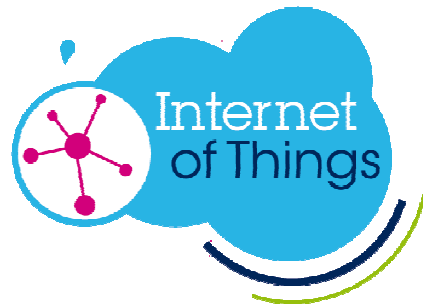


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- Approximately **45,500** employees worldwide
- Approximately **7,400** people working in R&D
- **11** manufacturing sites
- Over **80** sales & marketing offices

Application Strategic Focus

The leading provider of products and solutions for Smart Driving and the Internet of Things



Smart Things



Smart Home & City



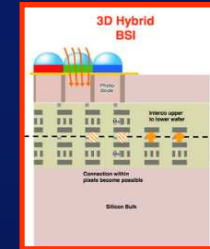
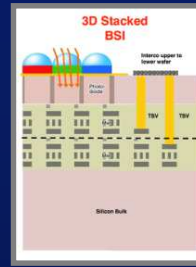
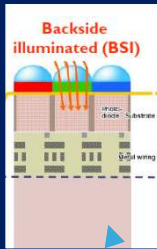
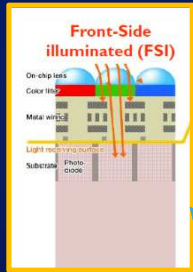
Smart Industry



Smart Driving



Technologies for Imager sensors

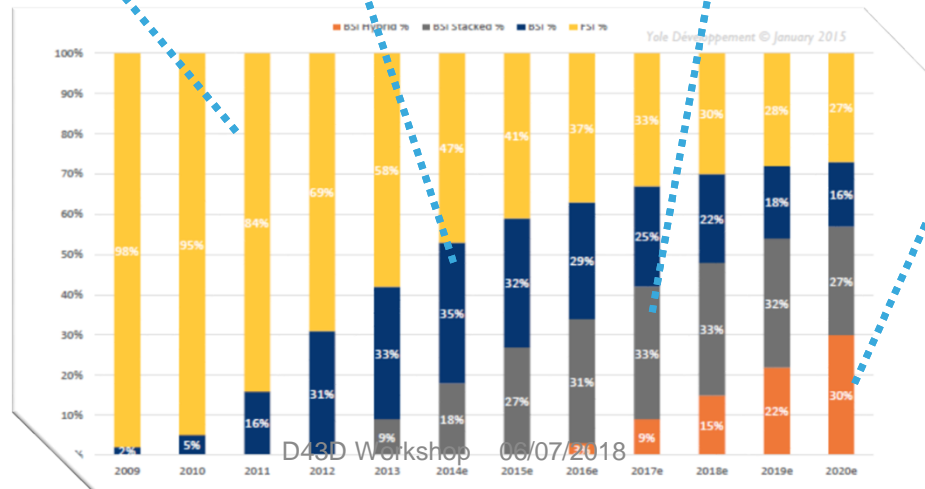


- FSI Technology :**
- Low fill factor
 - Limited for pixel size
 - Low cost

- BSI Technology :**
- Better fill factor
 - More expensive

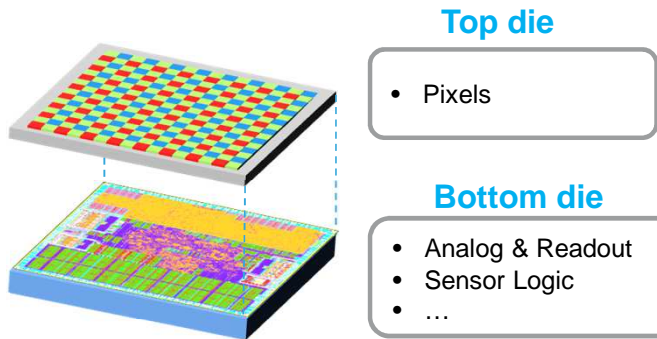
- 3D Stacked BSI :**
- Better integration
 - Even more expensive due to TSV

- 3D Hybrid :**
- Best In Class for integration
 - Less expensive than TSV
 - Direct pixel capability

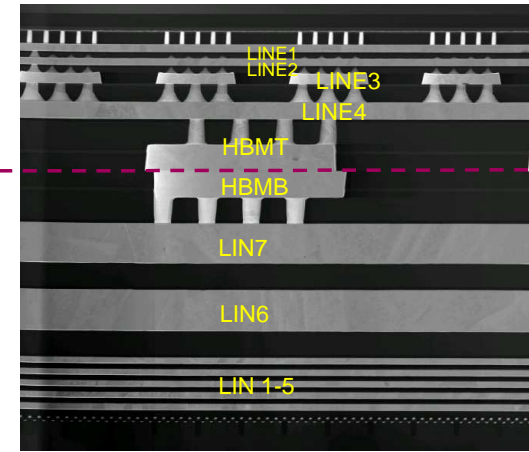
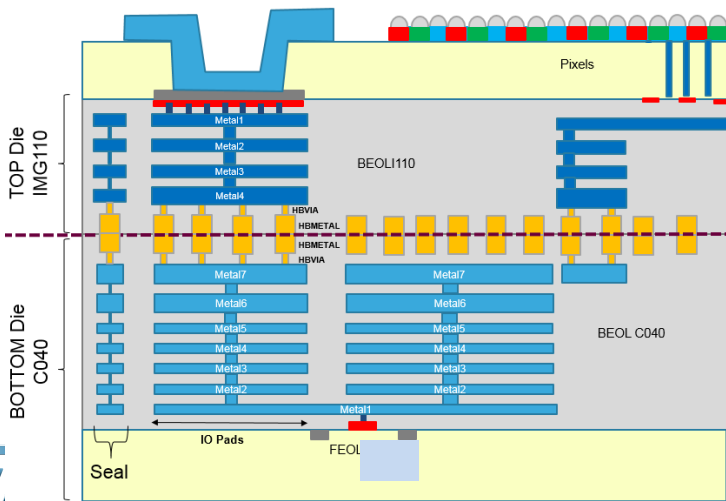


Market trends

Hybrid Bonding methodology



- No glue but **hybrid** molecular bonding
 - Direct SiO₂/SiO₂ bonding
 - Like in non-3D Back-Side Imager (BSI)
 - silanol SiOH-SiOH then siloxane Si-O-Si after anneal
 - Copper bonding
 - At 3D-via locations
 - grain growth/migration by anneal



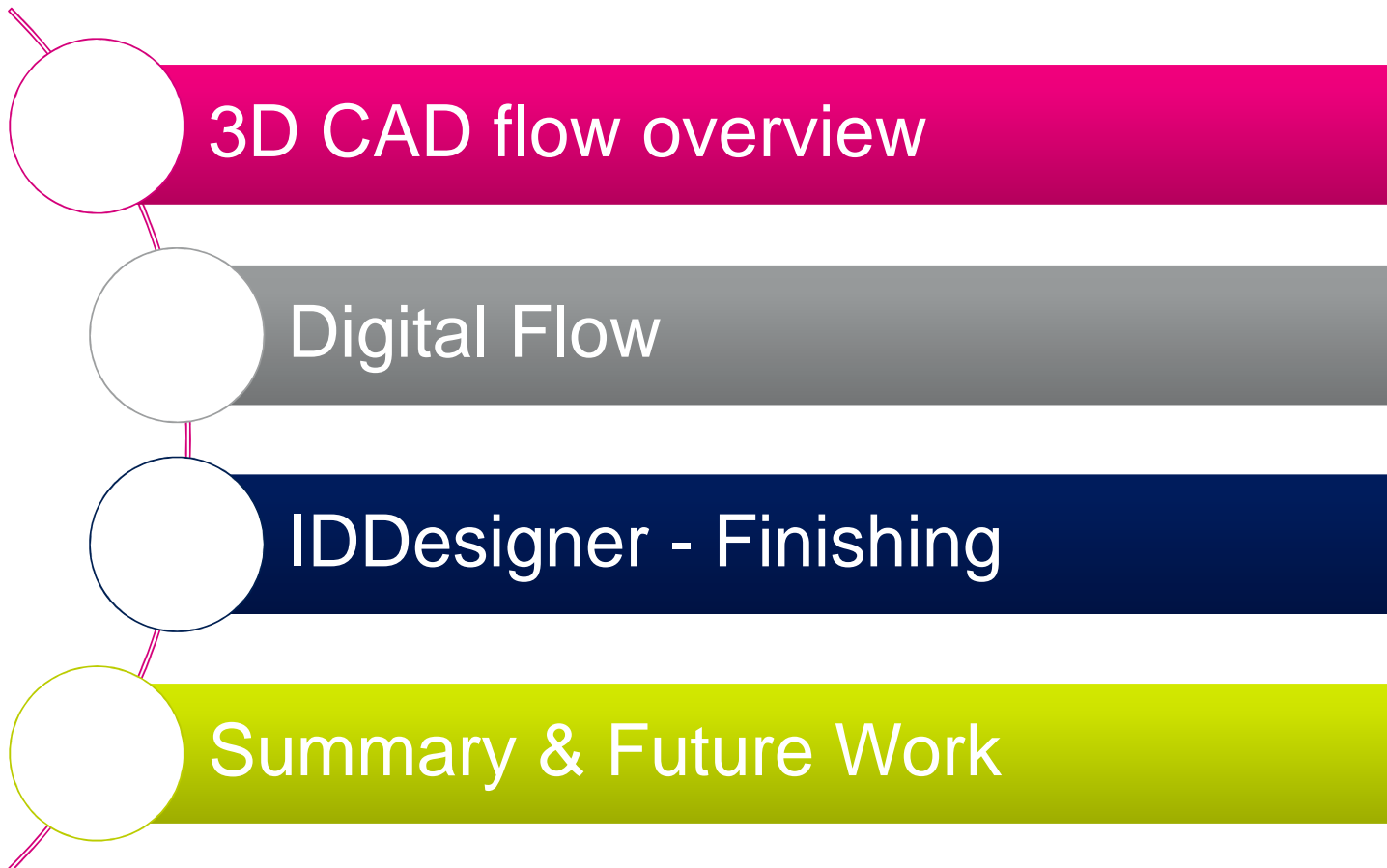
3D CAD flow Challenge

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- Complex co-design environment
- 3D Hybrid bonding technology in concurrent engineering (Technology/Design/CAD)
- 2D CAD tools

- Secure 3D design tapeout
- Provide flexible flow, in line with existing solution
- Mix technologies / Mix methodologies analog - digital
- 3D Verification

Agenda 7

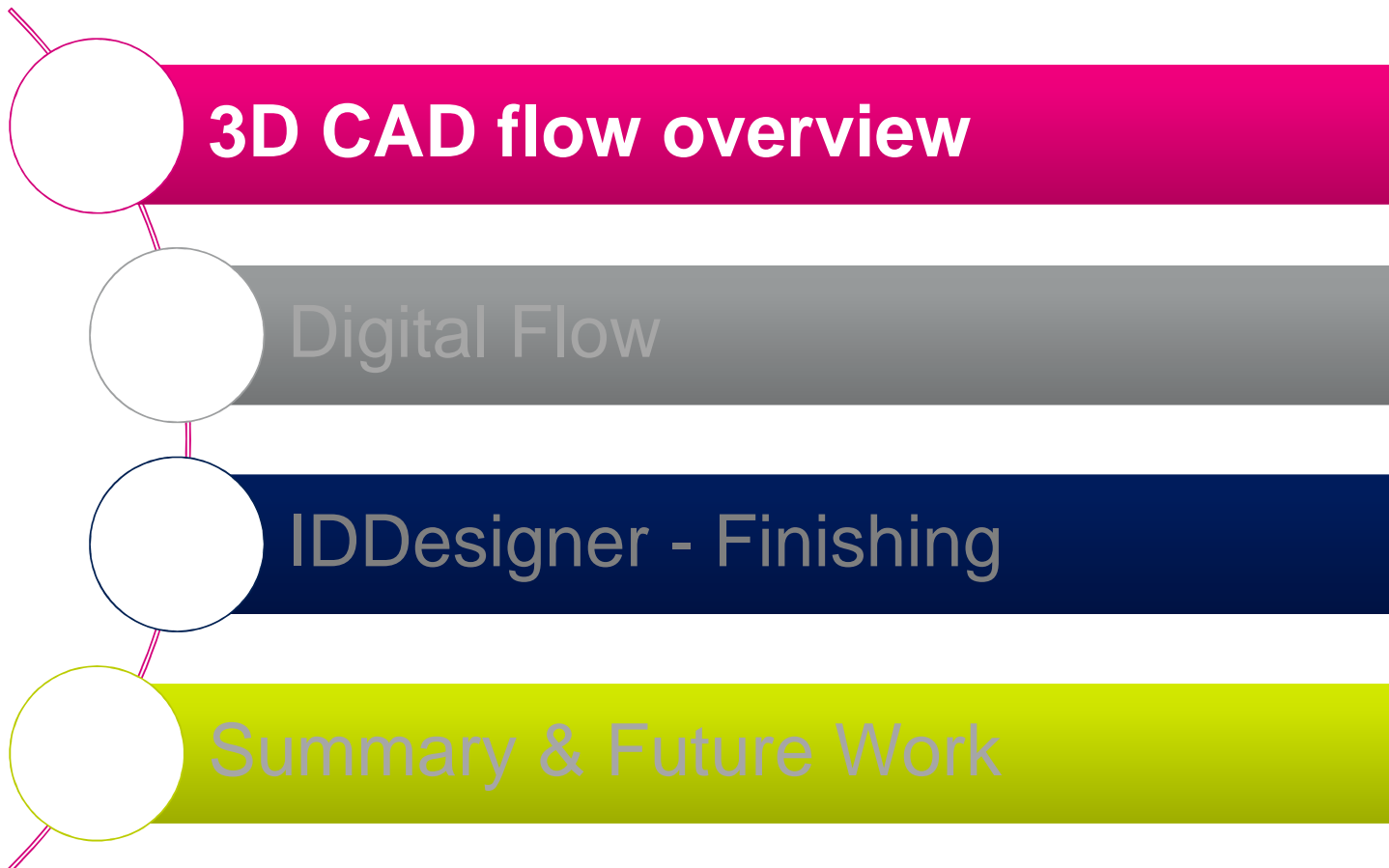


3D CAD flow overview

Digital Flow

IDDesigner - Finishing

Summary & Future Work



3D CAD flow overview

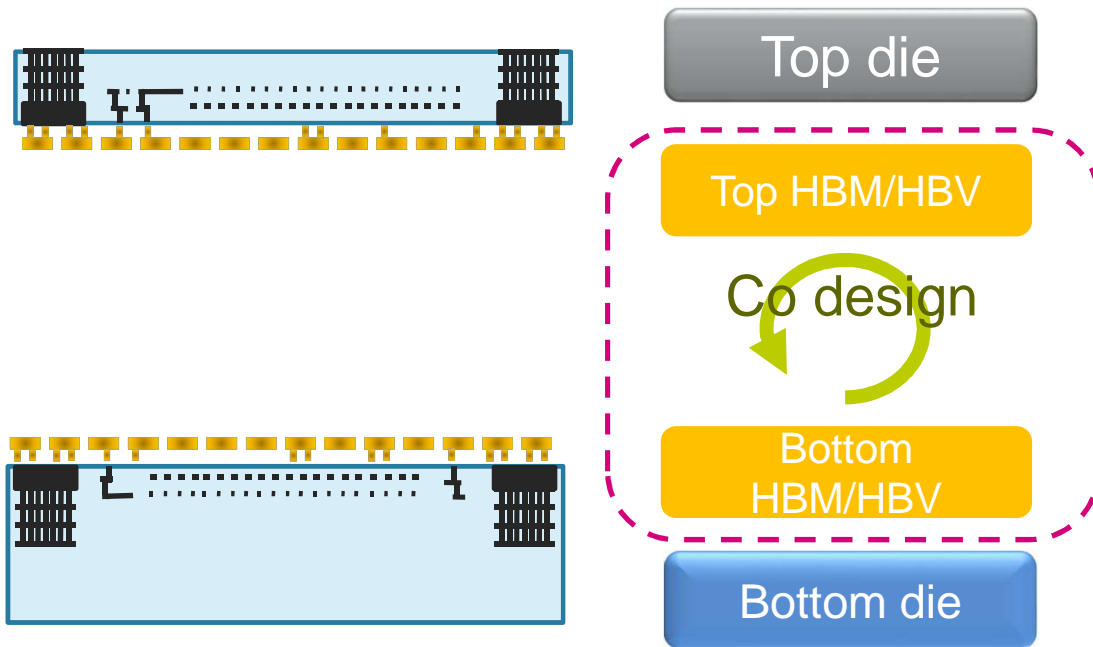
Digital Flow

IDDesigner - Finishing

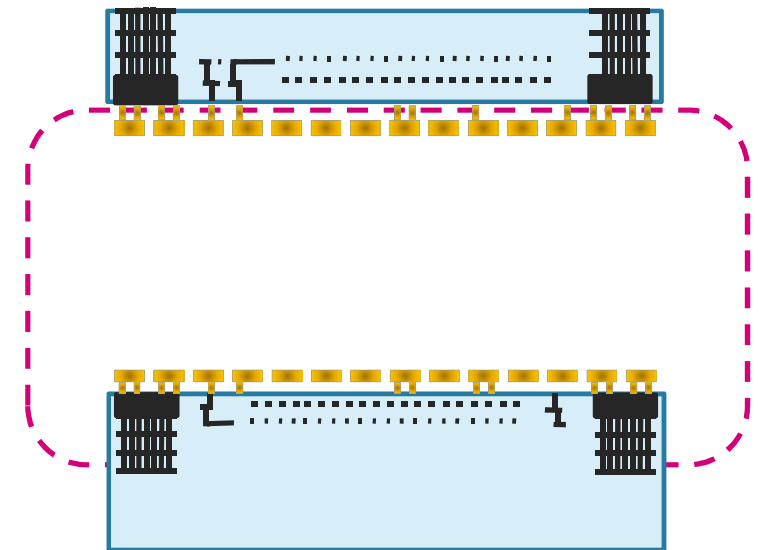
Summary & Future Work

3D hybrid CAD needs

3D Design solution

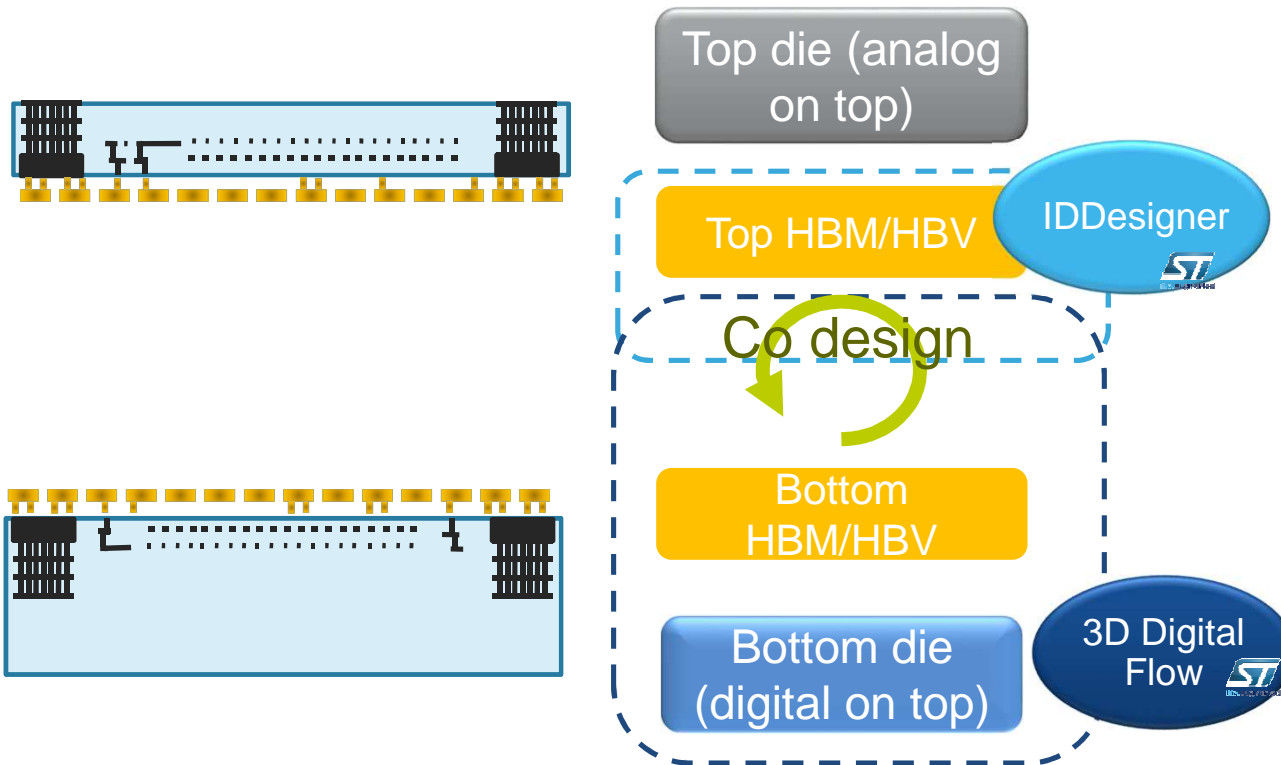


3D VERIFICATION

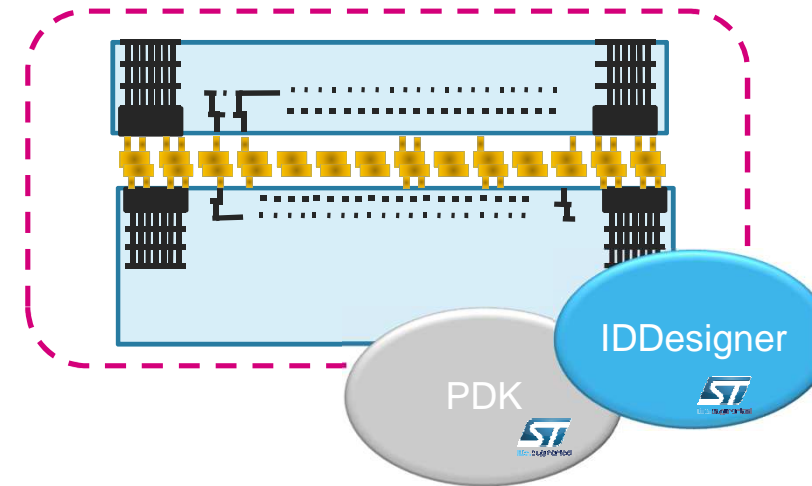


3D hybrid CAD overview

3D Design solution



3D VERIFICATION



ST 3D CAD flow offer

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IDDesigner

- 3D hybrid Finishing step for analog or digital design
- 3D Verification flow
- Flexible HBVia generation
- Support mixed technologies
- But ...
 - No co-design

3D Digital Flow

- Same product to address 3D, IO Ring implementation and Place&Route
- Digital on top design
- Allow optimization of HBM/HBV array along with floorplanning and IORing
- Co-design relying on standard exchange format
- But...
 - Some capacity limitation due to the millions of die to die interconnections



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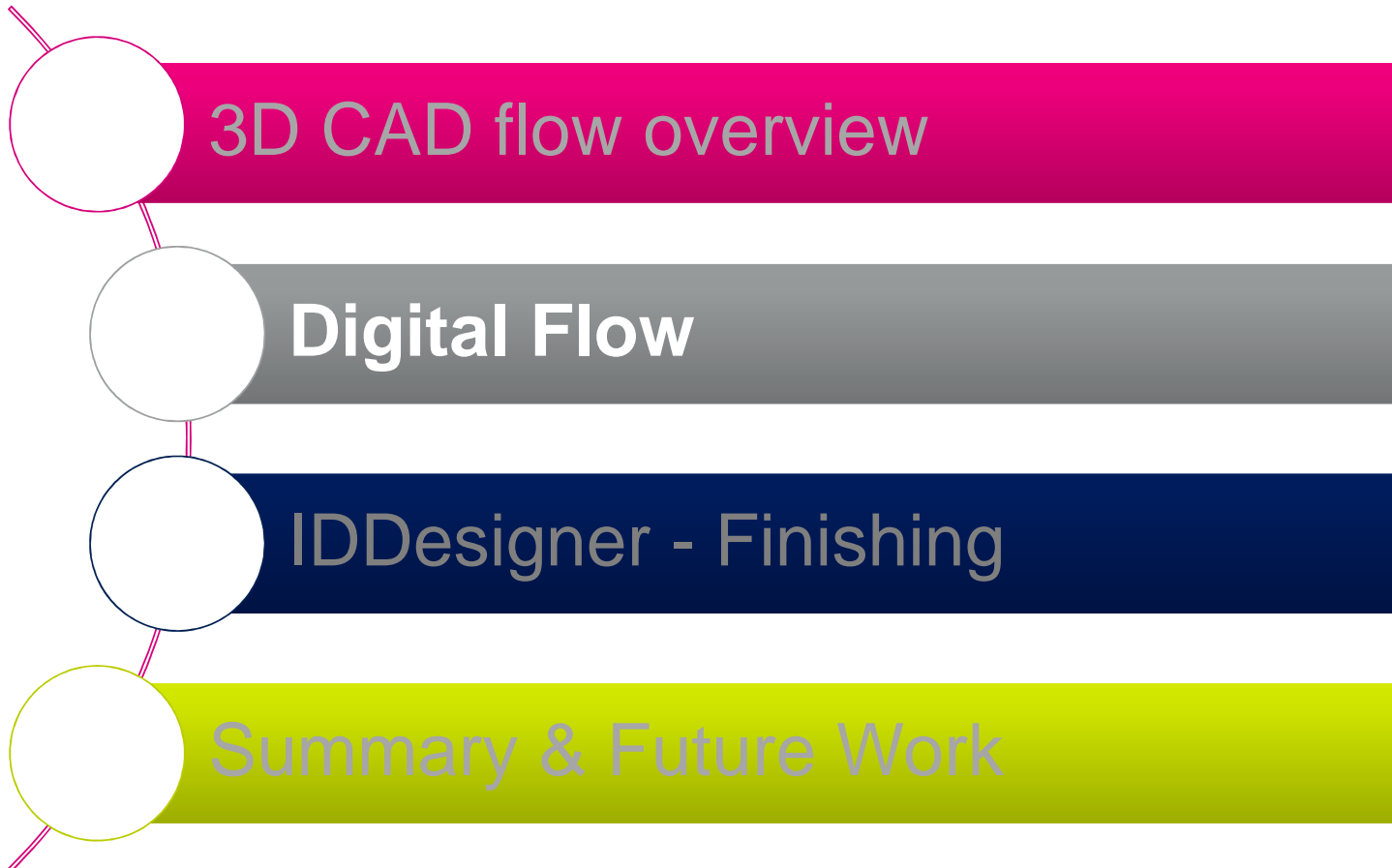
Tool: calibre



Tool: innovus 

D43D Workshop 06/07/2018

ST Confidential

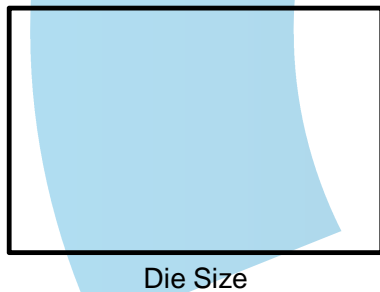
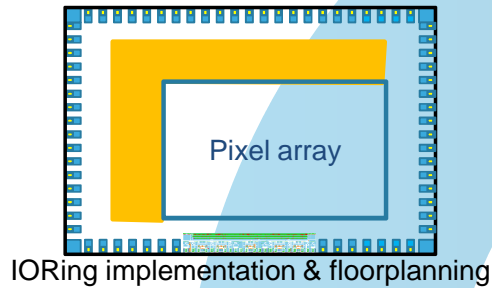


3D Digital Flow Methodology

BOTTOM Die
(digital on top)

IMG Top die drives:

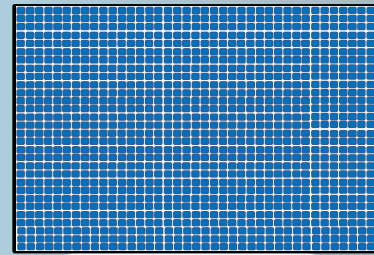
- die size
- IO pitch (package constraint)
- Pixel pitch



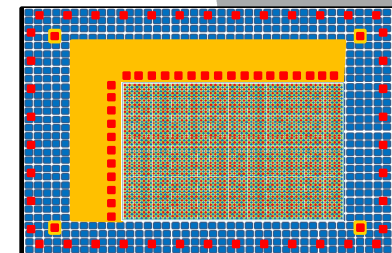
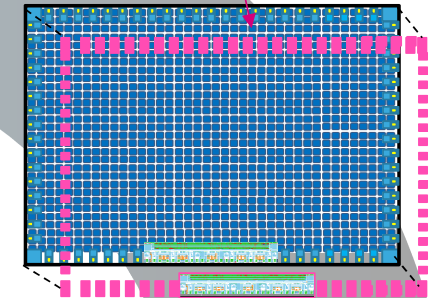
cadence
innovus

3D Digital Flow

Block	Area	Perimeter	IOs	IOs/IO Pitch	IOs/IO Pitch	IOs/IO Pitch	IOs/IO Pitch	IOs/IO Pitch	IOs/IO Pitch
Pixel Array	10000	4000	1000	1000	1000	1000	1000	1000	1000
IO Ring	1000	4000	1000	1000	1000	1000	1000	1000	1000
Die	11000	4000	1000	1000	1000	1000	1000	1000	1000

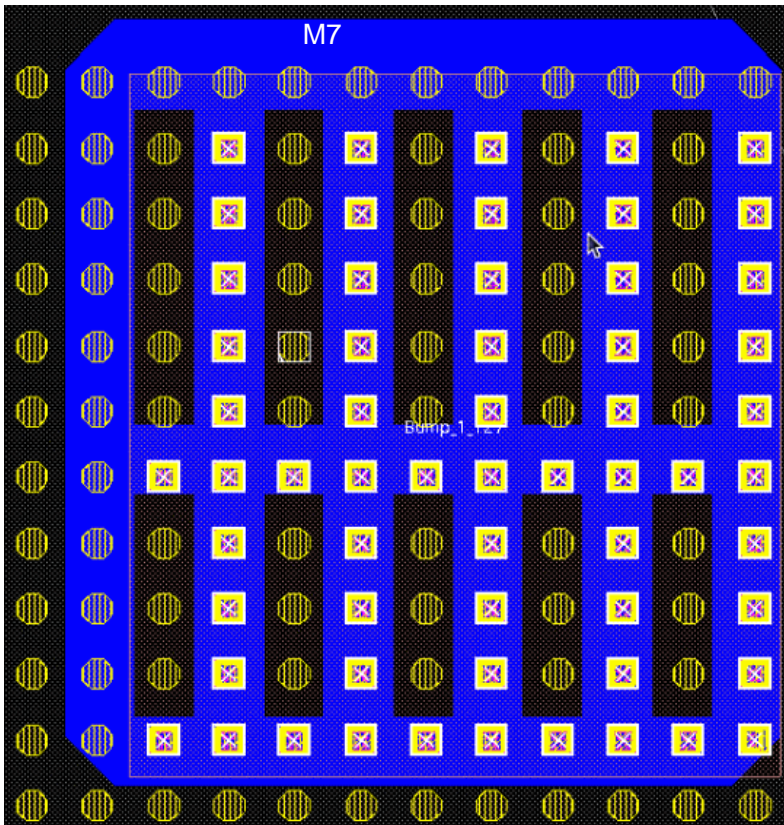


"BASIC_PAD",
To emulate IMG
IO placement
(ghost view)



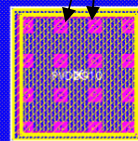
BOTTOM Die
(digital on top)

HBVIA Creation



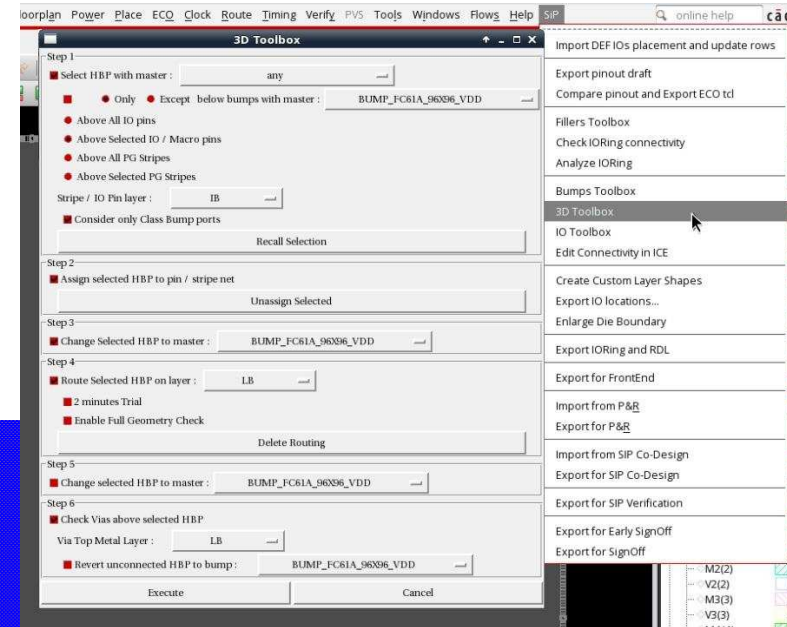
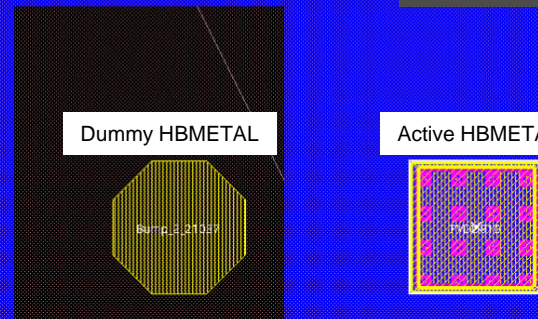
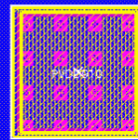
HBVIA

Several hundreds of
HBVIA per IO



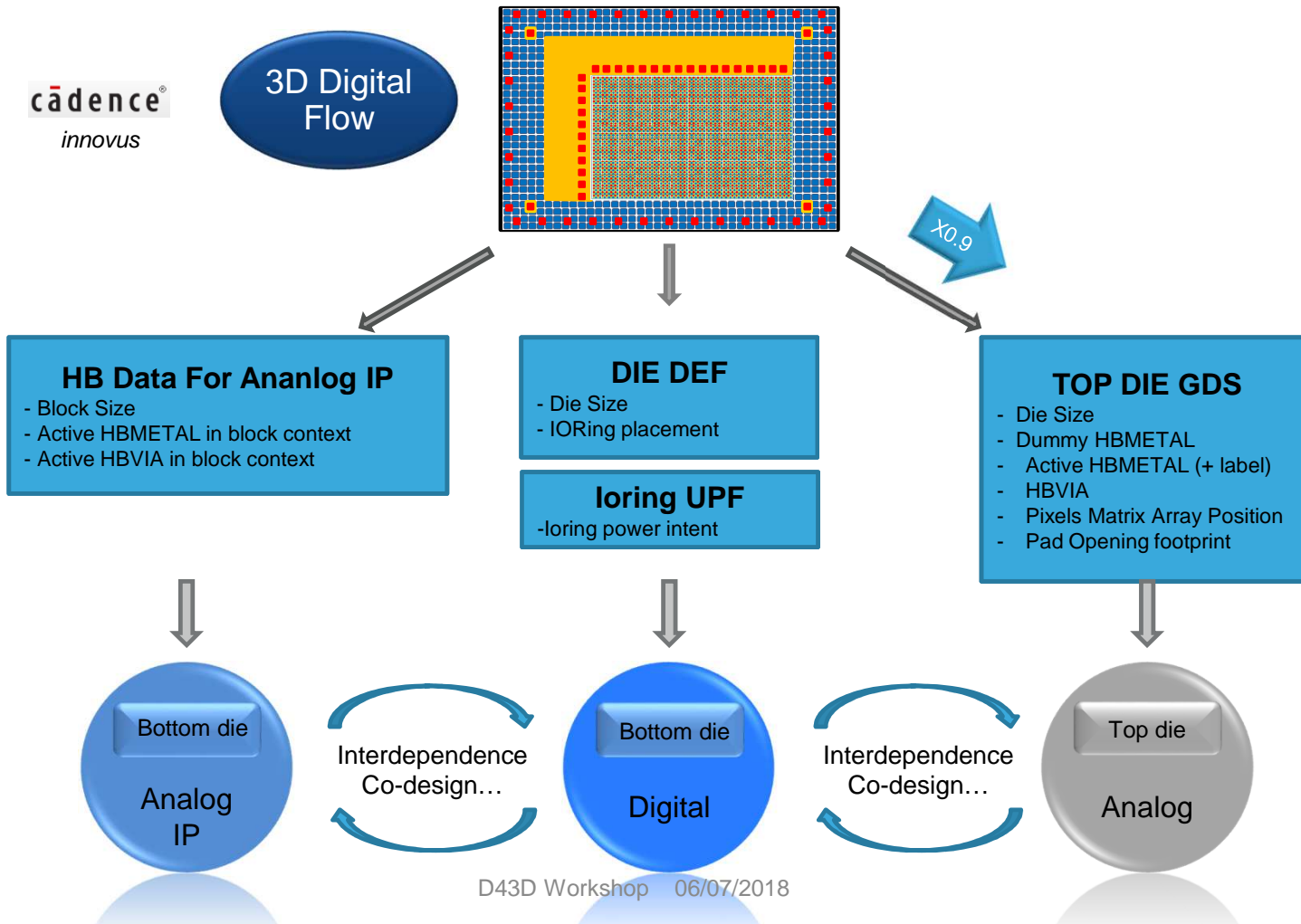
Dummy HBMETAL

Active HBMETAL



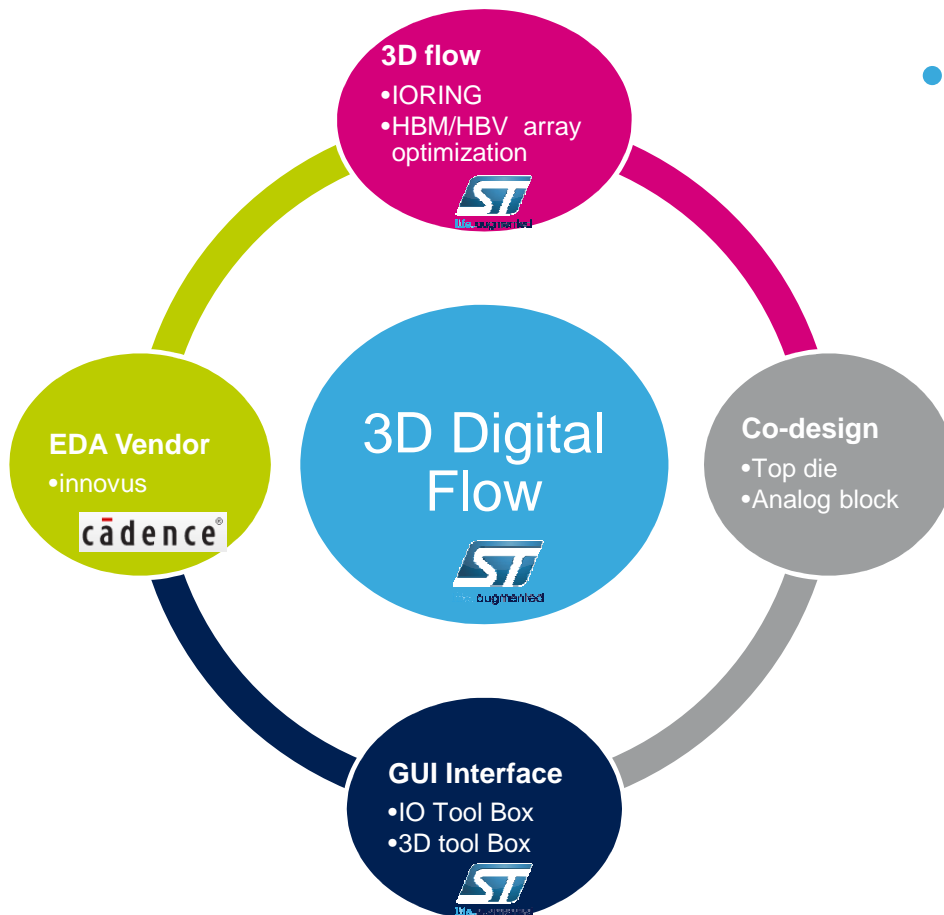
BOTTOM Die
(digital on top)

3D Digital Flow co-design

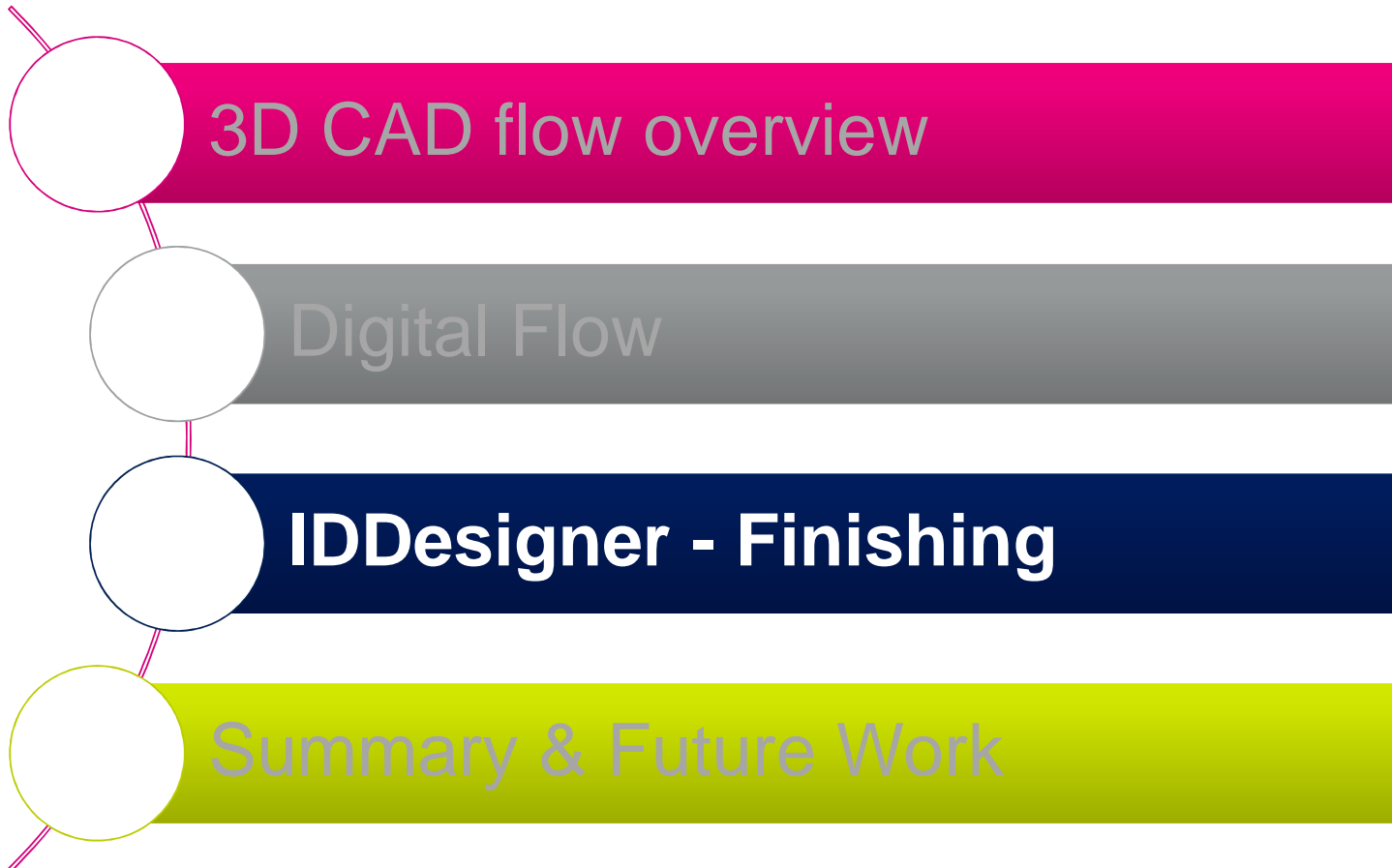


ST 3D Digital flow

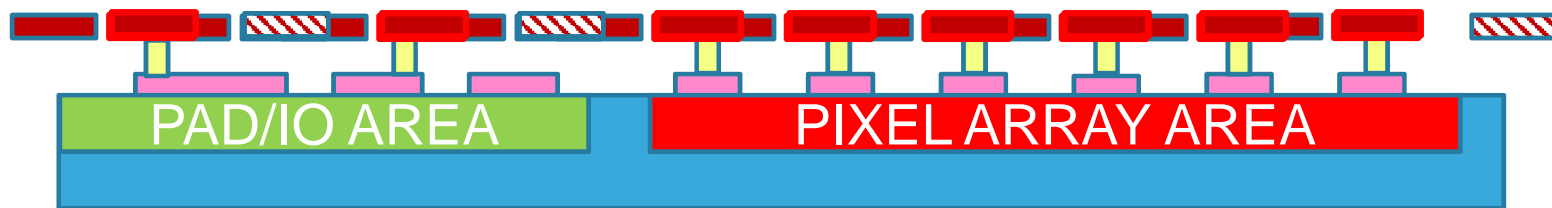
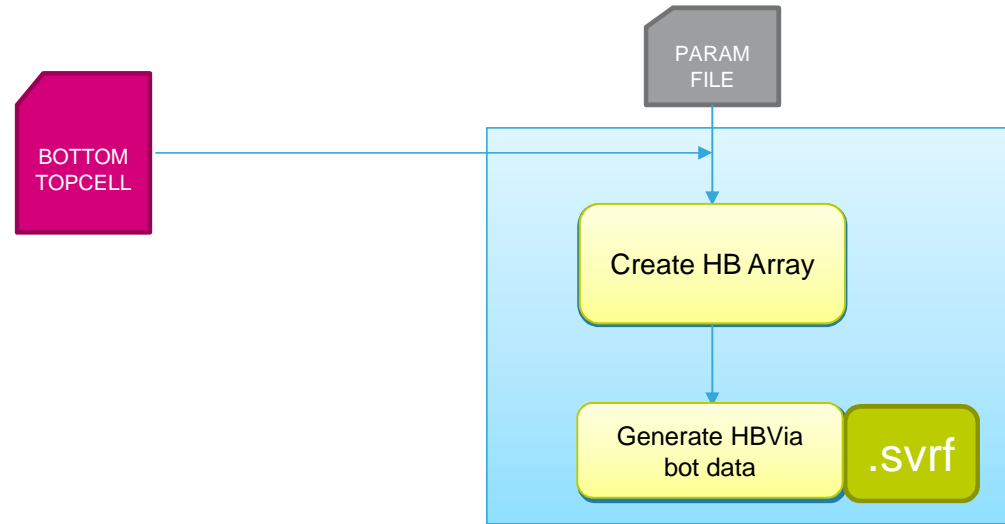
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- ST-DDFM team is providing a 3D flow for digital on top design
 - 3D flow is integrated in our Digital Implementation kit (IOring, Floorplaning and Place and Route)
 - HBM/HBV creation is part of the IOring flow
 - 3D tool box
 - HBM/HBV array optimization
 - User Customization capability
 - Co-design capability



Bottom Tier methodology

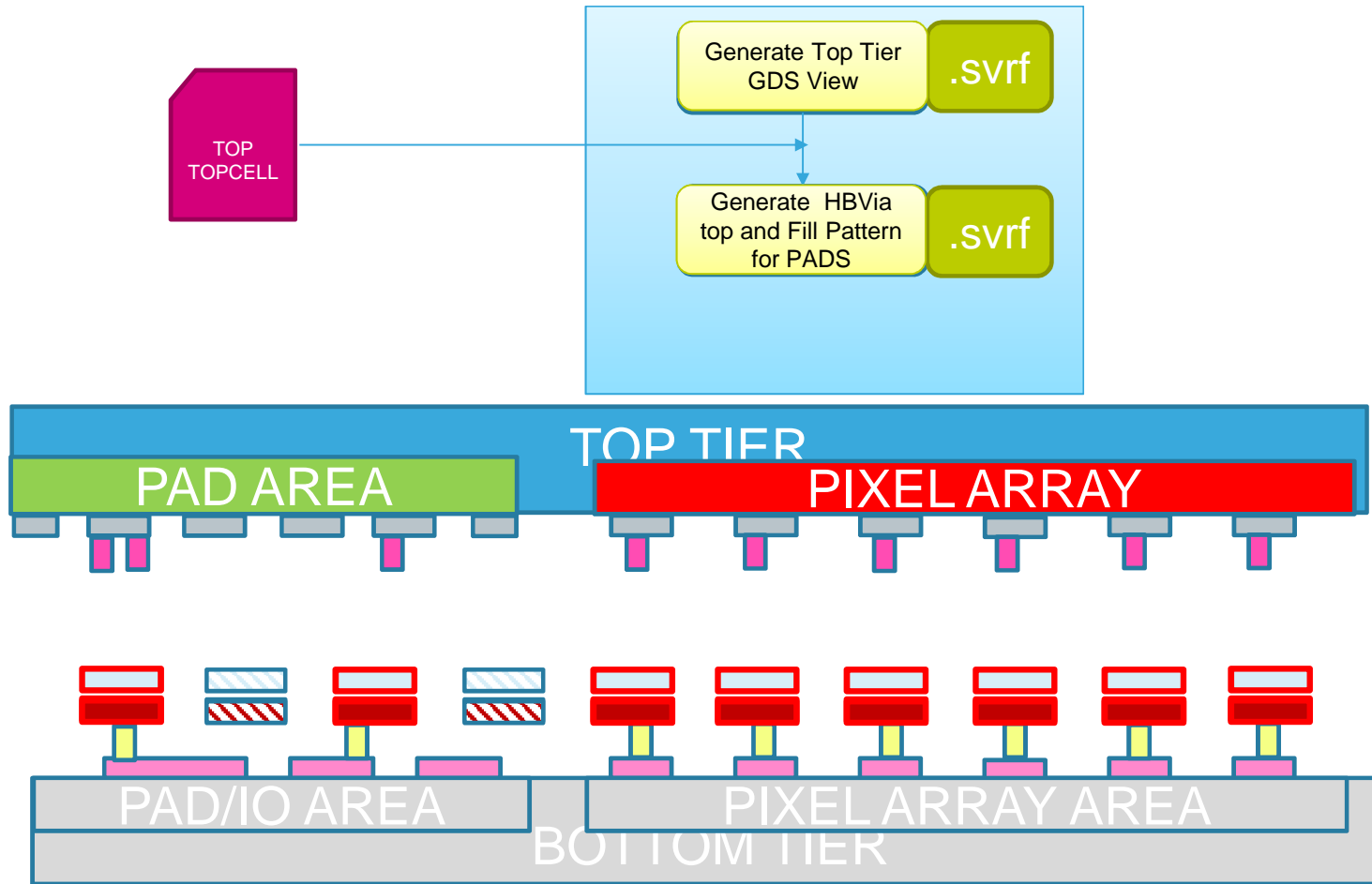


-  HBPAD dummy
-  HBPAD active

-  M7Z
-  HBMETAL bottom
-  HBVIA bottom

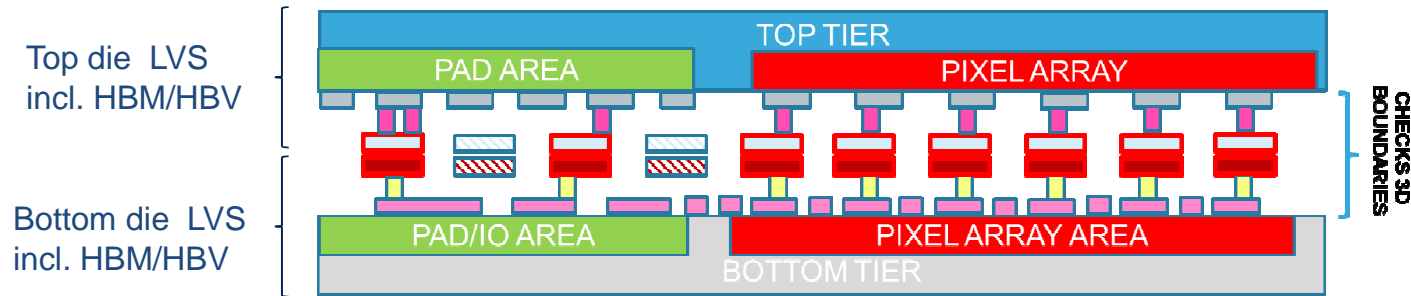
Top Die
(analog on top)

Top Tier implementation flow



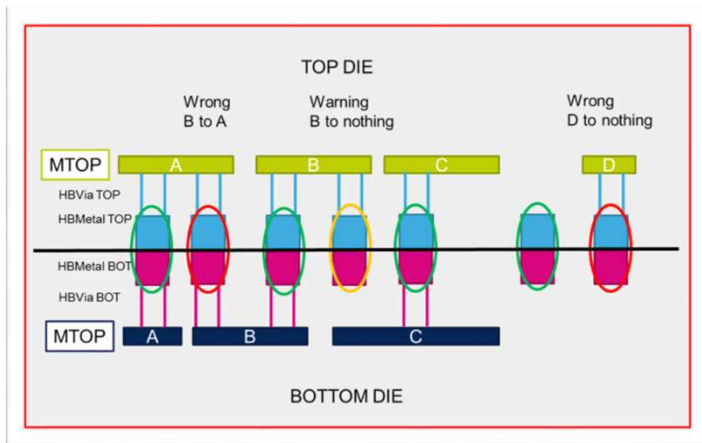
- HBPAD dummy
- HBPAD active
- HBVIA bottom
- HBVIA top
- M4/AP
- HBMETAL top
- HBMETAL bottom

3D Checks strategy

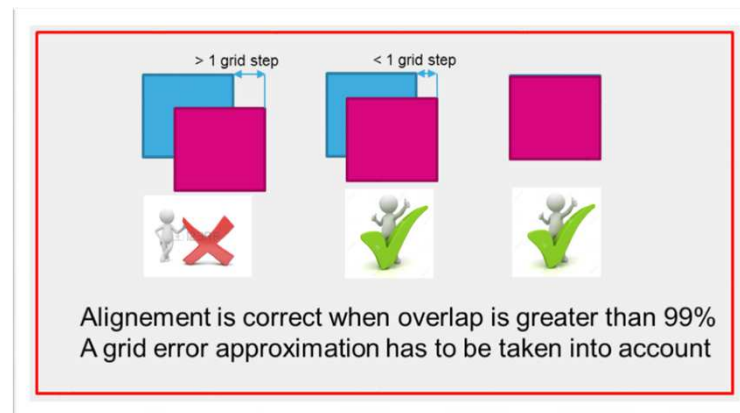


Typical 3D HBP Architecture – Imager on Cmos – W2W

Verification flow defined for 3D HBP



Assumption for good/bad connectivity

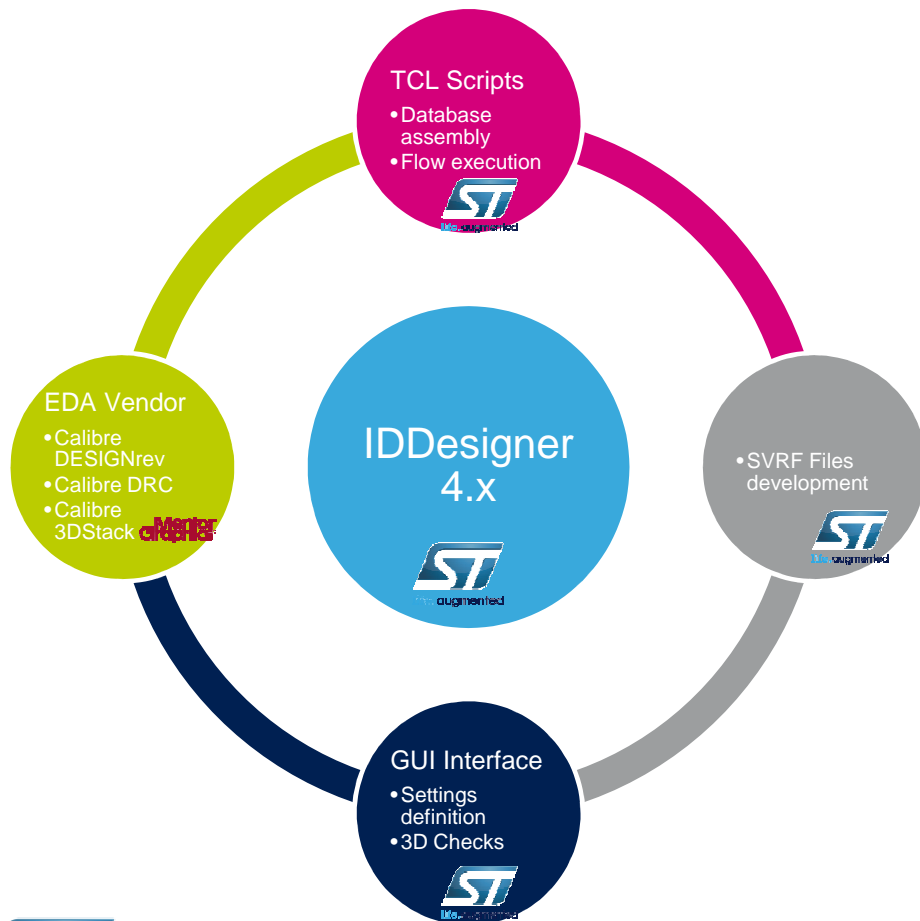


Assumption for good/bad alignment

3D ST Finishing and Verification flow

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- ST-PDK team is providing a full custom automated flow
 - TCL Scripts for the database assembly and the flow execution
 - 2 simple commands (IDDrun, IDDInit)
 - SVRF Files to provide modifications on all databases (HBVia insertion, AP Fill Patterning, ...)
 - GUI Interface (TBD)
 - Settings definition
 - 3D Checks





Summary & Future Work

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- ST 3D design platform
 - Concurrent development between Technology, Design Platform and IMG division
 - 3D CAD flows compatible with mixed applications/technologies
 - Full IPs compatibility with 2D or 3D designs
- 3D design success still strongly depends on thorough project management
- Future Work
 - 3D Verification flow: towards a true 3D LVS, Power Integrity, ...
 - Co-design framework: improve the overall methodology, propose solution for Analog/Analog 3D co-design

Acknowledgments

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- ST / Imaging Product Division
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