Lithography Setup and process variability assumptions for silicon chip manufacturing:

LETI Day's Lithography Workshop July 6th 2018

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Digital Front End Manufacturing / Technology R&D Process Development

With special thanks to

Laurène babaud
Project leader RD lithography

Maxime Gatefait
Project leader RD lithography scanner applications

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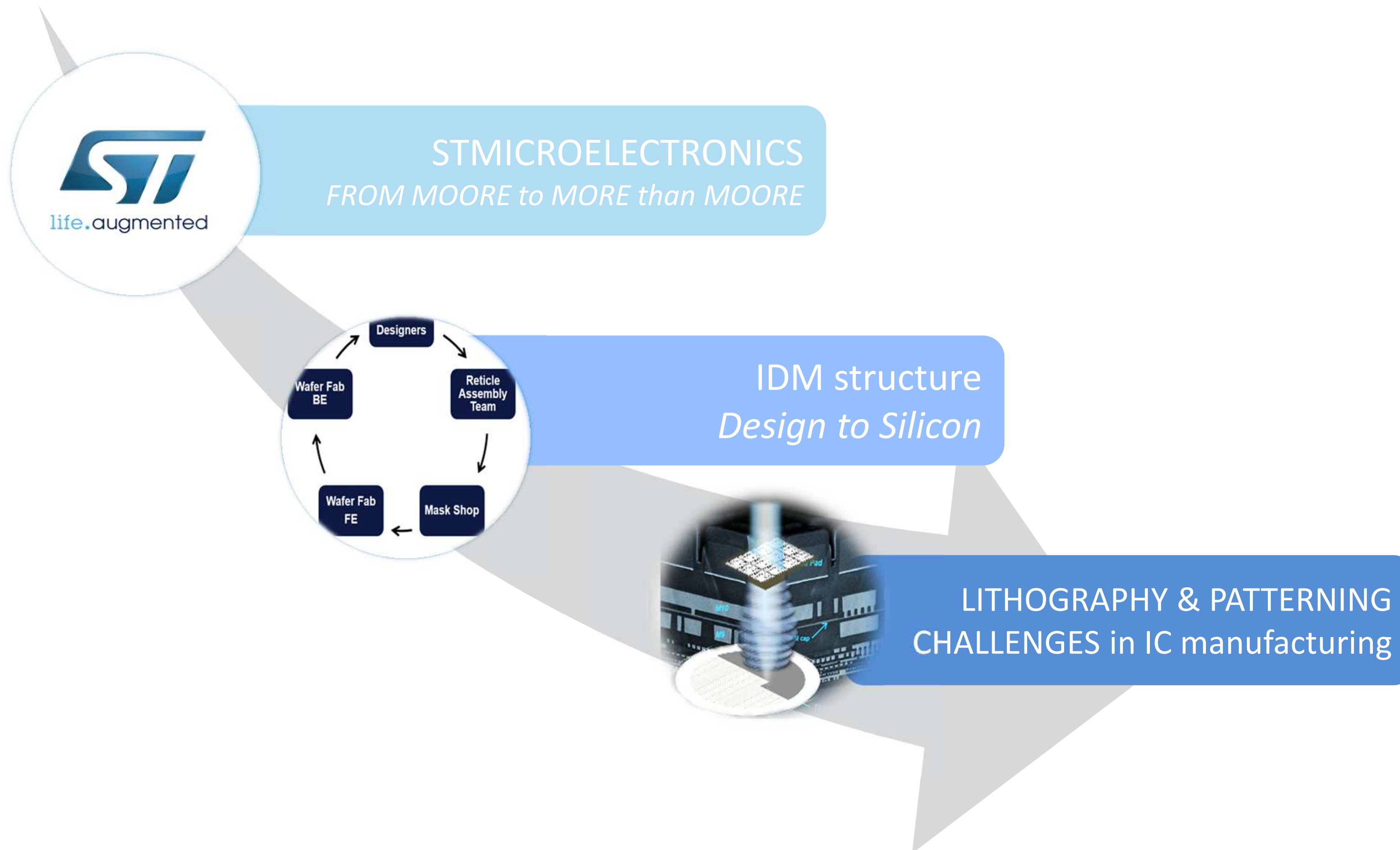
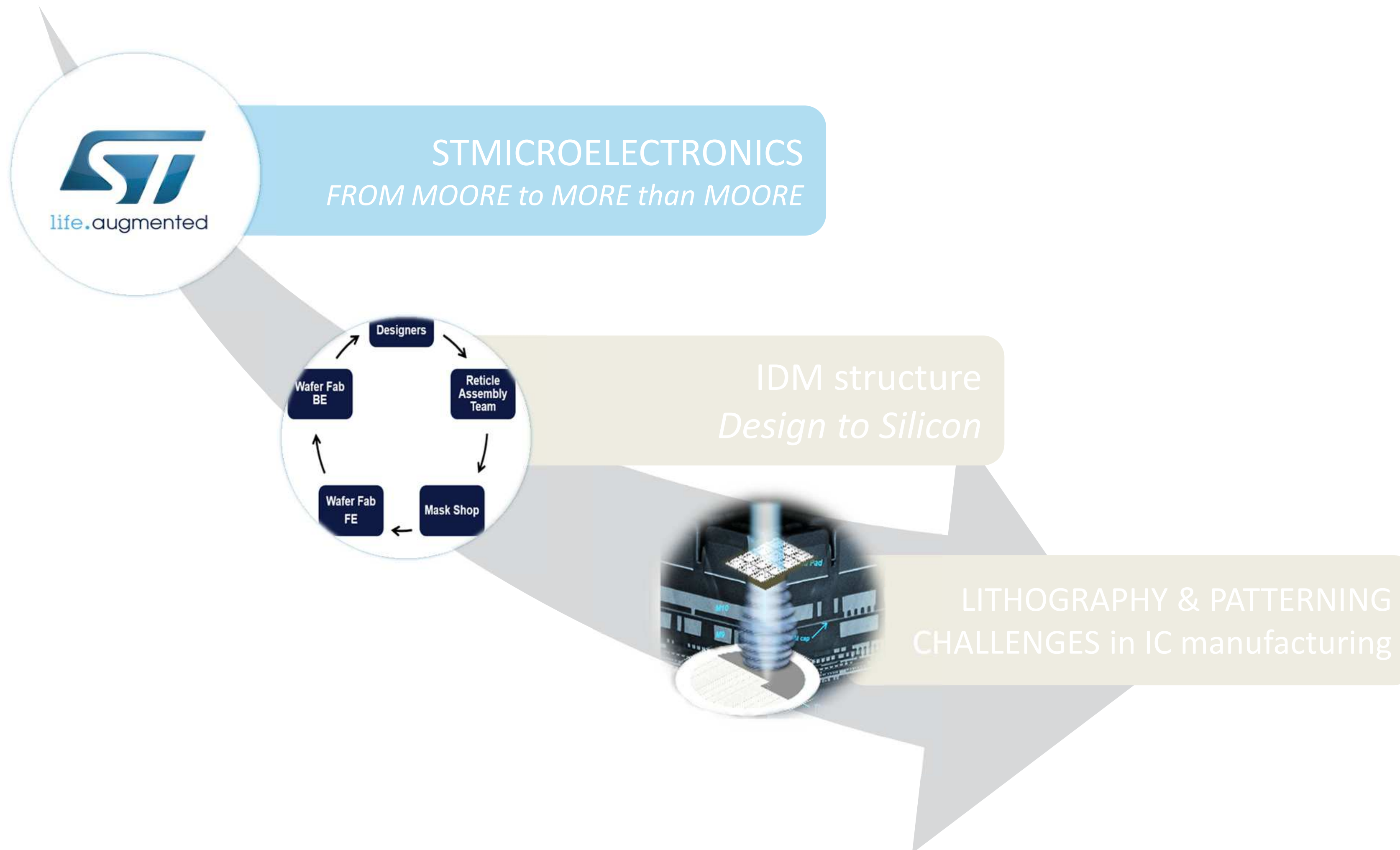
Outline



Outline



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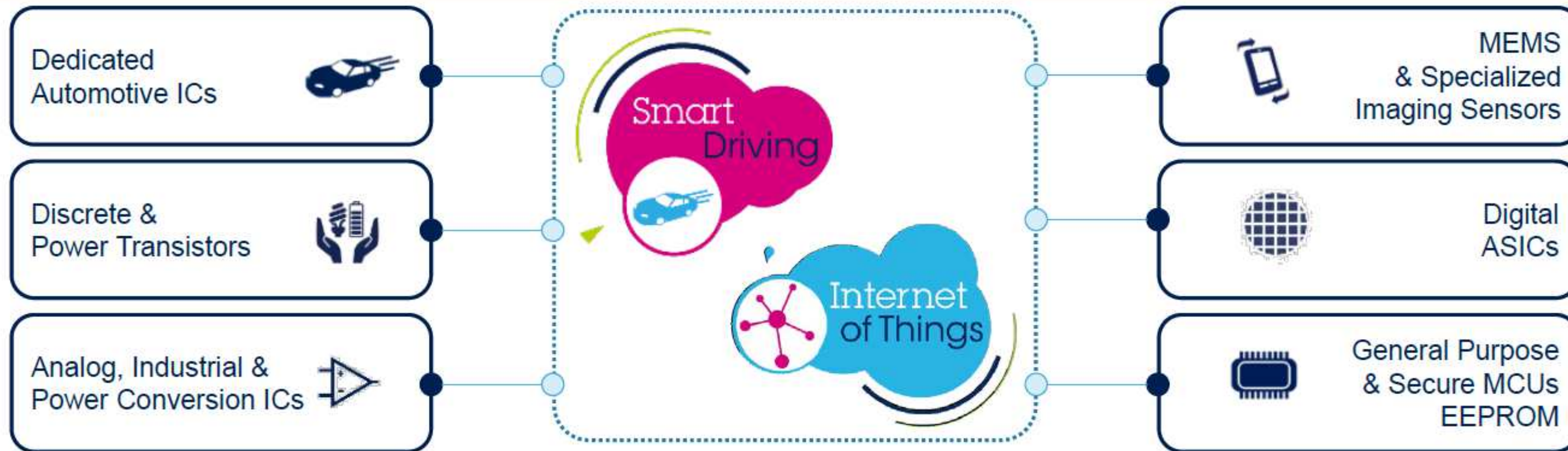

The leading provider of products and solutions for Smart Driving and the Internet of Things
Dedicated Automotive ICs
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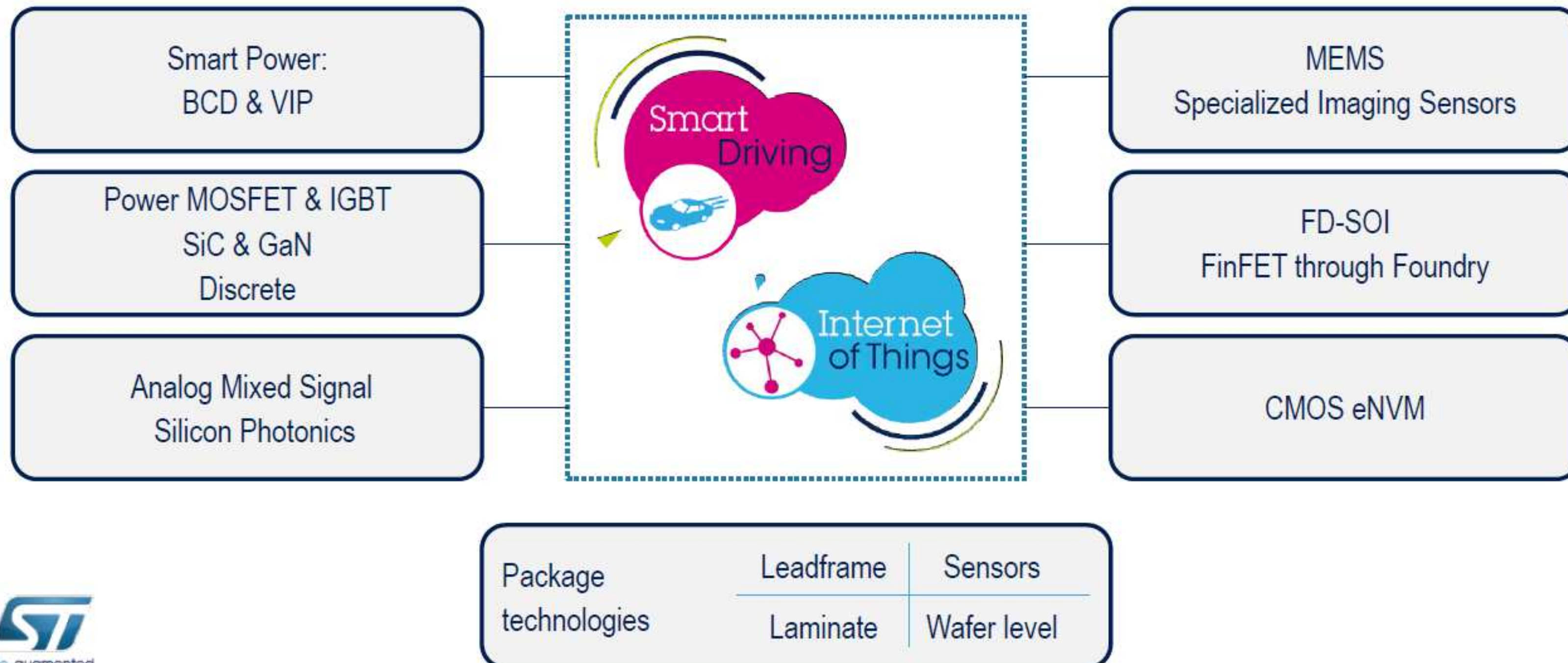
Digital ASICs
General Purpose & Secure MCUs EEPROM
Portfolio delivering complementarity for target end markets, and synergies in R&D and manufacturing



Smart Power: BCD & VIP
Power MOSFET & IGBT SiC & GaN Discrete
Analog Mixed Signal Silicon Photonics
Smart Driving
Internet of Things
MEMS Specialized Imaging Sensors
FD-SOI FinFET through Foundry
CMOS eNVM
Package technologies
Leadframe
Sensors
Laminate
Wafer level
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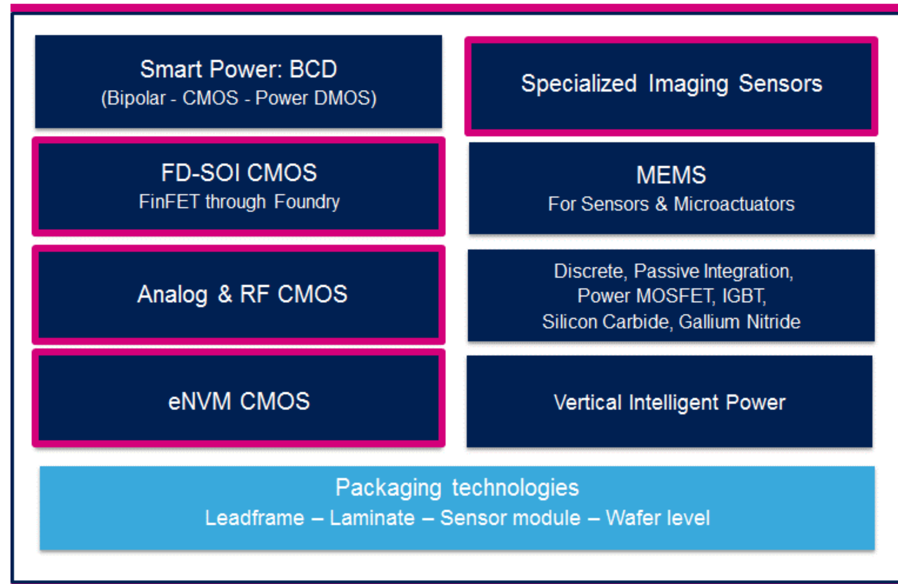
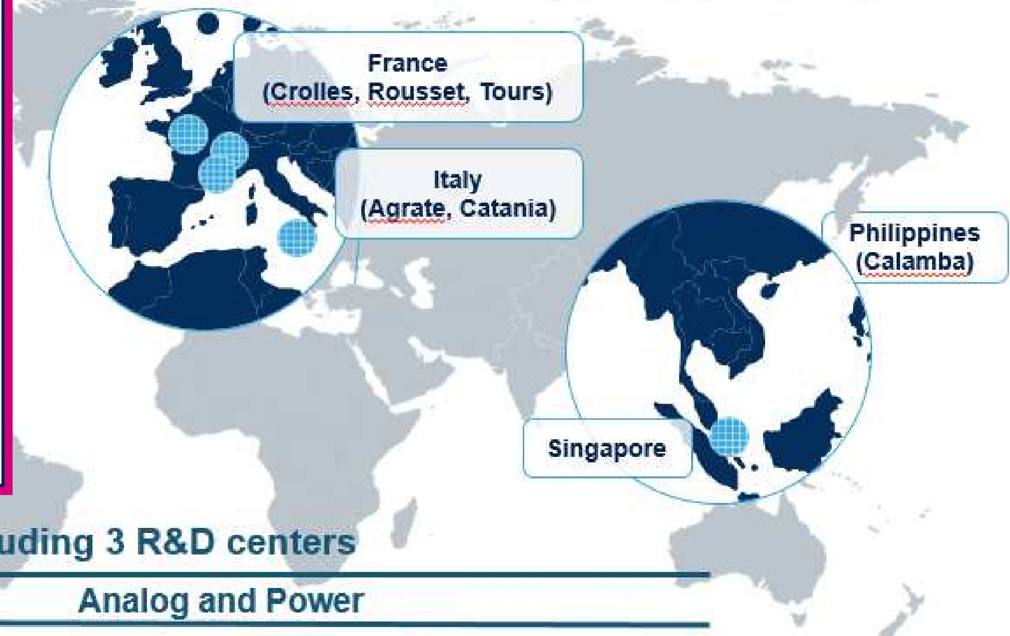
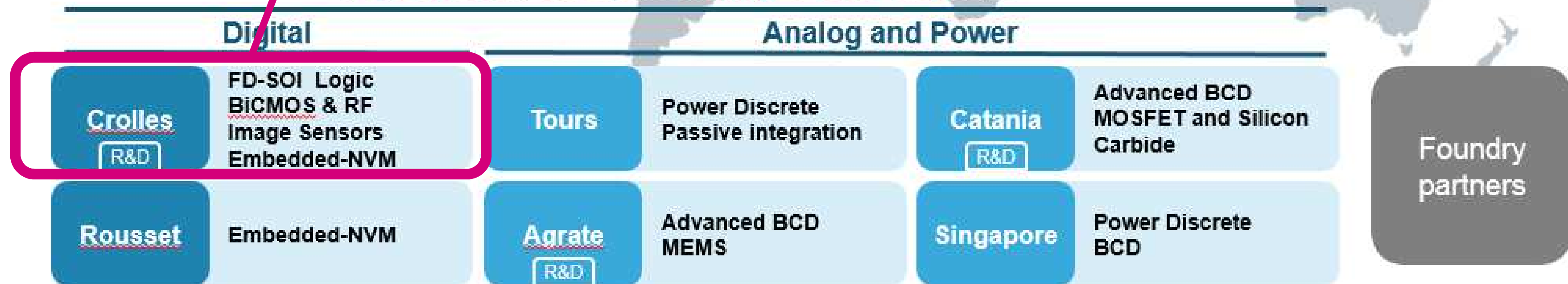
Front-End Manufacturing







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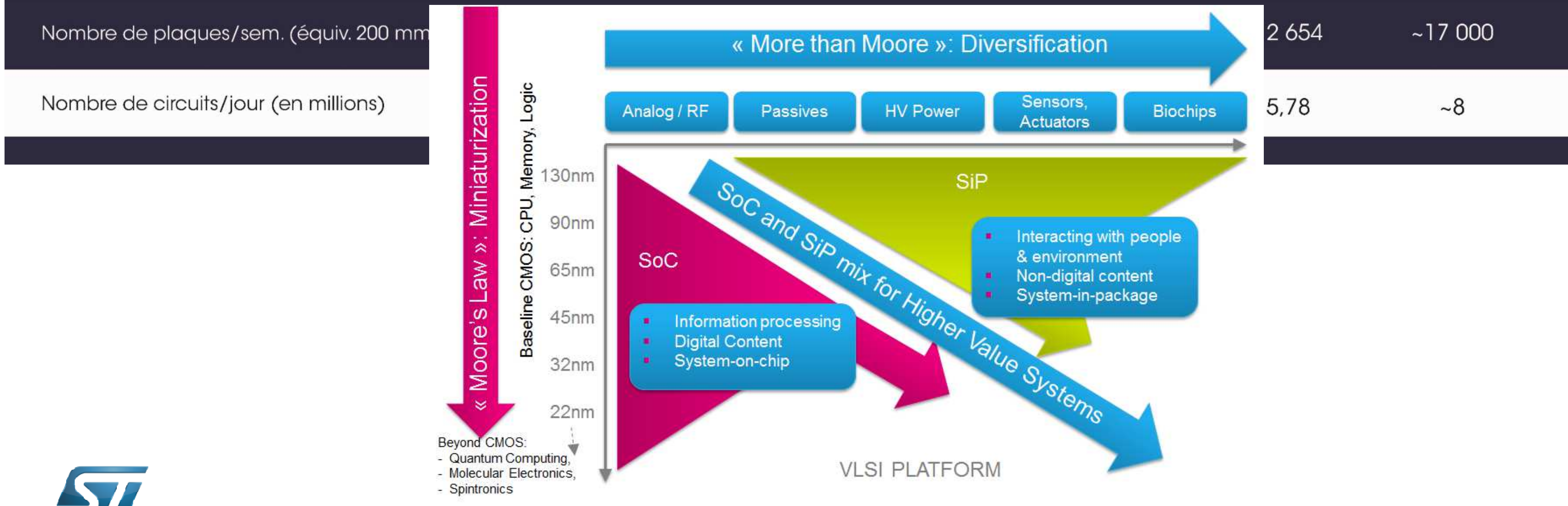
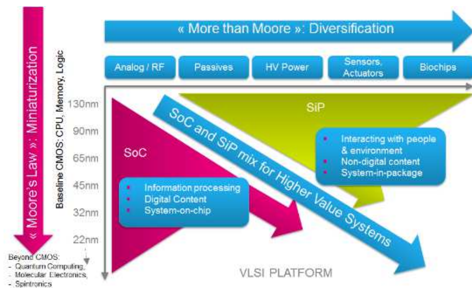
	1992	1997	2000	2002	2007	2012	2017
Surface salle blanche (m²)	4000 Crolles200	5500 + Extension	6700 + Crolles 1 bis	16 700 + Crolles300	18 700 + Extension B2	-	19 300 + Gowning room
Nombre de salariés ST	50	908	1578	2194	3964	4159	4000
Investissements cumulés (millions €)	58	669	1357	1639	2542	3550	> 4500
Technologies	0,5 µm	0,25 µm	0,18 µm	90 nm	45 nm	28 nm	technologies différenciées
Nombre de plaques/sem. (équiv. 200 mm						2 654	~17 000
Nombre de circuits/jour (en millions)						5,78	~8





Techno	Node	Comment
CMOS (Moore)	120-90-55-40-28	Classical More Moore
SOI (FD and others)	65-28	Low power differentiation + Automotive
Specialized Image sensors	I175-140-110-G140	Mix Moore + specific PIXEL integration Front Side / Back Side / Wafer bonding / 3D / Hybrid bonding / Stitching / Color and µlens processes
eNVM	110-90-55-40-28	MCU + Secure & Automotive / Very stringent in term of reliability (request < ppm levels)
BiCMOS	55	High Speed devices, complex integration > 60 masks
Si Photonics	25G-50G	Curvilinear shapes (new Gen need immersion)

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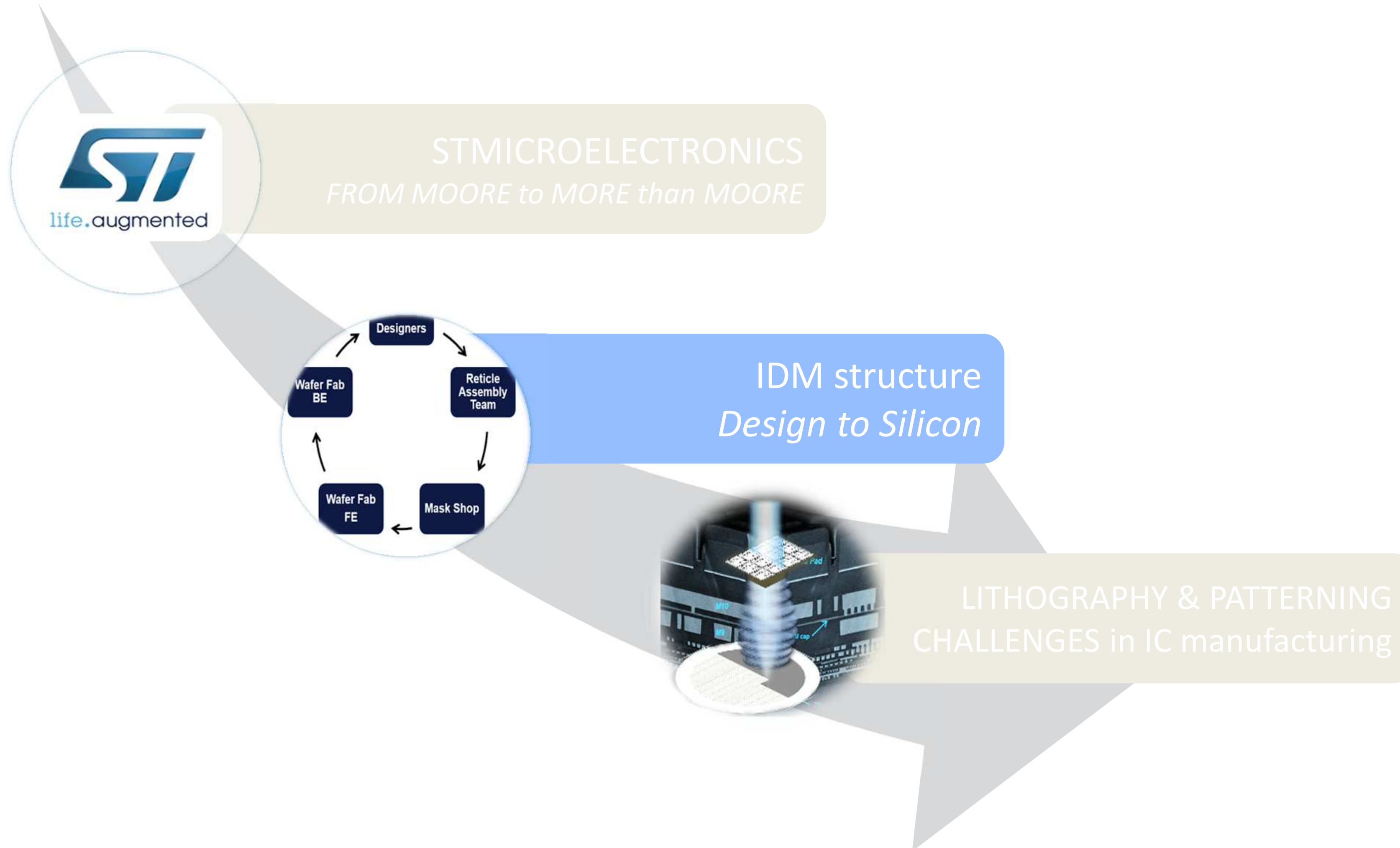
Outline



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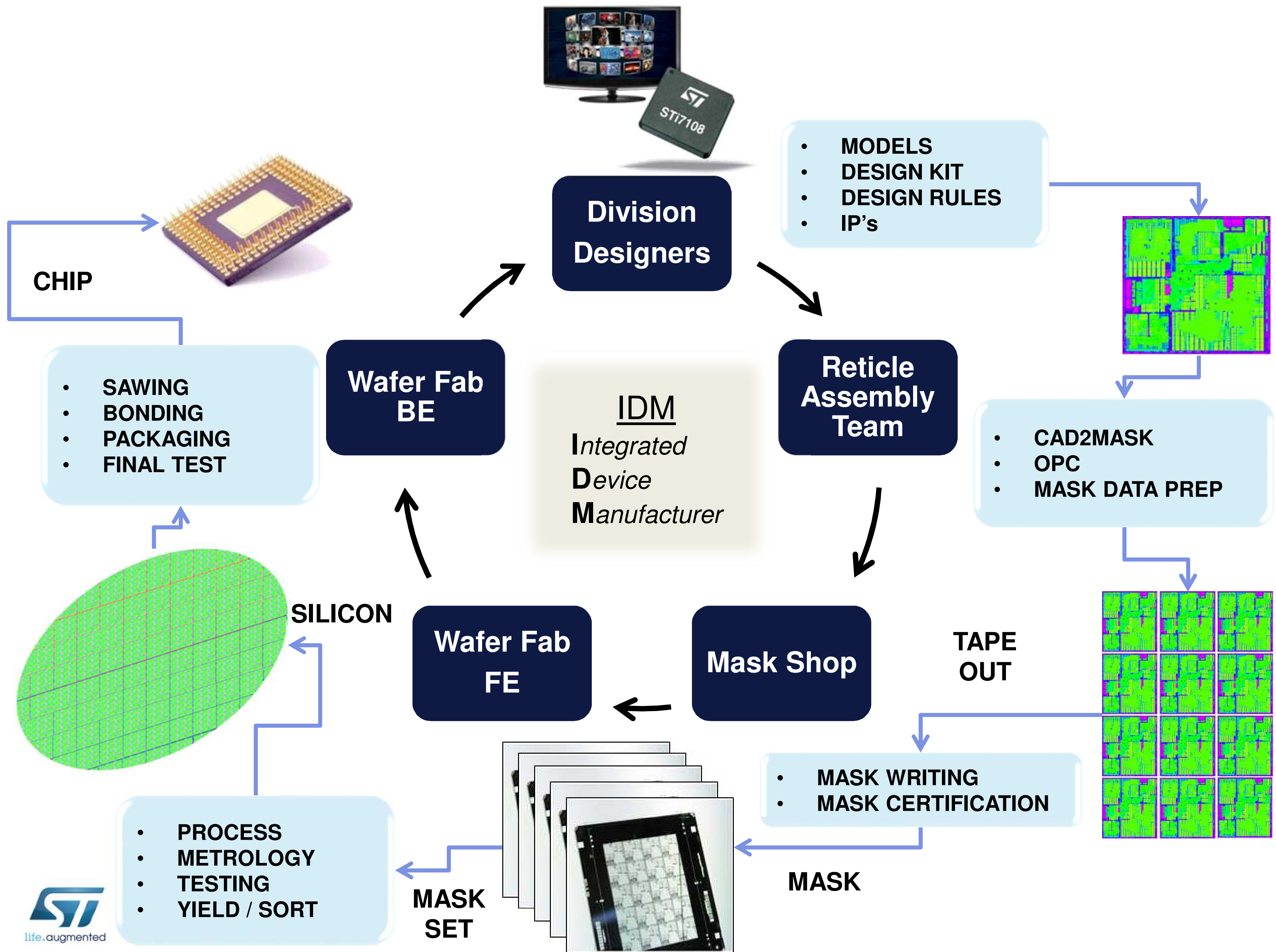

Division Designers
MODELS
DESIGN KIT
DESIGN RULES
IP's
CHIP
SAWING
BONDING
PACKAGING
FINAL TEST
Wafer Fab BE
IDM
Integrated
Device
Manufacturer
Reticle Assembly Team
CAD2MASK
OPC
MASK DATA PREP
SILICON
Wafer Fab FE
Mask Shop
TAPE OUT
MASK WRITING
MASK CERTIFICATION
PROCESS
METROLOGY
TESTING
YIELD / SORT
MASK SET
MASK
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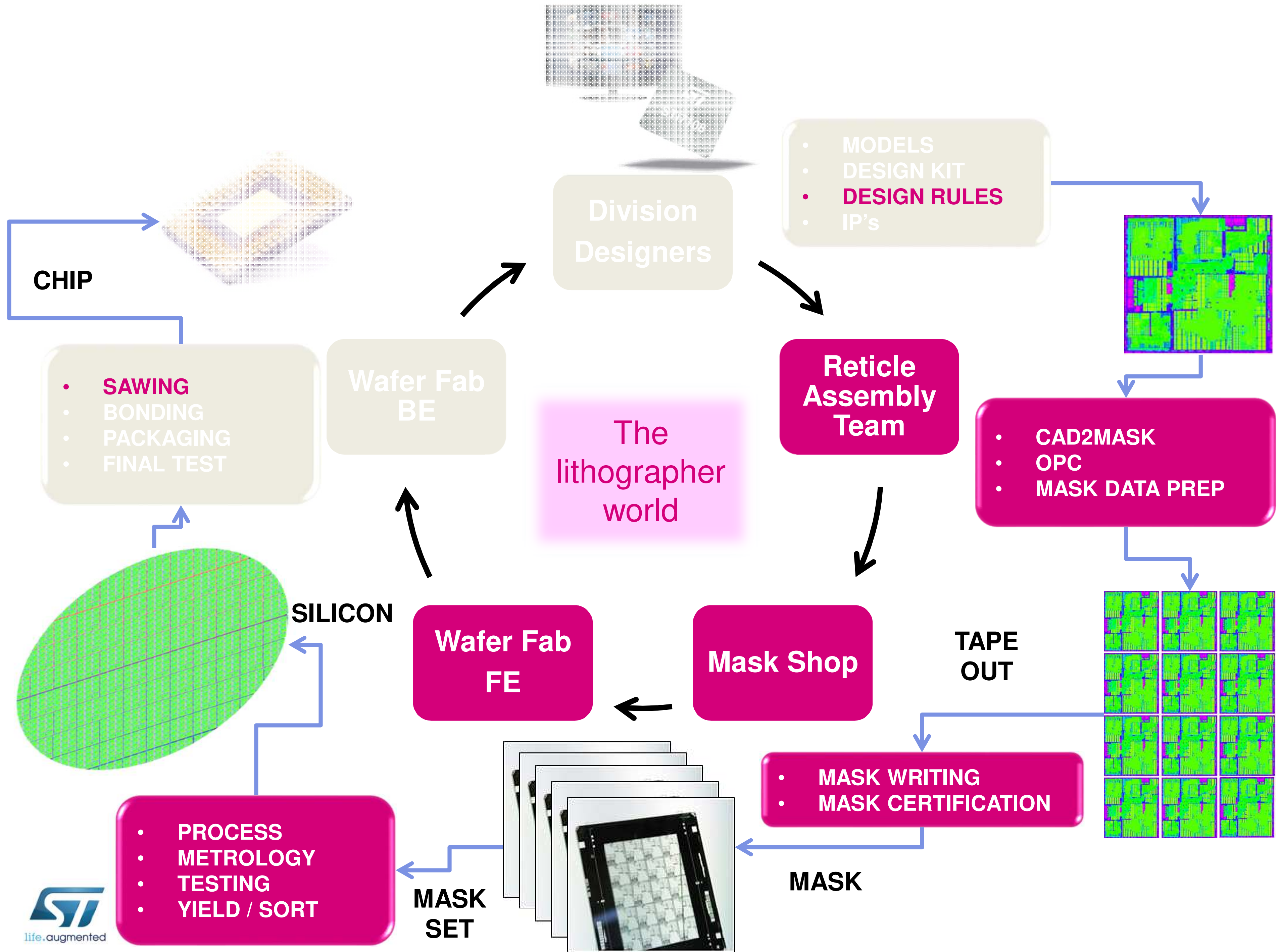

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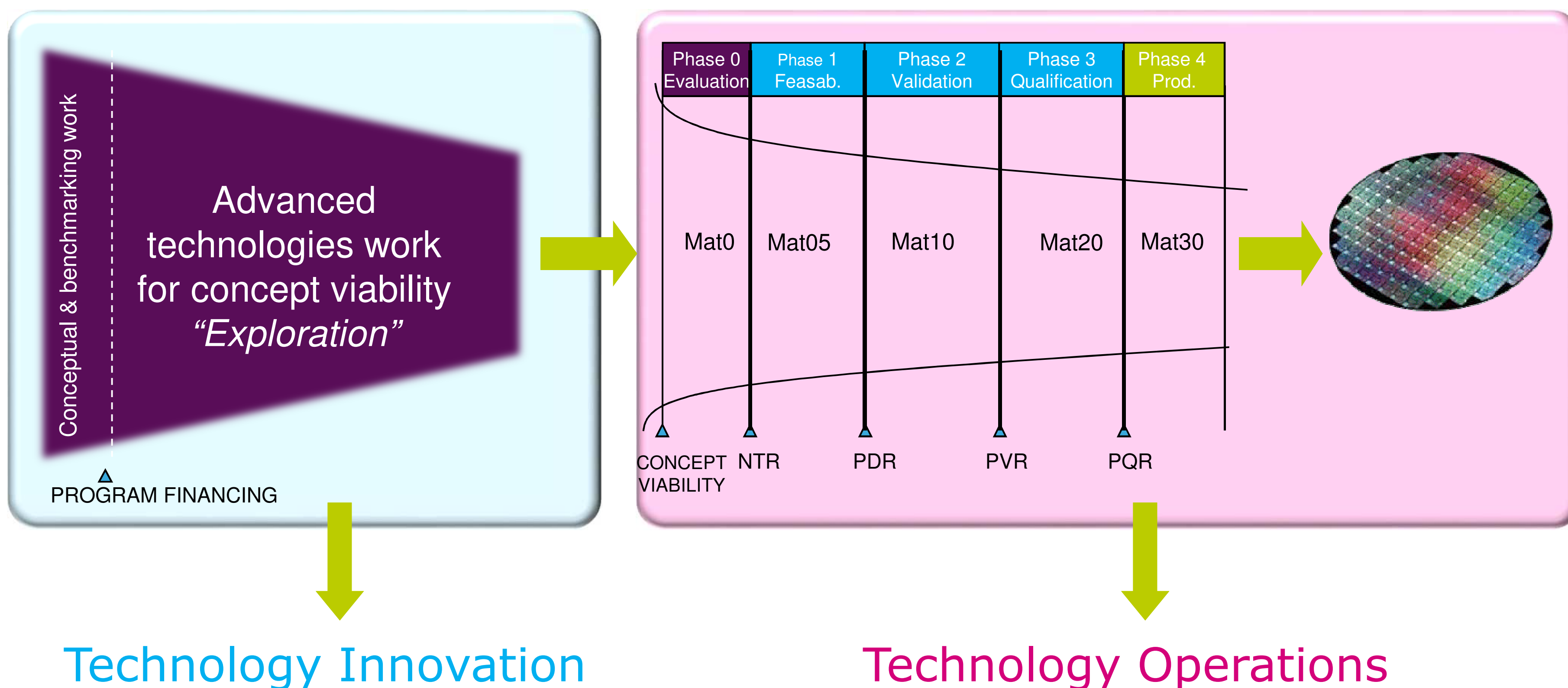
Technology Innovation Process



Technology Innovation

Technology Operations

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Technology Maturity Process

MAT05
feasibility

PROCESS ASSUMPTIONS
Calculate Design rules

Process Selection

Fix process variability targets
Select Process

MAT10
validation

DESIGN RULES MANUAL V1.0
OK for massive design of libraries

Process Capability Assessment

Process characterization / Capability Consolidation

MAT20
Qualification

PROTOTYPING
Many new mask sets very fast cycle time

Process Capability validation

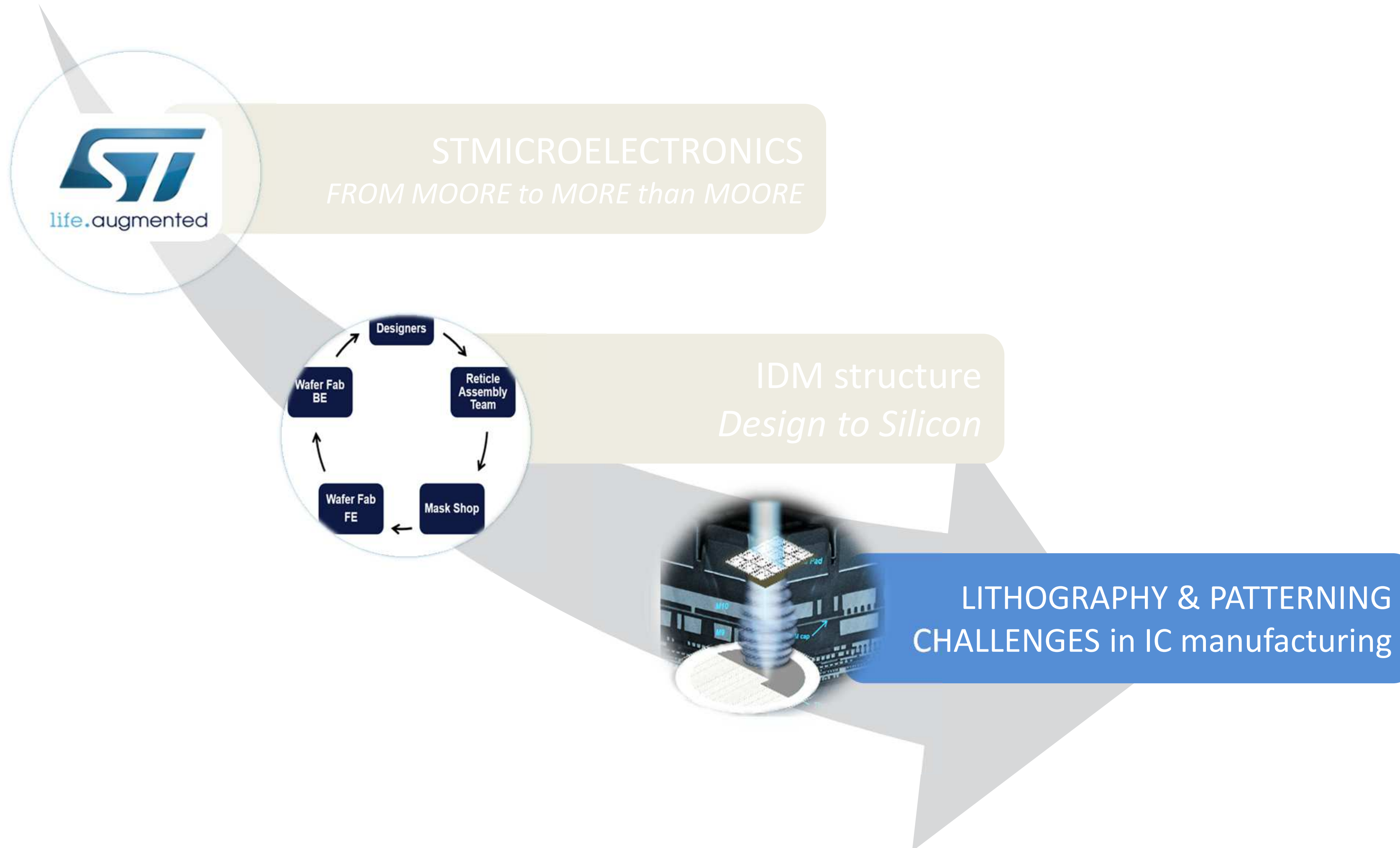
Secured Control Plan
APC / SPC* setup
FMEA's etc...

MAT30
Production

PRODUCTION

* **APC** Advanced Process Control (Run2Run / subrecipe etc..) ; **SPC** (Statistical Process Control: Control chart tool and process drift monitoring)

Outline



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PRODUCTION

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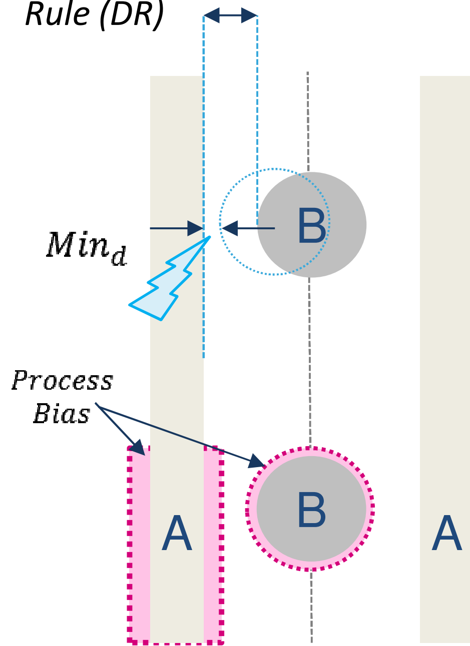
The Process Assumptions Challenge

Edge Placement Case

$$DR = Min_d + \frac{Bias_A}{2} + \frac{Bias_B}{2} + \frac{4}{3}\sqrt{\left(\frac{3\sigma_{CD_A}}{2}\right)^2 + \left(\frac{3\sigma_{CD_B}}{2}\right)^2 + (3\sigma_{OV_AB})^2}$$



PA component	Description
Criteria	*Failing mechanism @origin of the rule*
Bias	*Difference CAD (design) vs Silicon (process)* *All effects leading to Silicon edge ≠ drawn*
Variability	*Process variability (3sigma)*

Link Design / Process variability

- **Some design rules are set at the limit of process capabilities.**
- **In-line control (CD) plan must secure variability**
- **SPC is most of the time performed per layer, little visibility on interlayer interactions (except OVL)**

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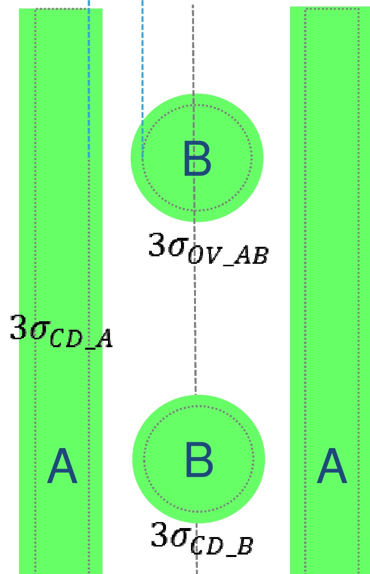
Motivation: The Process Assumptions Challenge

Edge Placement Case

$$DR = Min_d + \frac{Bias_A}{2} + \frac{Bias_B}{2} + \frac{4}{3}\sqrt{\left(\frac{3\sigma_{CD_A}}{2}\right)^2 + \left(\frac{3\sigma_{CD_B}}{2}\right)^2 + \left(3\sigma_{OV_AB}\right)^2}$$

Design Rule (DR)



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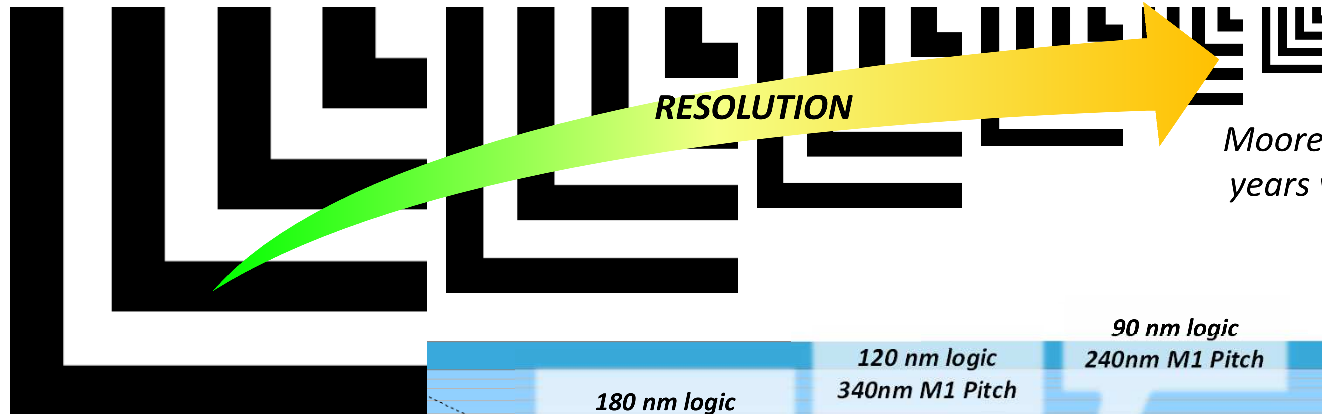
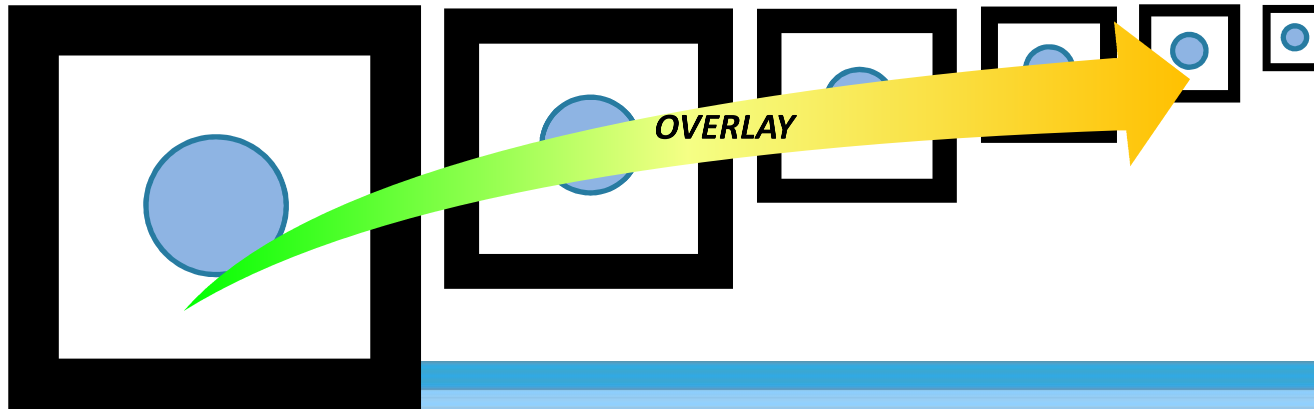
Motivation: The more we shrink the more we challenge tool capabilities (process margin reduces very significantly)



Moore's Law > One new technology every 2 years with 50% surface Shrink and roughly 0.7 resolution shrink

Motivation: The more we shrink the more we chalenge tool capabilities (process margin reduces very significantly)



(nanometres)

1000
100
10
1

1980 1985 1990 1995 2000 2005 2010 2015 2020

436 nm
365 nm
248 nm
193 nm
193i nm
13.4 nm

Exposure Wavelength
CD Gate logic
Pitch Metal1
GATE Contacted Pitch
OV budget (Contact-Poly)

40 / 28 nm logic & beyond Relax GATE pitch for OVL Contact to GATE

Multipatterning ERA, Overlay gets extremelly tight

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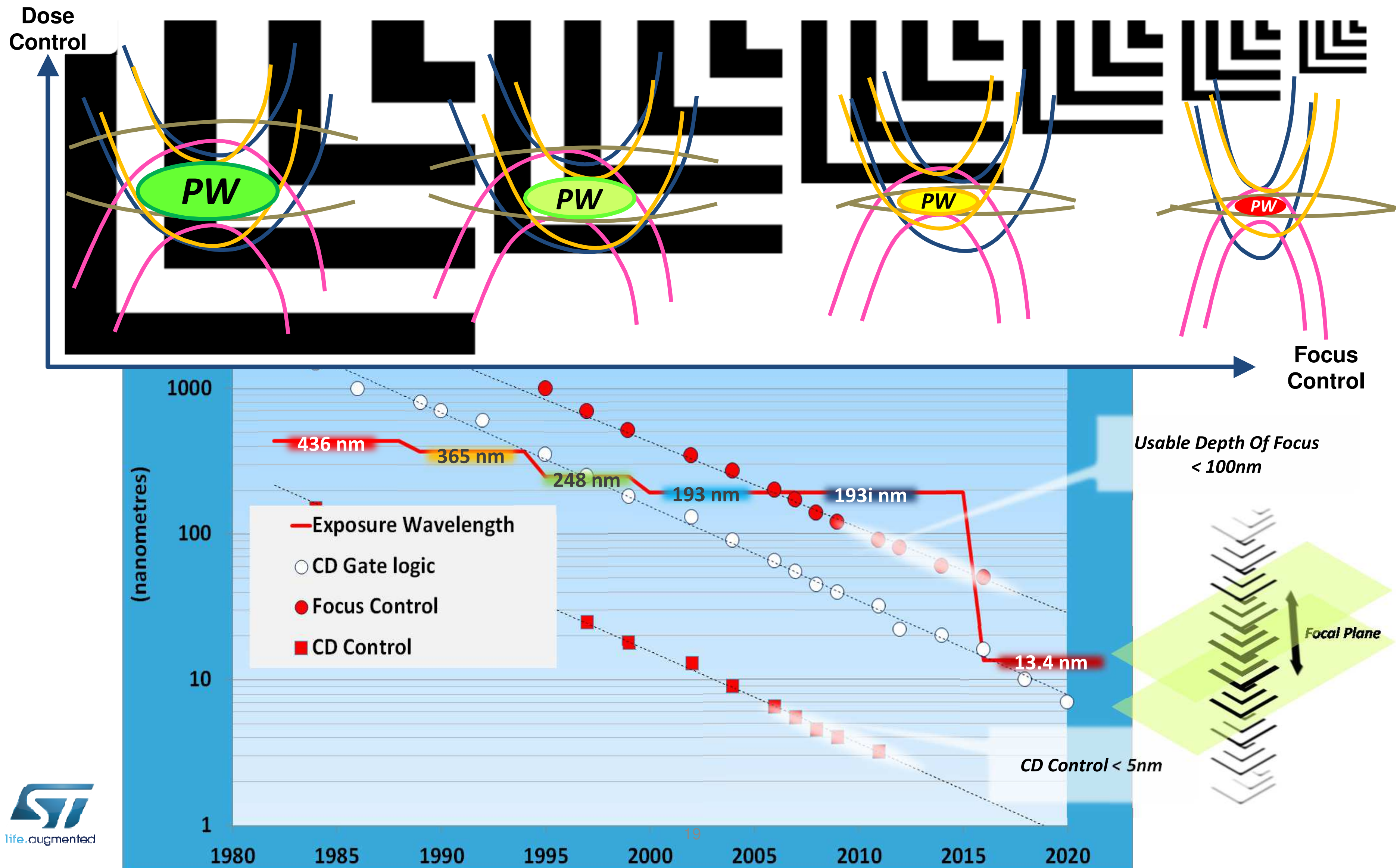

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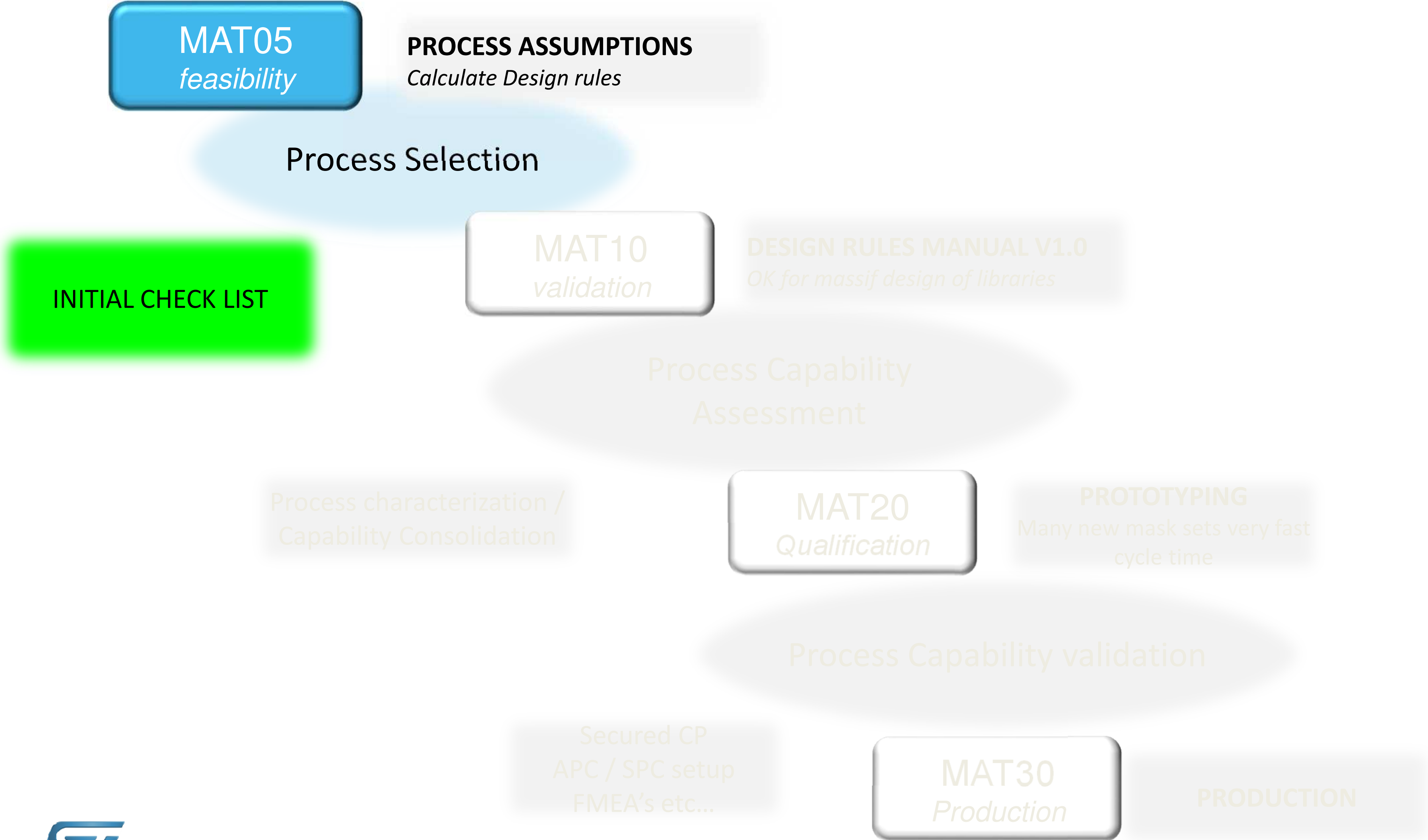
Technology Maturity Process



Lithography Checklist why?

Beginner
or
Expert

Mesdim

R2R options

ARC/Barc/
Tarc

xposure
tool

Mask

budget

Overlay

Defectivity

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Workspace

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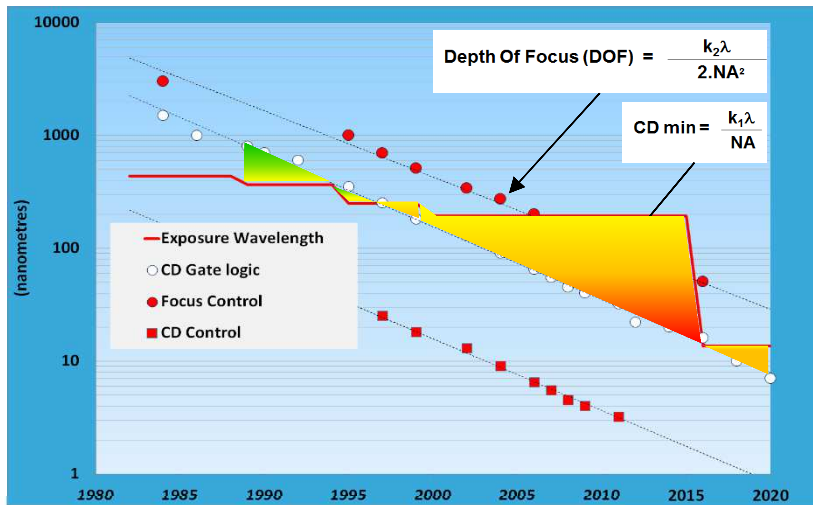
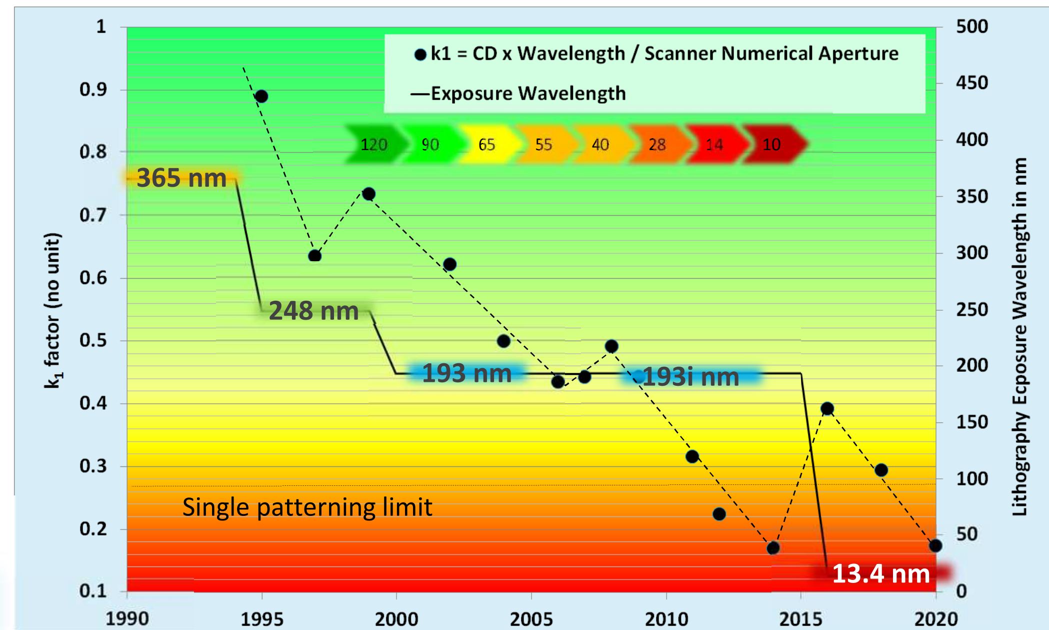
Technology Maturity Process

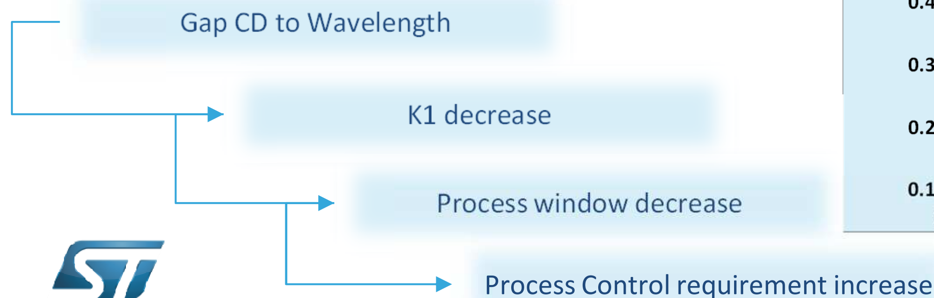
Phase	Step	Item
2- initial setting	1- Choice of litho process type	Exposure technology type: 248, 193, 193i, 193i NTD
		Planarization solution if needed: Barc/Trilayer
		Antireflective solution if needed: DBARC/BARC/TARC
		Solution for adhesion : DBARC/BARC/preatment.
		Resist Thickness range: Implant Conditions / Etch budget
		Resist stack preliminary choice
		Top coat solution if needed
		Litho exposure tool (From available Scanner List: 365 / 248 / 193 / 193i)
	2- Mask	Mask Grade & type
		Mask type for 193nm: binary, att PSM, OMOG
		OPC
	3- Metro CD	MONITORING feature choice
		Choice of Pattern type sensitive to focus: CD/pitch, stack, orientation (if non symetrical illum is used)
		IF Pattern type, CD, pitch, orientation and stack; spatial repartition
	4- Metro OVL	OVL Pattern type, intra field spatial repartition, layers n-1 for overlay
		Measurement quality (TIS, residual...)
	5- Track recipe	Initial Track recipe
		HMDS T°C and time
		EBR rules (chemical + optical)
		Dev type LD, GP nozzle, ADR stream (BKM)
		Double check PAB / PEB T°C and time.
		BTM recipe, barometric spin curve link.
	6- Scanner	Illumination choice
		Job scanner
	7- Scanner: Setting Nominal	R2R/APC Nominal Setup
		R2R/APC JOB tuning:
		R2R/APC loop mgt--> Energy, Overlay.
	8-MES: creation Capability	Capability list in the MES (association Litho Cluster / layer process enablement)

Motivation: Sometimes the challenge is not where you would think it is.

The k factor is a representation of the complexity to achieve a given CD or Focus control within specification. The smaller it is the more challenged the tools are due to variability control.

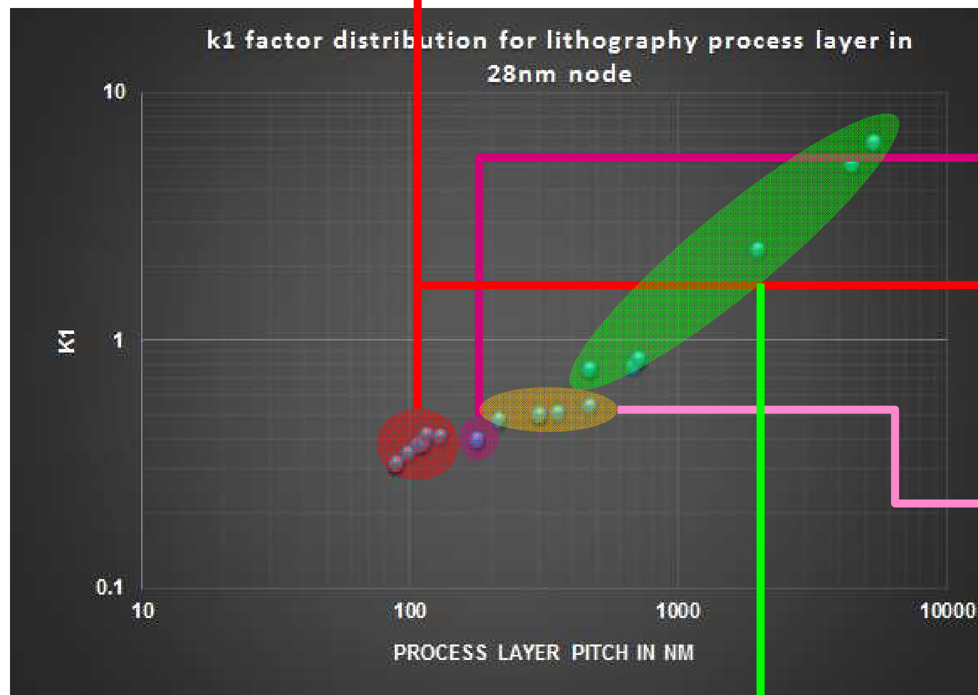






Example of 28nm node

Within a given technology node all the layers do not have the same criticity, therefore we will span a large k_1 range (process complexity)



Lambda	pitch	NA	k1
193i	90	1.35	0.31
193i	90	1.35	0.31
193i	90	1.35	0.31
193i	90	1.35	0.31
193i	90	1.35	0.31
193i	90	1.35	0.31
193i	100	1.35	0.35
193i	108	1.35	0.38
193i	113	1.3	0.38
193	180	0.85	0.40
193	180	0.85	0.40
193	180	0.85	0.40
193	180	0.85	0.40
193i	130	1.2	0.40
193i	117	1.35	0.41
193i	117	1.35	0.41
193i	117	1.35	0.41
193i	117	1.35	0.41
193i	117	1.35	0.41
193	216	0.85	0.48
248	306	0.8	0.49
248	306	0.8	0.49
248	306	0.8	0.49
248	306	0.8	0.49
248	306	0.8	0.49
248	306	0.8	0.49
248	306	0.8	0.49
248	360	0.7	0.51
248	468	0.57	0.54
248	468	0.57	0.54
248	468	0.8	0.75
248	468	0.8	0.75
248	684	0.57	0.79
248	684	0.57	0.79
248	720	0.57	0.83
248	720	0.57	0.83
248	720	0.57	0.83
248	720	0.57	0.83
248	720	0.57	0.83
248	2000	0.57	2.30
248	2000	0.57	2.30
248	4455	0.57	5.12
248	5400	0.57	6.21

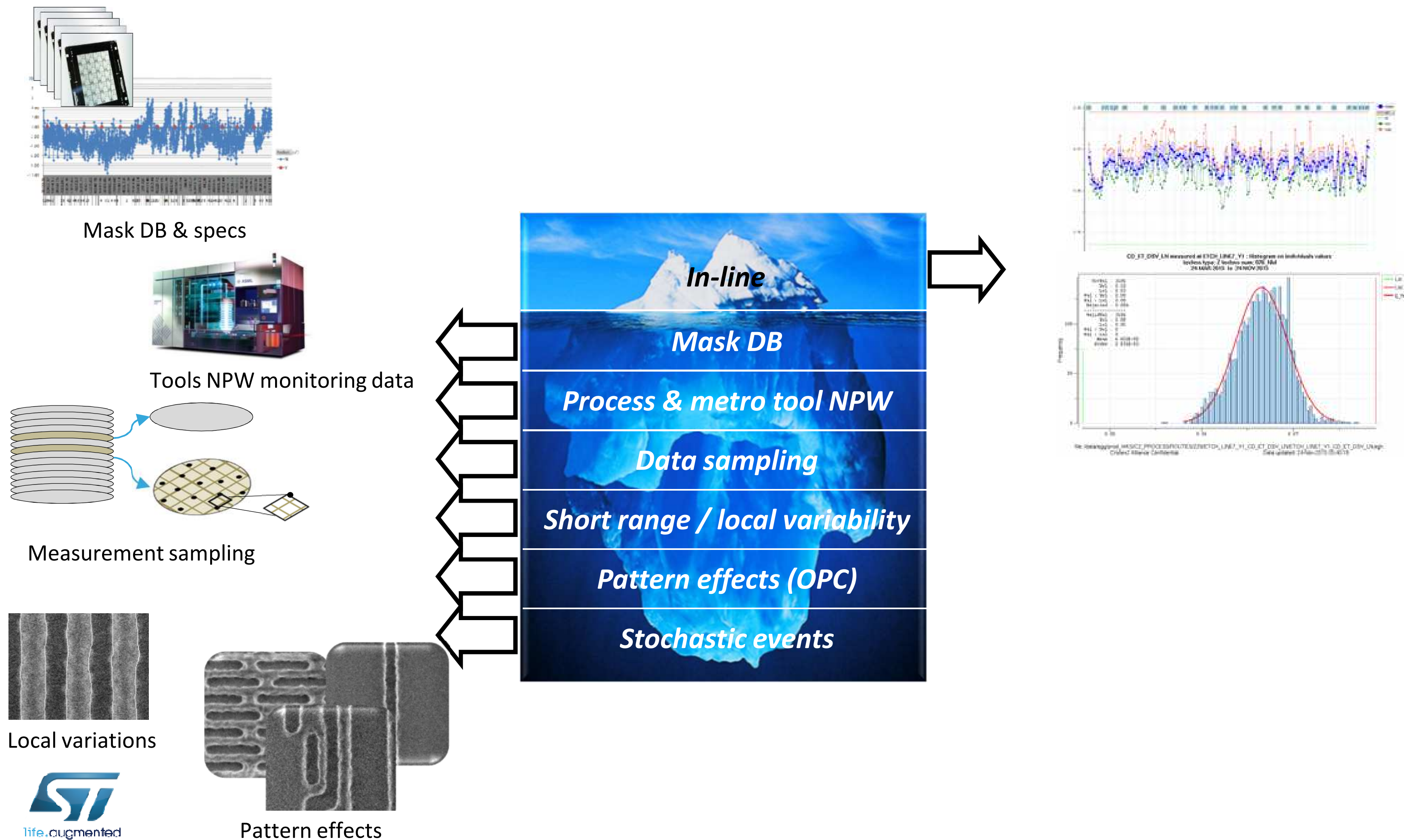
The lower k1 the more important it is to control and perfectly center the process in term of Dose & Focus.

“less” critical layers may appear in low k1 situation as well !
All the tools are challenged (Cost of Ownership is driving to)

3- …on		
	Focus	Best Focus determination
	Dose	Best Dose/Slope determination
	Process Window DOF/EL	EL/Dof Pocess window determination
		If above Criteria not achieved: Resist benchmark, ARC, PEB/PAB T°C opti, Dev recipe, illumination screening/DOE, mask/OPC optimization
	Resist Budget	Resists thickness validation: dry etch layer.
		Resists thickness validation: implant layer.
	CD bias	CD Bias during etch process (Photo-Etch Bias) or during implantation (Resist shrink during implant)
	OPC check	OPC Check
	… tuning	
	Def	PWQ, std def inspection
	MEEF	MEEF evaluation for Mesdim (mandatory for Symphony setup). MEEF evaluation for critical pitch or pattern. If needed: Resist benchmark, PEB/PAB T°C opti, illumination screening/DOE, mask/OPC optimization, assist features
	Resist profiles	X sections (+Tilted SEM if interesting)
	Rework	Rework process validation
	Symphony Set up	Dose Nom, slope, Focus, MEEF
	Throughput & cascading	Throughput assessement vs cluster target + cascading issue? (bake T°)

4- Pre-industrialization		
	R2R Set up	Regulation limits, links, feedback models, effects
	Track recipes naming	track recipe/module recipes and monitoring recipe naming
	Tool matching: illum	Scanner matched illumination
	Tool matching: Focus	Scanner specific focus offset
	Monitoring: inline	Control plan definition CD/Overlay: number of wafers, number of sites, IF sites
	Monitoring: resist	Monitoring resist & BARC (thickness & conta)+ PCM def.
	Alignment Strategy	Revision of best alignment strategy after process/stack stabilisation
	Resist codification	Resist code for procurement; Specifications: water content, solvent content, viscosity or film thickness, metal conta, sensitivity or CD, particle contamination

What Variability is made off ?
What do we see?



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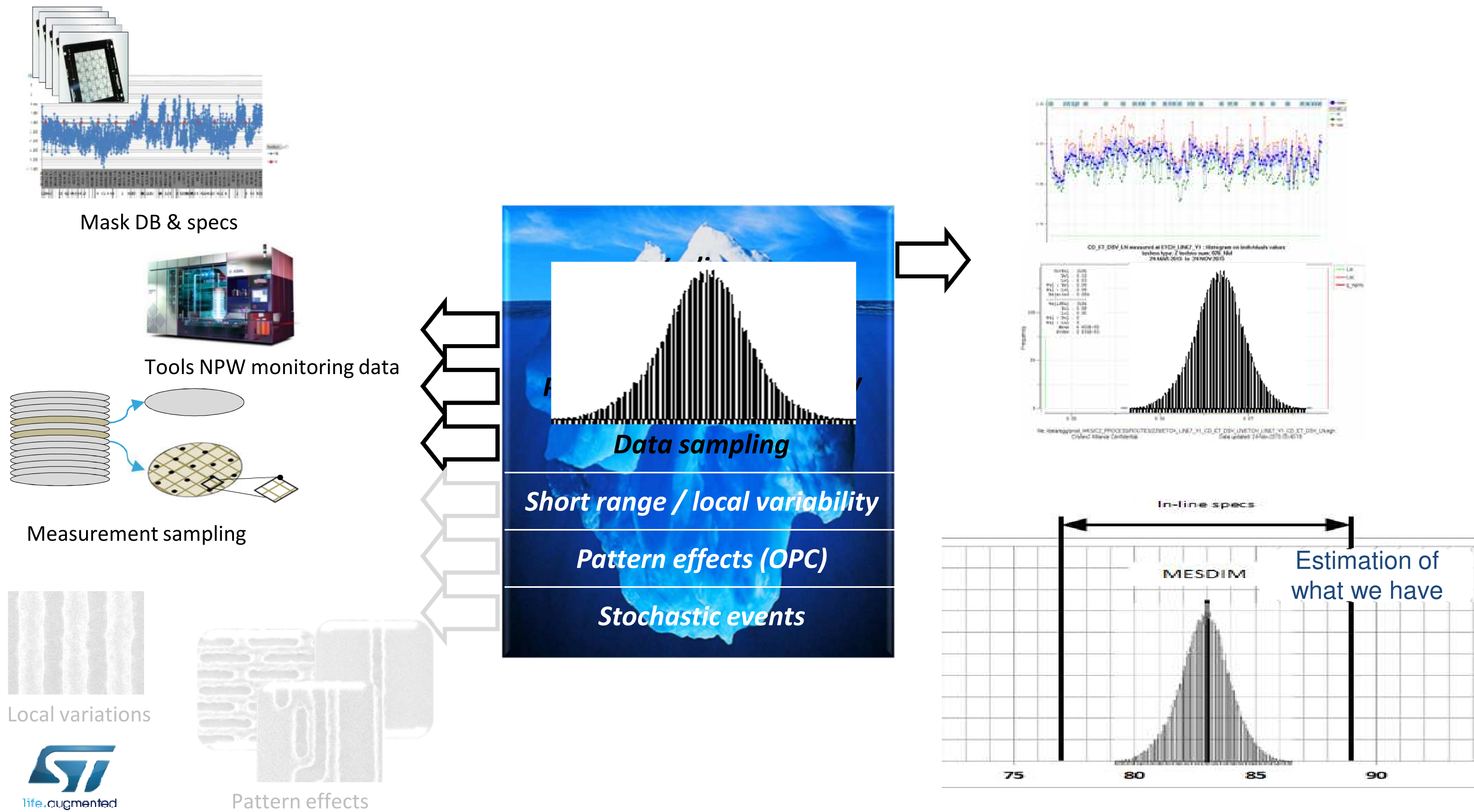
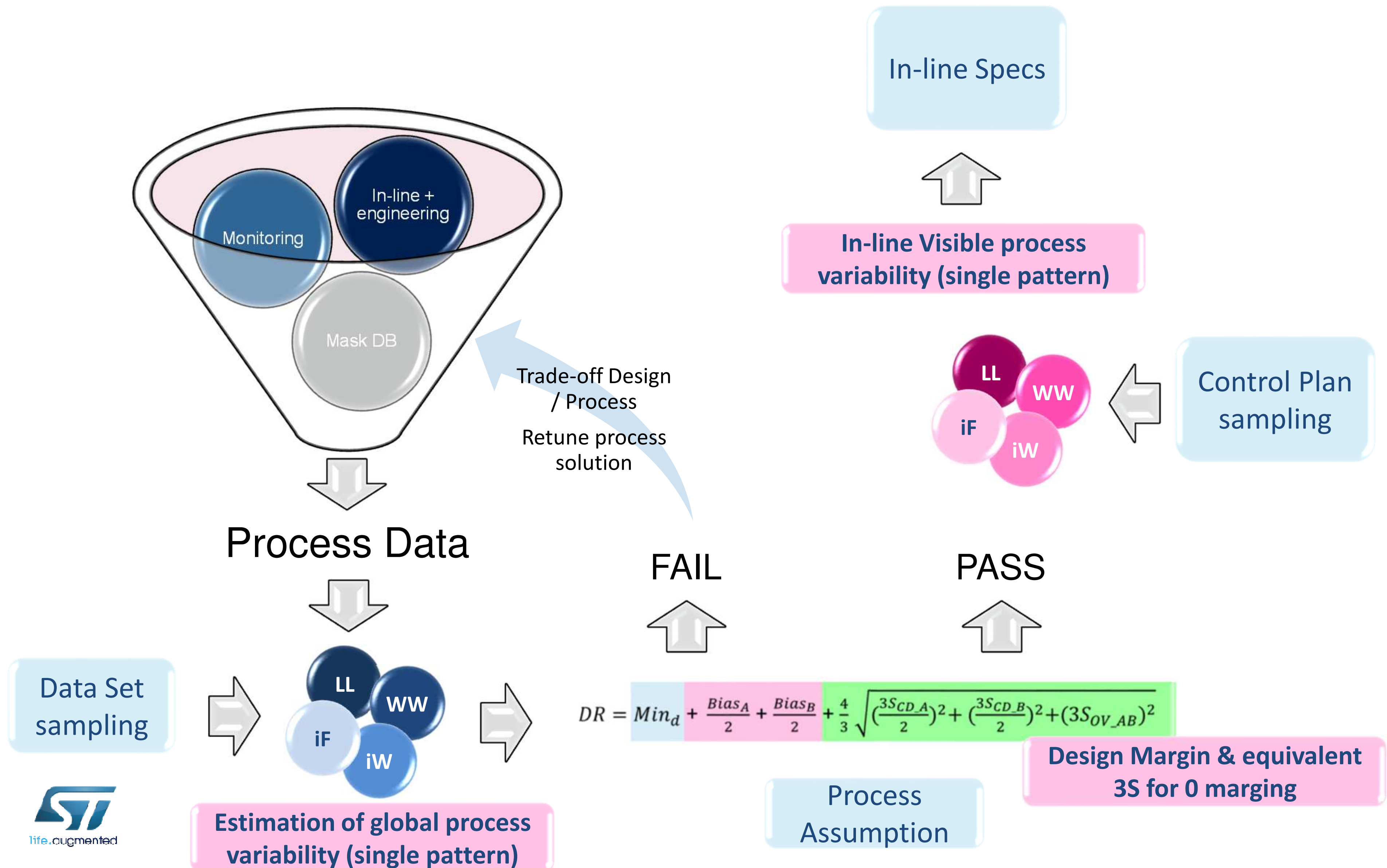


Setting up the Control Plan look beyond



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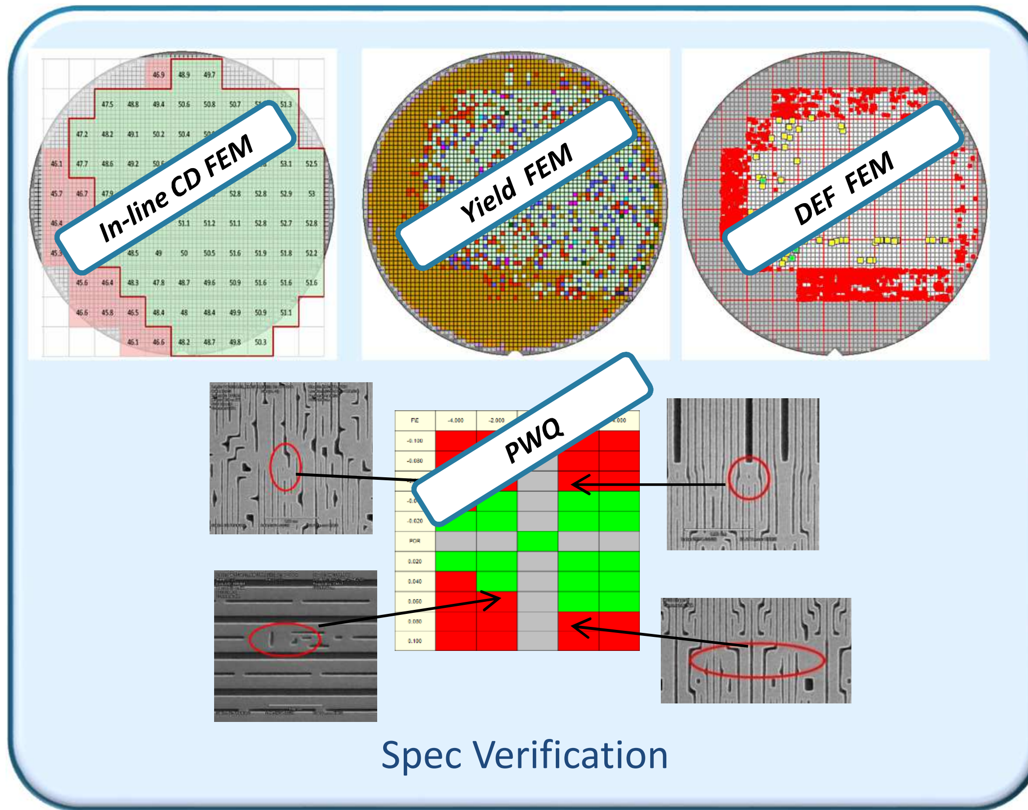
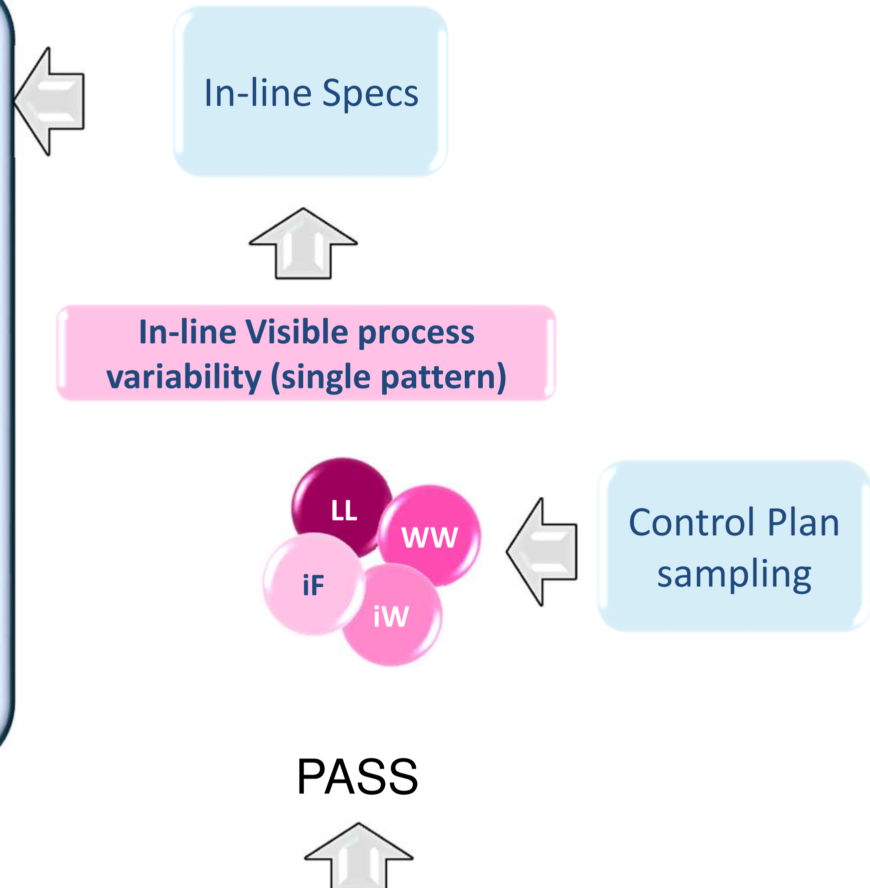
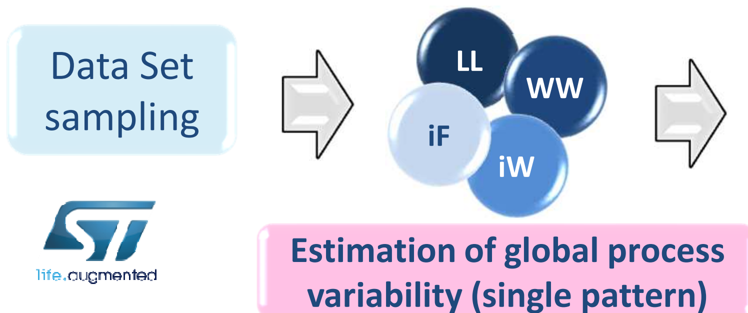




Data Set sampling



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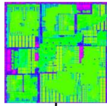
Design Margin & equivalent 3S for 0 marging

Process Assumption

VARIABILITY CONTEXT

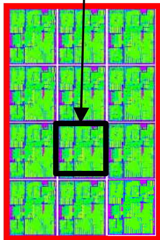
(Expl: 10^7 chips supply – chip size $7x7mm^2$)



✓ **Millions of transistors to make 1 chip.**

- IntraChip variability

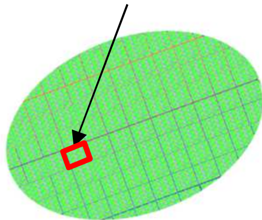
Pattern SHAPE , OPTICAL proximity Effect , Pattern DENSITY effects on ETCHING, POLISHING etc…



✓ **12 Chips per Mask** ***(3x4 chip matrix)***

- Intrafield variability chip to chip

MASK uniformity, SCANNER LENS uniformity, Pattern DENSITY effects on ETCHING, POLISHING etc…



✓ **960 Chips per Wafers** ***(100 Mask exposure 3mm wafer edge exclusion)***

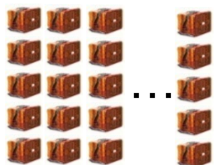
- Intrawafer variability

TOOL PROCESS CHAMBER uniformity

✓ **24000 Chips per Lots** ***(25 wafers per lot)***

- Wafer to wafer variability

TOOL CHAMBERS MATCHING



✓ **10.000.000 Chips is 440 Lots** ***(Waferfab Yield 95%)***

- Lot to lot process variability

TOOL MATCHING, TOOL DRIFT OVER TIME

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Process variability

- ✓ Variability is made of random and systematic signatures
- ✓ Many signatures can be explained through a carefull context management & pre-treatment.
- ✓ Some signatures are clearly systematics and associated to a context
  - They can be wafer to wafer (begin to end batch effect, chamber/chuck matching)
  - They can be intrawafer (process chamber signature, PEB, DEV, Deposition)
  - They can be Intrafield (product induced topography, Mask effects, Lens…)

Parameter	INTRAWAFER	INTERFIELD	INTRAFIELD

Systematics can be treated in APC Feedforward model.

!! Need High density data sampling to generate correction recipes !!
But
moderate sampling to monitor their stability

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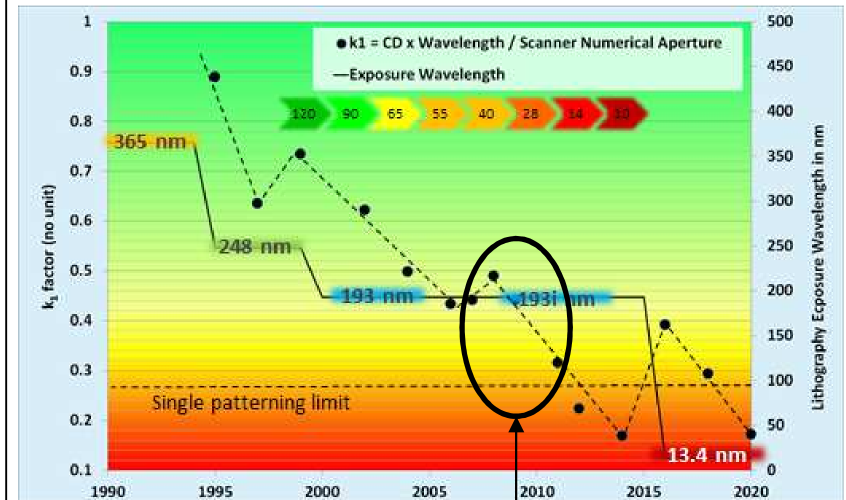
Low k1 lithography = IT

- For advanced technologies, advanced process correction are needed to achieve product specifications:
  - On some context more than 5000 corrections parameters per lot are sent to scanner to adjust Dose, Focus, Leveling, Lens, stage position,…
- To drive and control such type of correction and especially in CR300 High mix Fab context : Advanced IT-Litho system is mandatory
- Such IT/Litho System:
  - Improve and secure Product Performances
  - Minimize impact on Litho Resources
  - Improve Product Turn rate
  - Increase Scanner return on investment



low k1 lithography means.

Intrication Process / Data / IT management.

« Holistic » & « Computational » Lithography

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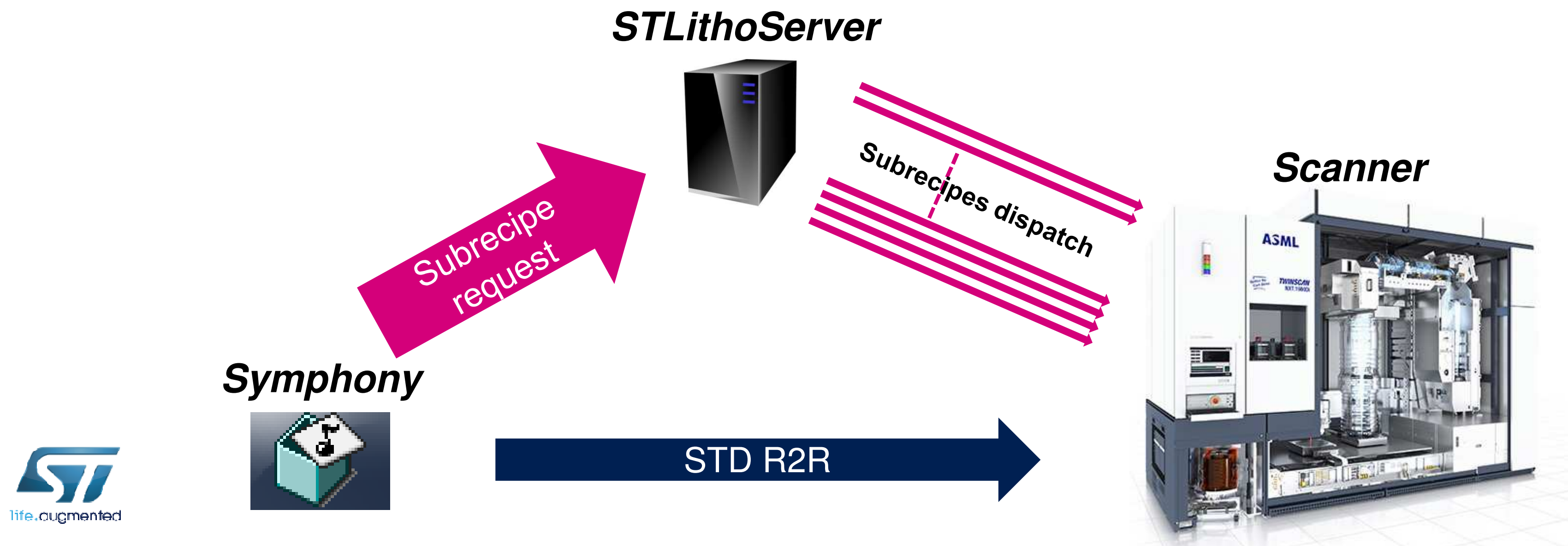
Sub Recipe Management

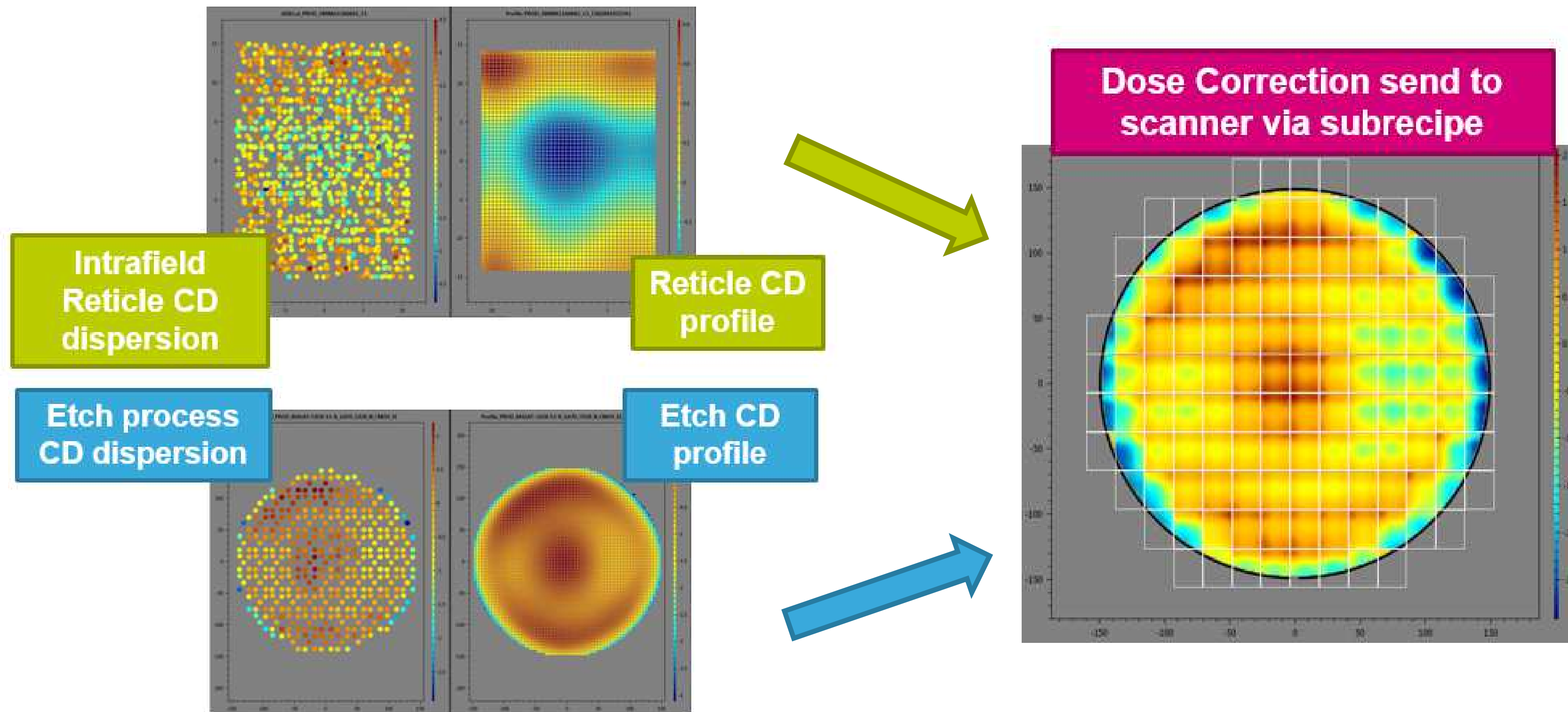
- Currently when a lot is processed @ critical litho process steps
  - > 40 Run2Run parameters are sent by APC to the scanner to expose lot at best condition
  - in addition high order process correction are automatically sent to scanner to correct for current lithographic process error or for non lithographic past or future process step error
    - such advanced process correction named subrecipe are sent to scanner via .xml file
    - each subrecipe file can contain up to 1000 variables to adjust Dose, Focus, Leveling, Lens, stage position,…
    - Up to 10 subrecipes are sent to scanner per lot



Advanced correction type

Dose Mapper

- Dose Mapper (DOMA) subrecipe: Dose Control
  - To Correct for Intrafield CD dispersion linked to reticle writing error
  - To Correct for Interfield CD dispersion linked to etch fingerprint



-Dedicated Correction per lot context
- Static correction

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Advanced correction type

Dose Mapper

IMPORTANT to KNOW:

DoseMapper cannot correct CD gradient > 1% Dose / mm
Dose Correction are clipped at +/- 3% when OPC is used

OBSERVATIONS:

DOMA helps reducing and stabilizing uniformity.
Some product have large Gain some don't.

APC Control — **Intrafield process stabilisation**

Dose Mapper

Intrafield & Intrawafer dose modulation

Scanner Intrafield signature

Etch Chamber signature

Mask Signature

Intrafield CDu (3sigma nm)

IF CDu DOMA

IF CDu no DOMA

APC Control — **IntraWafer process stabilisation**

Dose Mapper

Intrafield CDu (3sigma in nm)

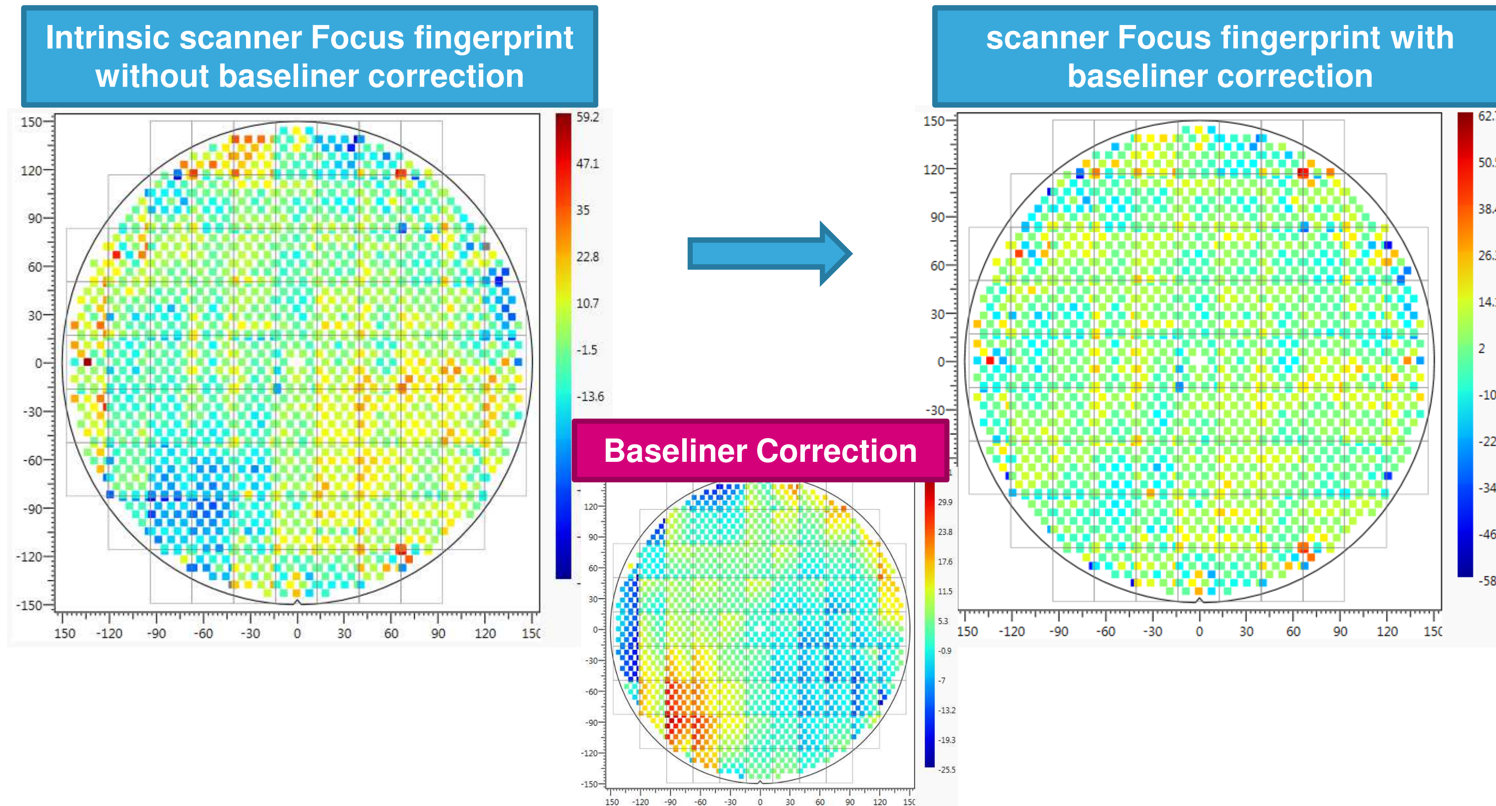
IW CDu with DOMA

IW CDu without DOMA

Advanced correction type

Baseliner

- Baseliner subrecipe: Focus and OVL control
  - To correct for scanner intrinsic focus and overlay fingerprint and drift



-Same Subrecipe Correction on All lots
- Dynamic Correction updated every weeks or after scanner PM

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Advanced correction type

AGILE (level sensor error corrections)

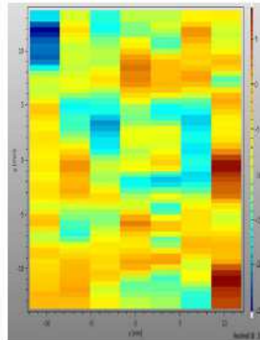
IMPORTANT to KNOW:

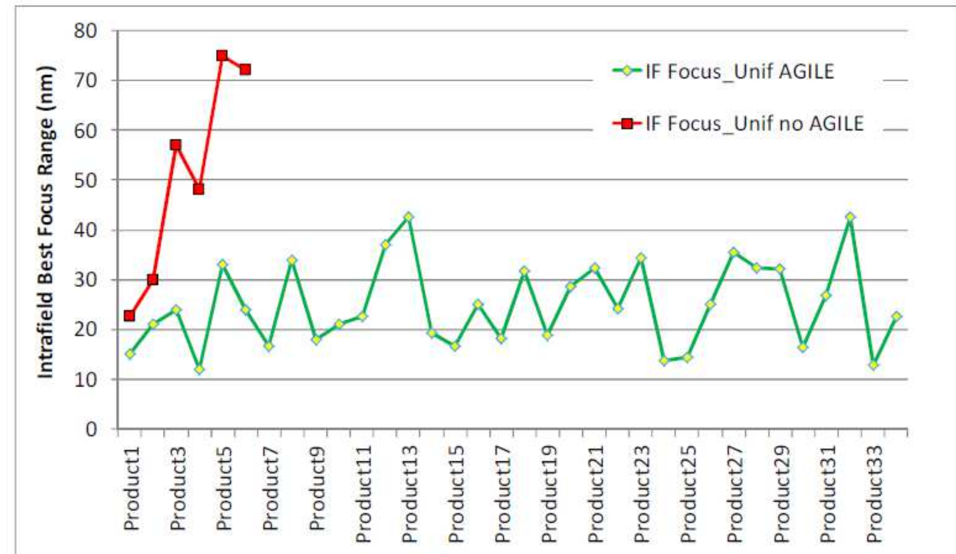
AGILE corrects for optical sensor errors which are stack dependent.
Delta AGILE / lot_n vs lot_ref is constantly monitored to avoid uncontrolled focus shift

OBSERVATIONS:

AGILE helps reducing and stabilizing focus control uniformity.
Some product have large Gain some don't.

AGILE





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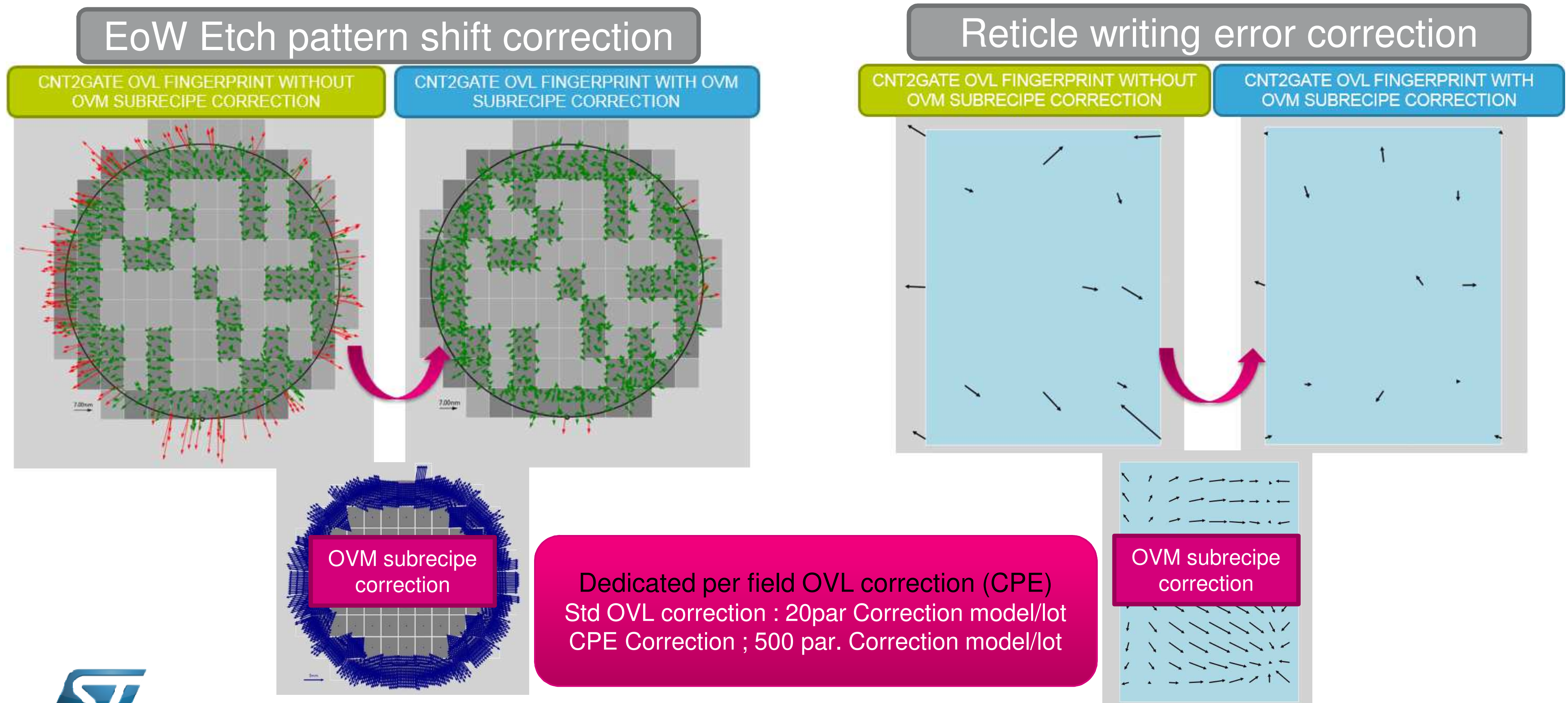
Advanced correction type

OverlayMapper

- Overlay Mapper : OVL control (mandatory for On product OVL spec < 8nm)
  - To correct for Scanner illumination overlay distortion
  - To correct for Reticle to Reticle XY writing error
  - To Correct for non Lithographic process step pattern shift



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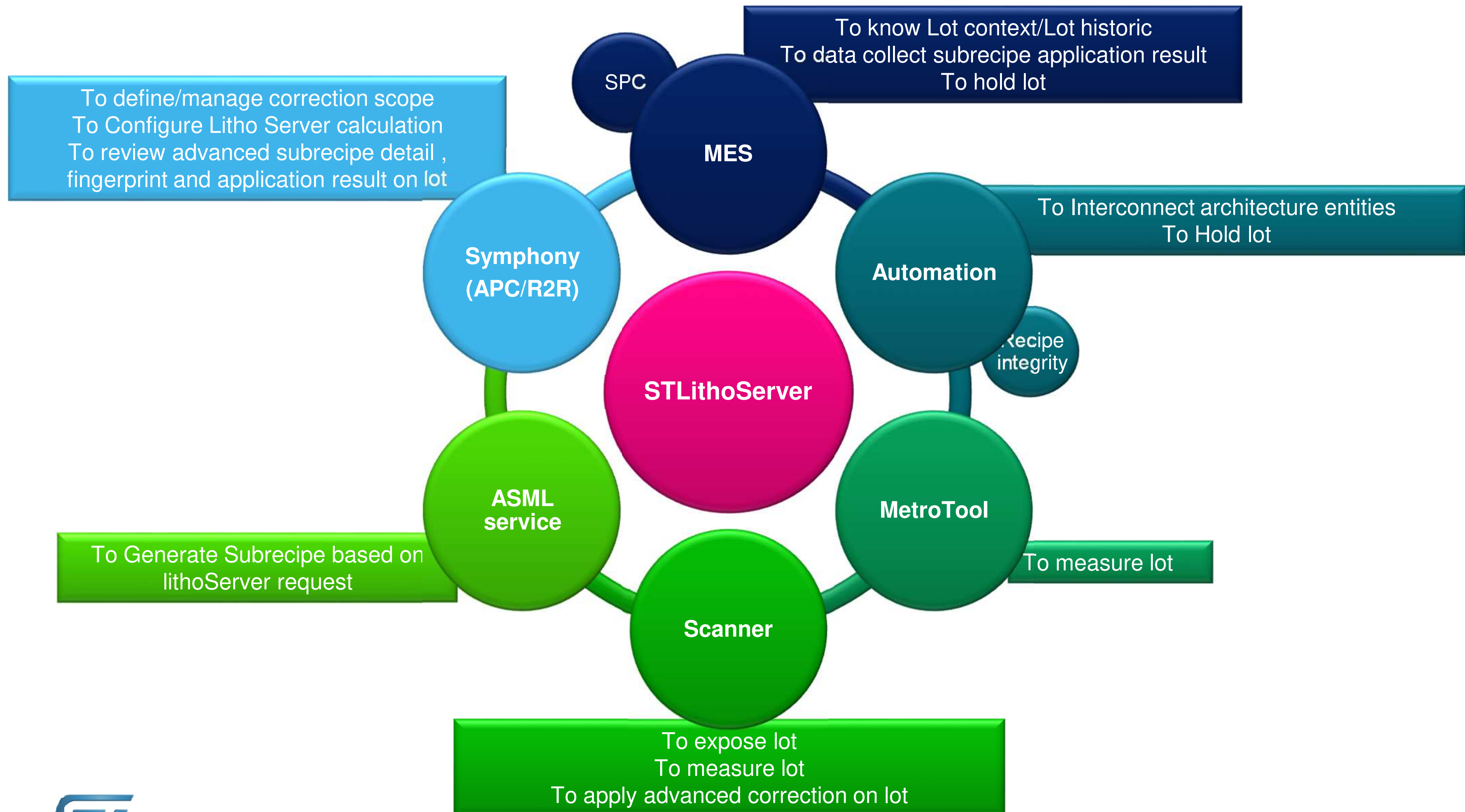
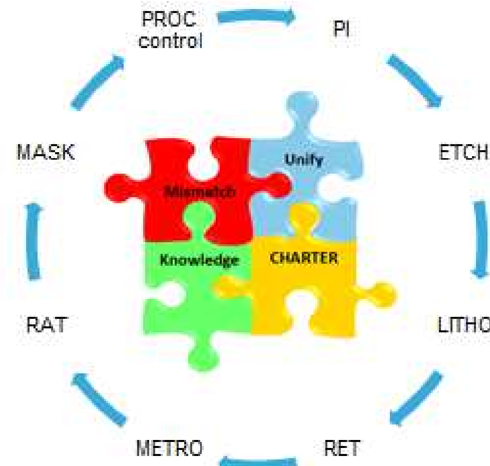
Complex IT Architecture



CONCLUSION



Lot of technologies with their own specificities sharing similar processes

OELECTRONICS
MOORE to MORE than MOORE

A complex system with many « customers »

Choosing best process is not trivial.
Beware copy-paste !!

APHY & PATTERNING
ALLENGES in IC manuf

You can only use the best of advanced tools if you have a proper « IT » infrastructure for Data management

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