MAPPER: High throughput Maskless Lithography

Almut Stegemann

Today’s agenda

- Introduction
- Applications
- Wrap up and conclusions

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Today's presenter

Almut Stegemann

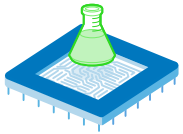
- 06/2014- today working at Mapper
- 2014- 2017 Process Development Engineer for MEMS process
- 2017- today Liasion at Leti to support collaboration projects between Mapper and Leti

Mapper makes e-beam direct write for volume manufacturing possible

Traditional e-beam

1 electron beam
per system

No optical
alignment



No full wafer
placement accuracy

< 25 full 300 mm
wafers per month

Throughput proportional to
pattern density and resolution

+

Lab use only

Mapper FLX

65,000 beamlets
per unit

Compatible, optical,
alignment

Matching to
DUV and 193i

> 450 wafers
per month (300 mm)

Throughput independent of
pattern density and resolution

+

Down to 40nm
logic node

FLX extension

> 1,000,000 beamlets
per unit

Evolution on the same platform

Unit clustering
for >40 wph

>5,000 wafers
per month/unit

It takes minutes only to
expose a wafer at <50nm

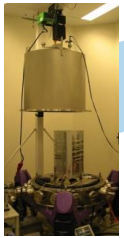
+

28nm logic
node and below

Mapper roadmap

Version: December 2017

Feasibility



Demonstrator

2005 - 2007

Process development

Pre-alpha series

2008 - 2011

Pilot R&D

FLX-1200 series

2012 - 2018

Unique ICs
N40 logic
Spectral filters

Photonics

Capacity ramp-up

65,000bm

III-V

19 wpd

Clustering

FLX-1300 series

2019

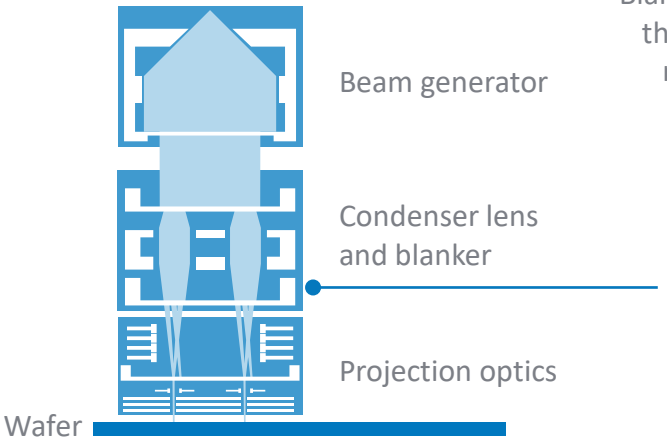
Productivity and CDu

1.6Mbm

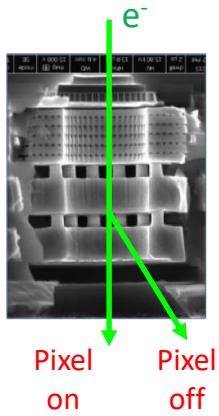
5.2Mbm

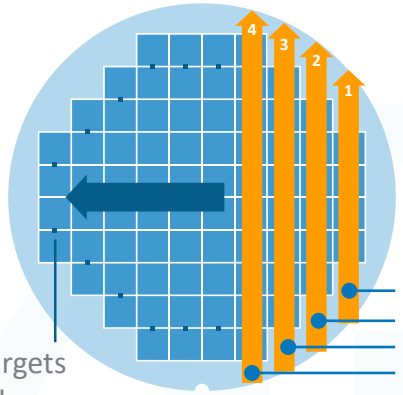
Ultra-advanced logic / cutting

Basic operations of Mapper FLX



Blanker detail: one of many thousands of apertures, made in 65nm TSMC



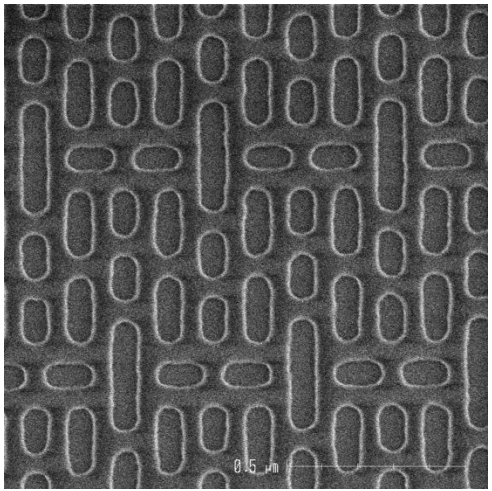


- The electron optics have no central crossovers making them intrinsically insensitive to Coulomb forces (electron repulsion)
- The electron optics are modular and much cheaper than high-NA DUV optics, and can be replaced or upgraded in the field

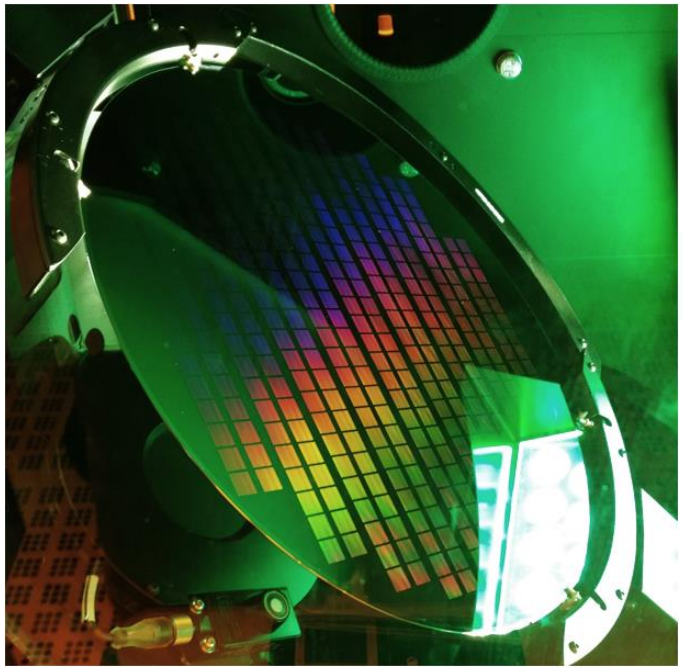
- Wafer exposure happens one column of fields at a time and always in the same direction – no need to meander
- Focus / leveling is performed during stage fly-back to reduce metrology overhead
- Each column of fields is aligned separately, with dedicated alignment targets

Status FLX-1200: full column operational at CEA-LETI as of August 2017

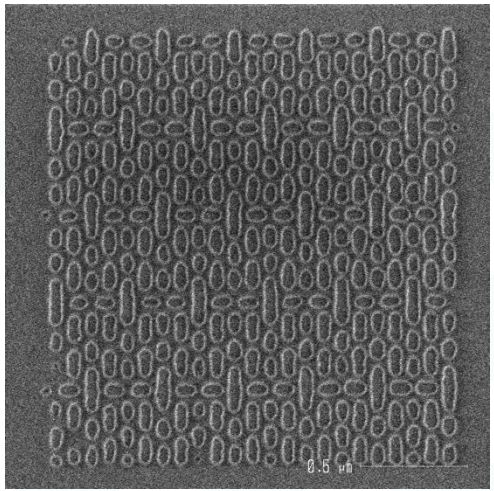
65k beams in 13x2 mm^2 slit. First exposures after upgrade to fully programmable blanker:



60 nm HP (N40)



Getting close to covering a full 300 mm wafer in 60 minutes



40 nm HP (sub N28)

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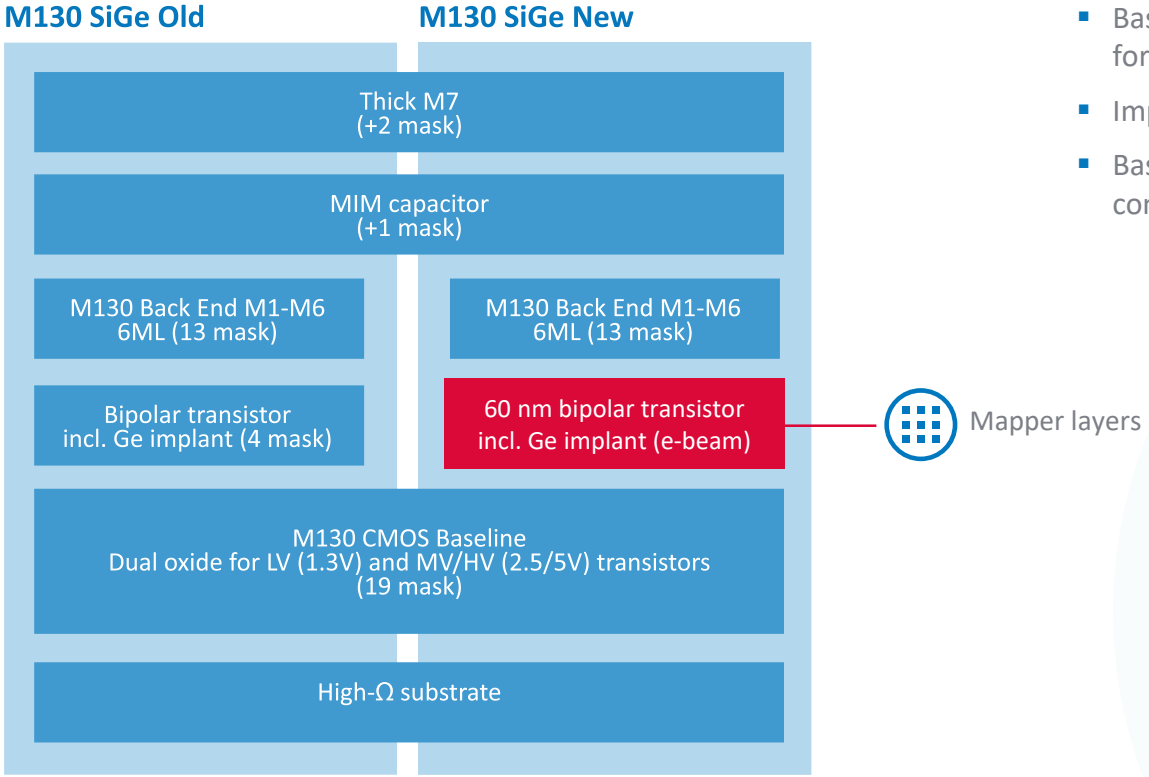
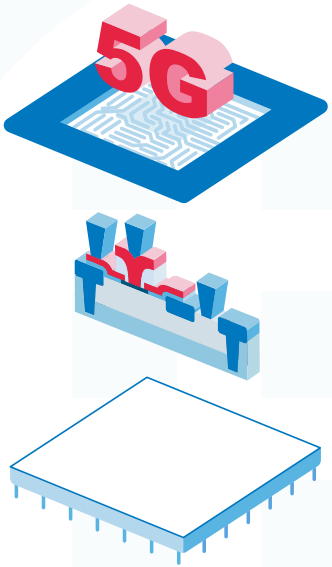
Many different end markets targeted by Mapper

Mapper applications		Tool	Description
Mapper market potential +	I R&D, prototyping and technology evaluation	FLX-1300	▪ Use in research labs/fabs for scientific experiments, prototyping and ultra-small-scale series production
	II Fab capability expansion: Defense and high-security applications	FLX-1300	▪ Use of maskless litho for small-series production (e.g., chip emulation) and to avoid external treatment of design data in mask shops
	II Fab capability expansion: III-V photonics devices & circuits	FLX-1300	▪ Use for producing III-V photonics circuits and passive devices, avoiding mask cost and enabling new device design features that cannot be produced with mask-based lithography
	II Fab capability expansion: Specialty silicon circuitry	FLX extension	▪ Use for small-series products for specialty applications in silicon, as a low-cost replacement of a mask-based system
	III Integrated CMOS sensor optics	FLX-1300	▪ Use for novel optical filters/elements that are directly integrated on top of a silicon CMOS sensor that cannot be produced using mask-based optical lithography
	IV Truly unique ICs: RFID	FLX-1300	▪ Use for 1 layer per chip creating unique, hard-wired ID for RFID tag to be used as trusted root of trust for security applications
	IV Truly unique ICs: Scale-up across applications	FLX extension	▪ Embedding of unique, hard-wired IDs into security chips across different applications and uses (e.g., smart cards, IoT,…)

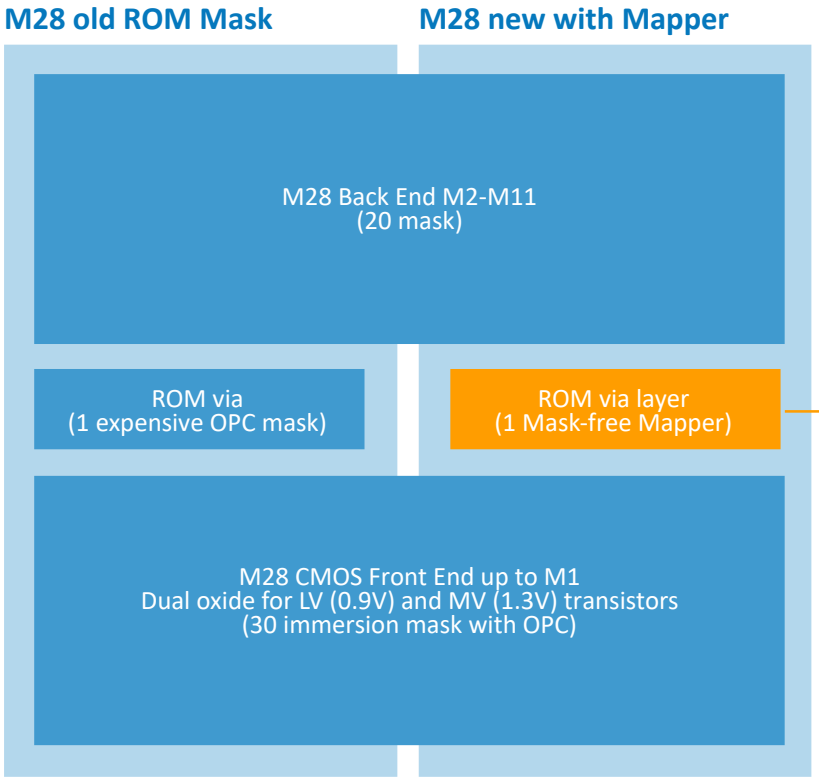
Technology migration with Mapper: <90nm SiGe technology on 8”



- Basic SiGe transistor (and M1) using Mapper for small feature size and (much) higher f_T
- Improved lateral control
- Baseline CMOS and M2-M6 stack keeps using conventional M130 flow



Technology migration with Mapper: ROM and structured ASIC



Mapper layers

Mapper layer replaces very expensive ROM-via programming layer in nodes where Flash is not available

- Classical optical mask very expensive due to closely spaced repetitive via pattern
- Mapper has no problem with these patterns and could even allow smaller ROM dimensions
- Mapper layer has a much faster turn-around time due to 100% software; one day cycles possible
- Eliminate need to add external memory → simpler and lower cost devices

Mapper tool can generate unique pattern for every chip

Data security

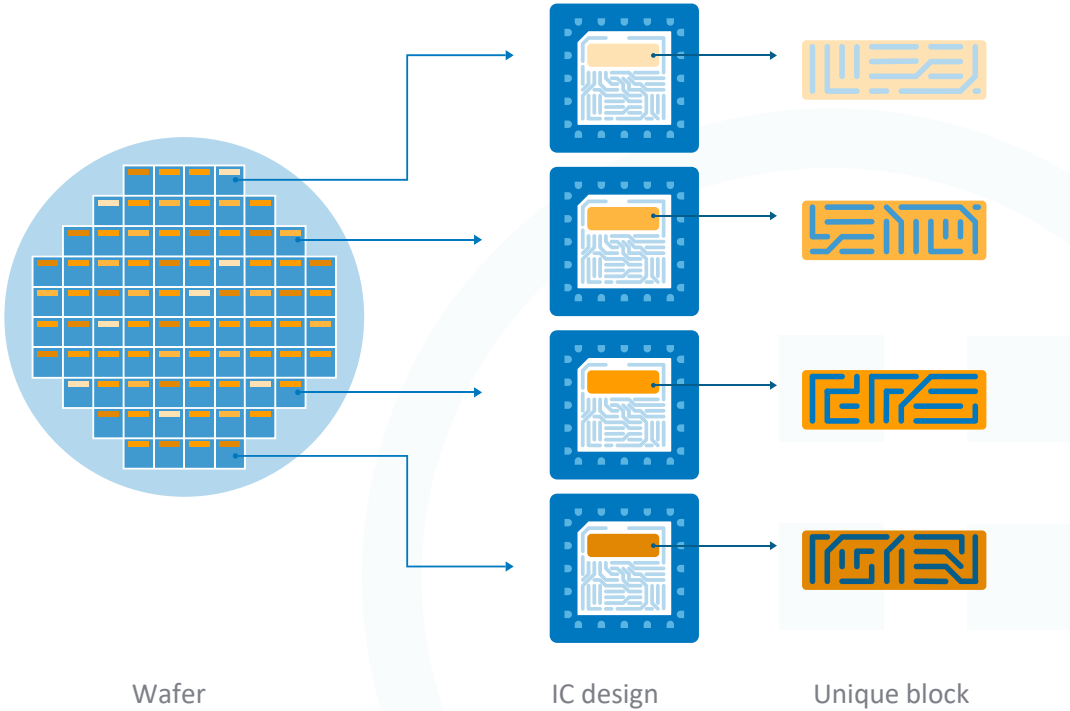
- Industrial infrastructure
- IoT gadgets
- Digital rights management
- Mobile storage
- Smart cards

Traceability

- Automotive
- Aviation
- Medical
- Postal
- Retail

Anti-counterfeiting

- Defense spare IC's for 20+ year old equipment
- Luxury goods
- Bank bills, coins



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Wrap up and conclusions

Roadmap:

- FLX-1300: step in manufacturability, availability, overhead reduction
- FLX-1300: will support various wafer sizes and substrates
- Path to 1.6M and 5.2M beams to improve productivity and CDu

Application highlights:

- Fab capability expansion
- Truly unique IC’s