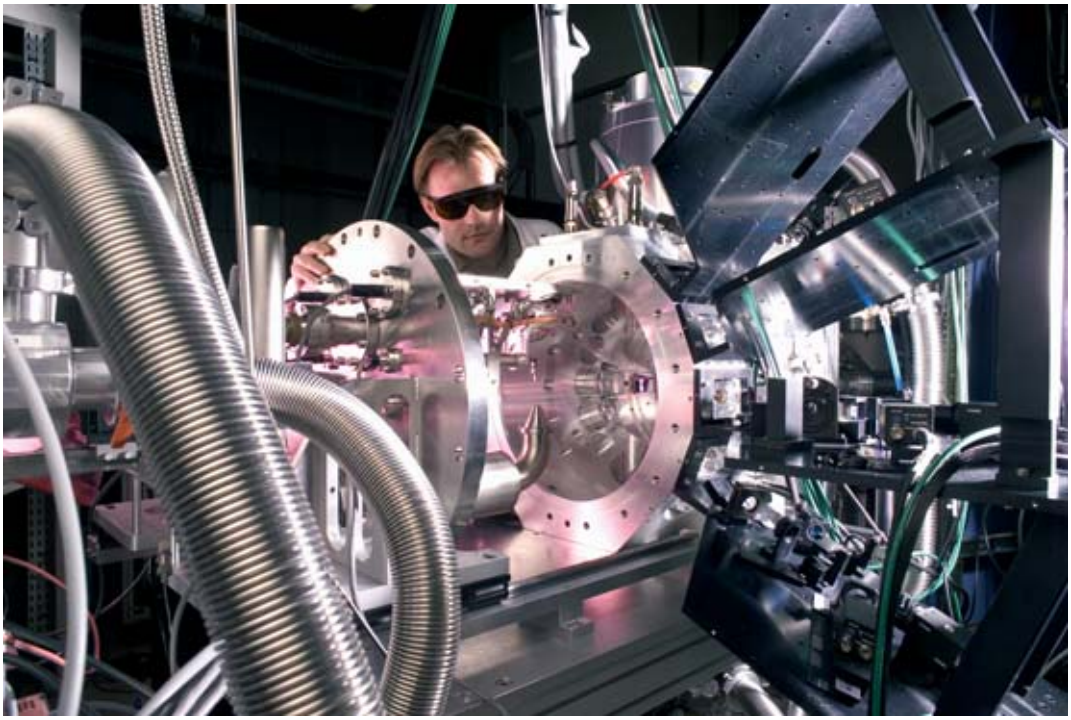
# Extreme ultraviolet lithography: towards even finer-featured circuits

Achieving nanometre-scale patterns able to process even more information is a constant challenge for the microelectronics industry. One very promising research direction that the CEA has committed to is the use of extreme ultraviolet light (EUV). The goal, set for 2010, is to develop lithography technology capable of etching patterns at ultra-short wavelengths (32 nanometre feature size).



A. Gonin/CEA

At CEA Saclay, setting up a laser-produced plasma EUV source developed by the Exulite consortium. Six laser beams focus onto a glass microbead simulating a xenon micro-jet, inside an experimental vacuum chamber.

The spectacular progress made in optical **lithography** (Box E, ***Lithography, the key to miniaturization***) made over the last two decades has led to considerable scaling-down of pattern feature-size etched into **silicon**, thereby boosting the performance of **integrated circuits** (IC). The number of **transistors** on today's Pentium 4 has been multiplied a thousand-fold since the Intel 80286 PC/AT, one of the first office computers to be put on the market back in the 1980s. Few people at that time were aware of the technological progress implied by the predictions of Gordon Moore, co-founder of Intel Corp. (see the box in *From microelectronics to nanoelectronics*), who stated that the number of IC transistors was expected to double every 18 months. If current microelectronics industry forecasts are true, "Moore's law" is set to hold strong for several years to come. In the meantime, microelectronics has also become a major factor in economics. Market demand is driving the miniaturization of IC structures towards further-enhanced performance, while prices have fallen dramatically. In 1973, a million transistors would have cost the price of a house (€ 76,000), whereas now they wouldn't cost so much as a Post-It® (€ 0.004).

This staggering progress stems from an ever-smaller pitch size. One of the main factors underlying this technological process is the use of light sources with shorter wavelengths within the device, called a photo-stepper, used in optical lithography. **Feature-size**-enhancement techniques have even led to patterns being achieved at well below the wavelengths used: current ultraviolet-enabled laser technology used at 193 nm wavelength can pattern down to 110 nm in high volume production (HVM).

New lithography technologies have attracted huge investment, and ROI dictates that the technology needs to remain economically viable for a relatively long period of time. This is why the 157 nm wavelength step was recently just straight dropped. The sector has elected to push on with 193 nm technology, but incorporating a new optical innovation (see *From microelectronics to nanoelectronics*). This development nevertheless remains compromised by the technological means used. The whole sector, across the board, would prefer to work in a similar situation to the 1980s where feature size was greater than the wavelengths used, whereas the

industry is looking to develop lithographic technology that in 2010 is expected to be capable of working down to 32-nm-scale, or further.

## EUVL, first and foremost optical business

Along these lines, then, various industry actors such as ASML in Europe, Nikon and Canon in Japan, and Intel in the US, have proposed to use extreme **ultraviolet** lithography (EUVL) operating at a wavelength of 13.5 nm(1). EUVL is considered today's top option for reaching this objective. The advent of EUVL represents both real continuity and a revolutionary step forward. On one hand, it is an optical-based lithography able, as before, to incorporate a range of known enhancements and adjustments to further reduce pattern size. On the other, it incorporates totally novel technology: the process has to be performed entirely under ultra-high vacuum , as practically all matter, even gases, absorbs light at 13.5 nm. This means doing without the refractive lenses of the previous stepper systems, and using a reflective mask and optics, extremely high-precision mirrors. Even more radical, the light source will no longer be laser but a hot **plasma** created from a tiny volume of material (xenon, lithium or tin). This light source is a crucial element in whether EUV lithography becomes a success. Figure 1 shows how an EUV stepper system works.

## The CEA and laser source

The advent of EUV lithography represents a huge technological challenge taken on by sector leaders throughout the hi-tech world (Japan, the USA and Europe). The CEA already boasts several years of investment in EUVL-targeted R&D projects, starting by the French national Preuve project (part of the RMNT – Micro- and Nanotechnology Network) launched by the CEA-Leti (Electronics and Information Technology Laboratory: Laboratoire d'électronique et de technologie de l'information) in late 1999, and completed in August 2002. Three CEA clusters took part in this project: the Technological Research Division, as lead contractor for Europe's first EUV lithography machine, and the Military Applications and Materials Science Divisions which each developed a 13.5 nm plasma source. Following on from this success, several Europe-wide projects(2) were launched under MEDEA+ focusing on masks, sources and photoresist processes for EUVL (see *Resists and masks, the other crucial components of EUVL*). To round up, a project called More Moore was launched in 2004 as part of the 6th FPRTD, and the Leti is playing its role.
The CEA's work on sources includes research under the French Exulite project, which aims to engineer a laser-produced plasma (LPP) EUV source. The cost and performance targets set for plasma sources are highly ambitious. Effective power output at 13.5 nm

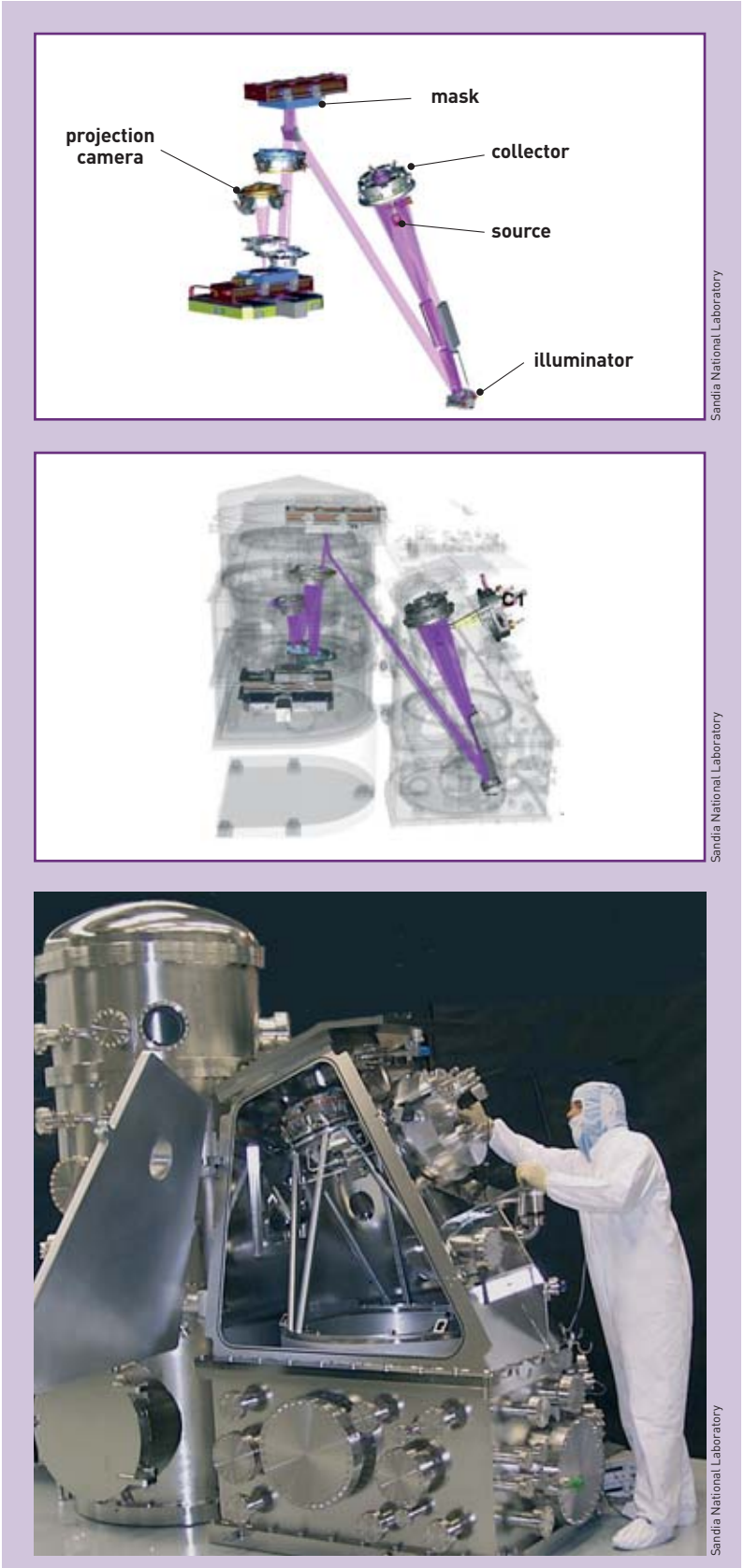



Figure 1.
The first prototype of an EUV lithography machine was built in 2001 at the US-based Sandia National Laboratory, as part of the EUV-LLC project. The top diagram shows the optical path of an EUV beam from the source through the collector, then the mask illuminator, the mask, the projection camera, and finally to the silicon wafer. The middle scheme shows how the optical system is integrated into a vacuum chamber split into two sections, with the "source" on the right and the "projection optics" (P.O. Box) on the left. The bottom illustration shows the Engineering Test Stand (ETS) prototype of the first experimental EUV lithography apparatus built at the US-based Sandia National Laboratory.

(1) A joint agreement set the wavelength at 13.5 nm to optimize the reflective capacity of the Mo-Si multilayer optical coatings.

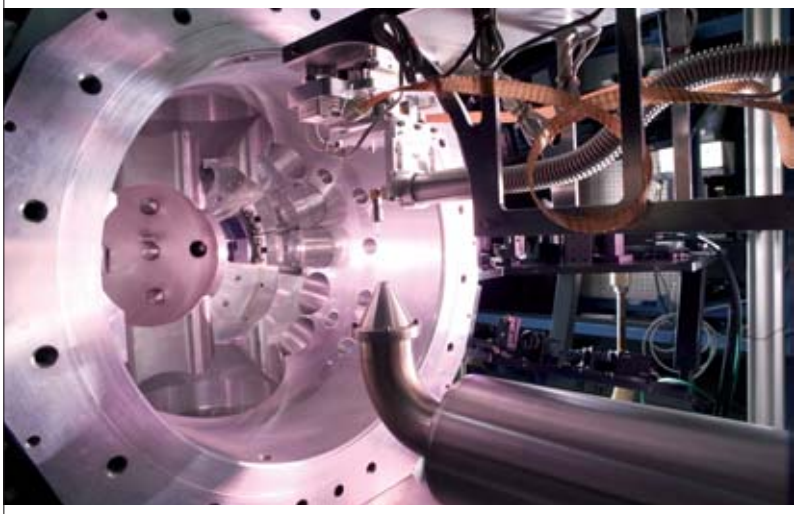
(2) (Extumask T404 - DRT/Leti), on sources (Exulite T405 - DEN/DPC/SCP and DSM/Drecam/Spam) and photoresist processes for EUVL (Excite T406 - DRT/Leti).

within a very narrow spectral window of 0.27 nm has to reach 115 W. The point source diameter has to stay at 1 mm or less in order to collect the EUV light. These are figures that take us to the limits of physics, signalled by a **black-body** heated to around 350,000 kelvins. This is the kind of power level that is required, as only a small fraction of light created by the source actually reaches the silicon wafer, as illustrated in Figure 2. This is due to the fact that EUV light is inexorably absorbed during its journey through the photo-stepper as it travels through the source collector, the mask illuminator, the mask, and finally the projection camera.

To top it all off, the source has to turn in exceptional reliability with a 30,000-hour lifetime, and run at a minimum repetition rate of 7 kHz. The conversion efficiency of the EUV light source has to be optimized to keep thermal load on the vital source components to a minimum. Of the two plasma source concepts that are being developed worldwide, the CEA has opted for laser-produced plasma (LPP) over discharge-produced plasma (DPP)(3). LPP does carry the disadvantage of being more sophisticated and at higher cost, but in comparison, the use of a DPP source in a manufacturing setting is hampered by pollution and thermal load complications.

Within the pan-European MEDEA+ T405 project coordinated by the Germany-based firm Xtreme Technology, the Exulite consortium is harnessing the research effort led in France. The CEA is working in close partnership with Alcatel Vacuum Technology/Adixen and Thalès Laser to produce a feasibility prototype called ELSA/C (EUV Lithography Source Apparatus/Cw), with financial backing from the French Ministry of the Economy, Finance and Industry. Completed in late 2005, ELSA/C is expected to deliver an effective EUV capacity of several watts at a repetition rate of 10 kHz. The installation was put together in a laboratory shared by the CEA's Nuclear Energy and Materials Science Divisions, the first managing the optical technology (using lasers initially developed for uranium enrichment based on Atomic Vapour Laser Isotope Separation – SILVA project) and interfacing with the source chamber, while the second is charged with integrating the source chamber housing the liquid xenon target.

The modular structure design has incorporated six identical 500 W lasers all aligned to a single focal spot



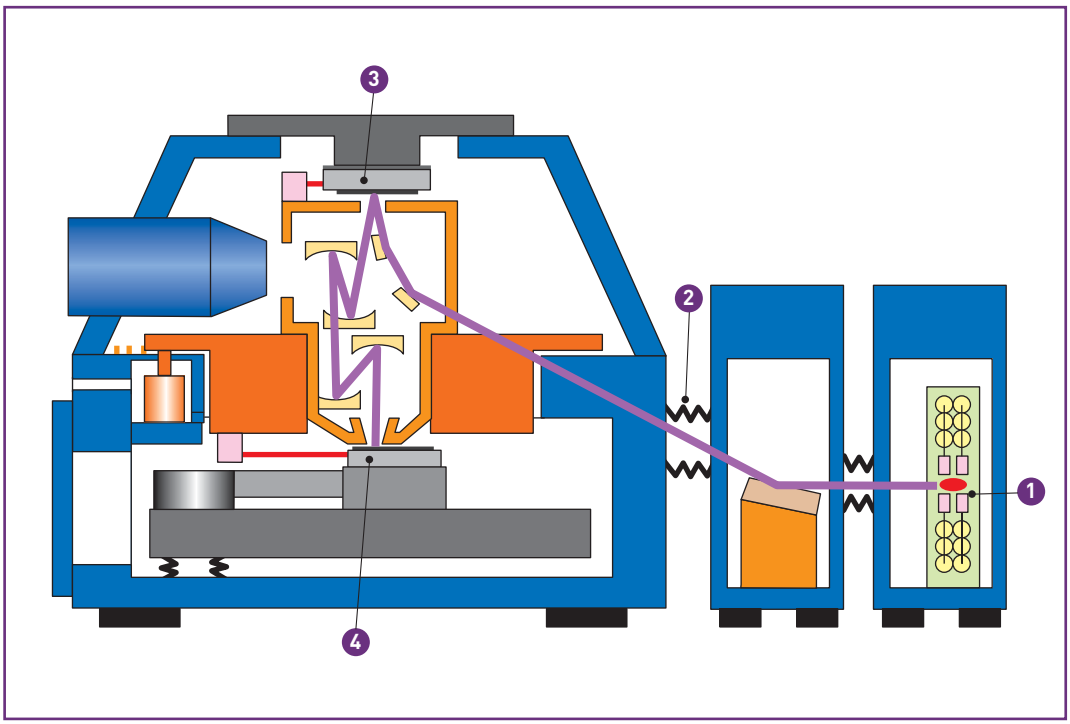
A. Gonin/CEA

At CEA Saclay, inner part of the experimental vacuum chamber of the laser-produced plasma EUV source developed by the Exulite consortium.

(3) The two source types currently under development are mainly differentiated in their excitation and heat-up mechanisms of the emission plasma. Laser-Produced Plasma sources utilize high-intensity pulsed lasers focused on a dense target, whereas Discharge-Produced Plasma sources are based on intense electrical discharge in a moderately dense gas.

(4) Cryogenic: its literal meaning is "producing cold"; by extension, means "related to low temperatures".

(5) rms (Root-Mean-Square): average square root of a set of numbers: method for giving a better statistical measurement of the calculated average of several variables.




Xtreme Technology (Germany)

Figure 2. Illustration of the progressive drop in luminous intensity at 13.5 nm in an EUVL stepper. The 1,600 W power at source ❶ drops to just 115 W at the intermediate focal point ❷ located between collector and illuminator, then 6.1 W at the mask ❸ and only 0.321 W at the wafer ❹. This example is for a discharge-produced plasma (DPP) source. A laser-produced plasma source gives better performance due to the improved EUV beam collection making it possible to reduce the initial source power to 500 W.

on the liquid xenon target (Figure 3). This modular approach offers several advantages: laser power can be upgraded, and development and maintenance costs can be cut. Single module power may eventually reach 2 kW. Therefore, coupling 10 to 20 laser modules would make it possible to inject several tens of kW of laser power onto the target to obtain the required EUV power. The source architecture was designed based on a fully comprehensive functional analysis to define all the source sub-assemblies: cooled vacuum chamber carrying the cryogenic[4] xenon target, the target injection system, the xenon pumping and recycling system, laser beam transport and focusing units, EUV collector, and the overall command and control system.
This modular approach also offers another, decisive advantage stemming from the ultra-precise dose control of the EUV on the silicon wafer. A breakthrough technique developed by the CEA enables stable EUV dose control to 0.1% rms[5]. The solutions package developed by the CEA has been protected by several patents.

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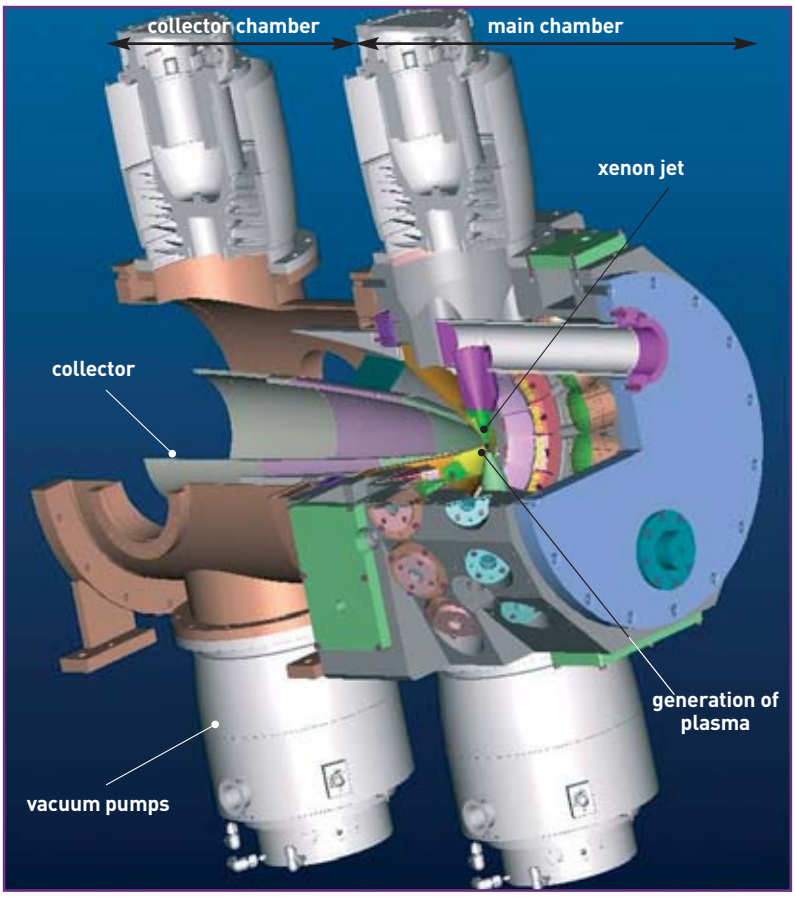



Figure 3.
The ELSA/C (EUV Lithography Source Apparatus/Cw) source built by the Exulite consortium at CEA Saclay. On the right, the source chamber with cryogenic xenon jet, and on the left, the grazing incidence mirror for collection. The top and bottom cylinders are magnetically levitated (maglev) turbo vacuum pumps.

# Resists and masks, the other crucial components of EUVL

In addition to source, extreme UV lithography requires cutting-edge research and testing of two other components: the photoresists and the masks carrying the circuit patterns.

The underlying mechanism behind the resists used prior to the introduction of **Deep-UV** (DUV) photolithography was based on direct photosensitivity: each **photon** induces a single, unique photochemical reaction modifying the dissolution behaviour of the resist in the developer. The shift towards DUV lithography and now extreme ultraviolet **lithography** (EUVL) brought with it an increase in photon energy, and as a result, a decrease in the number of photons needed at a particular exposure dose. In order to maintain the same efficiency in terms of hourly wafer throughput, a new concept was put forward, based on *Chemical Amplified Resists* (CAR) comprised of a **polymer**, a PhotoAcid Generator (PAG), and various additives. Under DUV exposure (Figure 1), the PAG releases an acid, thereby creating a latent mask pattern in the resist, but without modifying the dissolution characteristics.

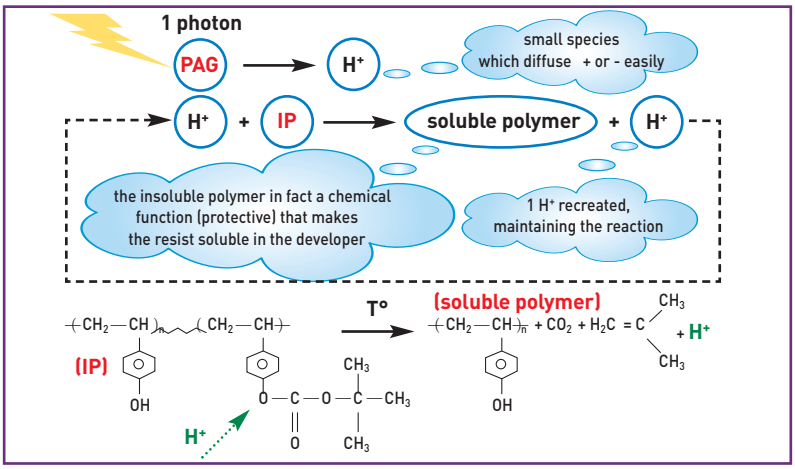
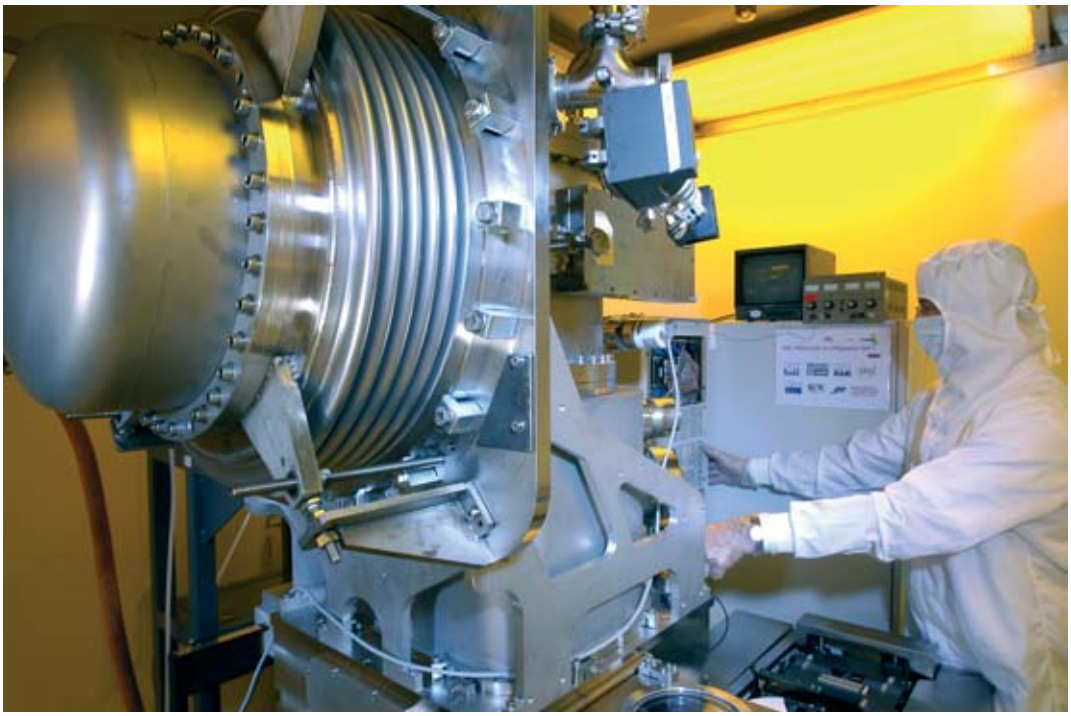



Figure 1.
"Deprotection" principle of a chemical amplification resist
insoluble polymer (IP) + solvent + photoacid generator (PAG) + other components.



Experimental EUV lithography bench (BEL) in testing at the CEA Grenoble. The EUV source has not been installed.

Artechnique/CEA

A second process, called Post-Exposure Bake (PEB), triggers an acid-**catalyzed** deprotection reaction, where an acid molecule is regenerated at each deprotection reaction, going on to probably deprotect another site following diffusion in the resist film. This reaction, which is mistakenly called chemical amplification, increases thermally the dissolution properties of CAR. Over and above the capabilities of lithography hardware, the **resolution** limits of CAR are closely related to the diffusion properties of the acid in the resist film. These properties control the Critical Dimension (CD), Line-Edge Roughness (LER) and Line-Width Roughness (LWR) of the UV-generated patterns in increasingly small resist films.

| node (≈ CD) | 45 nm | 32 nm | 22 nm |
|---|---|---|---|
| resist thickness | 90-160 nm | 65-110 nm | 45-80 nm |
| Line-Width Roughness (LWR) | 2 nm | 1.4 nm | 1 nm |
| PEB sensitivity | 1.5 nm/°C | 1 nm/°C | 1 nm/°C |

Table.
Photoresists criteria according to the International Technology Roadmap for Semiconductors (ITRS).

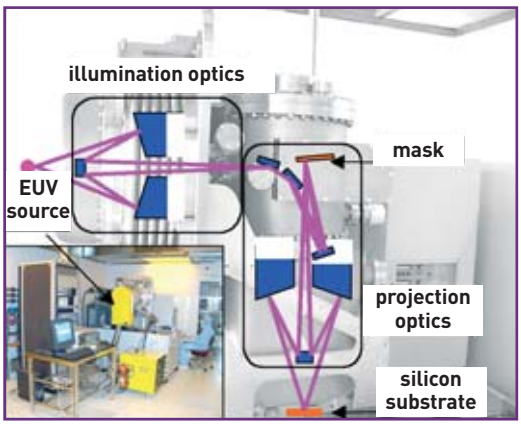



Figure 2.
EUV lithography testbench (BEL) at the CEA-Leti, Grenoble.

## Challenges in next-generation lithography

The criteria set out by the ITRS (International Technology Roadmap for Semiconductors), which are technological bottlenecks that absolutely must be overcome (see the table and *From microelectronics to nanoelectronics*), also represent research orientations for the CEA-Leti. The CEA has set up an EUV research platform to meet these challenges. The platform is designed around a tool that is one-of-its-kind in Europe, the BEL (Lithography testbench) installed as part of the Preuve programme, a research consortium grouping major French actors including industrial manufacturers, start-ups, public research institutions and universities. It is a step towards the development of next-generation lithography for advanced microelectronics, aiming specifically at fabricating submicron-scale circuits (below 32 nm).

The BEL (Figure 2) is installed in ultra-clean facilities at the Grenoble CEA-Leti. There are four main components: the EUV source, the illumination system (comprising a EUV collector optics system and a filter maintaining the spectral band at 13.5 nm), the projection system (comprising mask, projection optics and substrate-targeting system), and the photoresist coated substrate receiving the exposed patterns.

Having a fully-operational BEL in an EUV lithography platform has enabled the CEA and its partners to team up on research development projects, driving their leadership on major tasks in several Europewide programmes: MEDEA+ Excite, MEDEA+ Extumask, IST More Moore.

The utilization of extreme ultraviolet wavelengths introduces technological breakthrough, requiring a full ultra-high vacuum system with all the mask and optics components operating in reflective mode. Perfect control of mask production is one of the most critical issues, as confirmed at the last international EUV lithography symposium held in November 2004. This is doubly the case for the production of "zero-defect" masks.

Figure 3 shows how a mask is built. For several reasons, EUV masks require major technological advances on the current standard masks used in production today. First off, EUV mask substrates need to reach 10 to 100-times higher-quality polished smoothness: the main target qualities are flatness, perfectly-parallel surface alignment, and a defect-free mask after the operation. EUV masks which work by reflection require mirror at 13.5 nm. This mirror (Figure 4) is a multilayer interference system (Bragg mirror), where the most critical issue is producing a multilayer deposit with an extremely low defect count ($10^{-3}$ defects per $cm^2$).

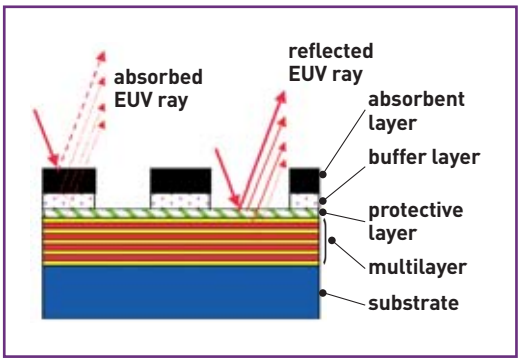



Figure 3.
Diagram of a EUV mask.

Lastly, the mask patterns have to be produced at a feature size of at least 120 nm (*patterning* of the absorbent layers) to generate feature sizes of 32 nm at the wafer, since the optics system leads to a pattern reduction of magnitude 4X.
Metrology techniques for inspecting the masks (multilayer mirror reflectivity at 13.5 nm, checking for size defects down to 50 nm) have been specially developed for use with EUV masks.

## The role of the CEA

The CEA-Leti is conducting studies on mask depositing processes together with advanced technology development measurement tools for multilayer defects. Defects occurring in the multilayer stacking of EUV masks are well known to be initiated from either nodules growth (intrinsic defects) or extrinsic defects caused by the depositing process. In the process used at the CEA-Leti, each of these defect groups is roughly responsible for half of the total defects observed, with extrinsic defects generally over 175 nm while intrinsic defects are between 90 and 120 nm, giving a total defect density of 0.9 defects per $cm^2$ at Ø > 90 nm. These figures highlight that the current process has reached its limits, and that a technological breakthrough is needed. The Leti is ready to propose a novel *in situ* extrinsic defect elimination system.

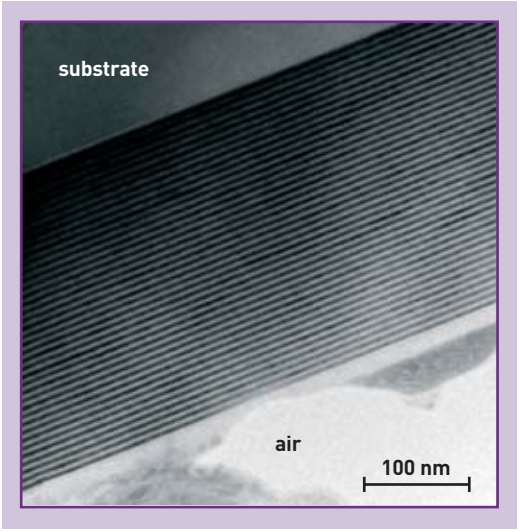



Figure 4.
EUV mask: transmission electron microscope image of a 40 layer pair Mo(3 nm)/Si(4 nm) multilayer.

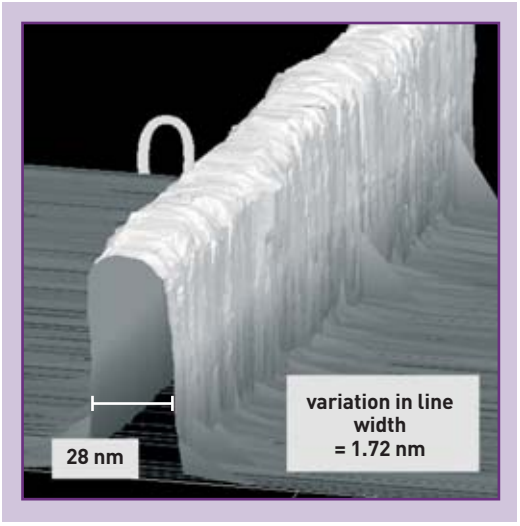



Figure 5.
3D AFM image of an illuminated resist line.

The CEA's mask and resist research activities are underpinned by significant advances in metrology techniques, which themselves are the target of a major research effort. In 2004, the Leti set up a Resists Expertise Centre to study the physicochemical properties of photoresist.
Since we are dealing with dimensional metrology, 3D analysis metrology products such as Veeco's in-line 3D AFM are being drafted in to give qualitative and quantitative analysis of geometric variables such as CD, profile or line roughness (Figure 5). Finally, the Comnet EUV mask blank defect counting tool can be run on 200 mm silicon wafers to detect defects of 80 nm.

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# E Lithography, the key to miniaturization

Optical lithography (photolithography) is a major application in the particle-matter interaction, and constitutes the classical process for fabricating integrated circuits. It is a key step in defining circuit patterns, and remains a barrier to any future development. Since resolution, at the outset, appears to be directly proportional to wavelength, feature-size first progressed by a step-wise shortening of the wavelength λ of the radiation used.

Artechnique

Photolithography section in ultra-clean facilities at the STMicroelectronics unit in Crolles (Isère).

The operation works via a reduction lens system, by the *exposure* of a photoresist film to energy particles, from the ultraviolet (UV) photons currently used through to X photons, ions, and finally electrons, all through a mask template carrying a pattern of the desired circuit. The aim of all this is to transfer this pattern onto a stack of insulating or conducting layers that make up the mask. These layers will have been deposited previously (the *layering* stage) on a wafer of semiconductor material, generally silicon. After this process, the resin dissolves under exposure to the air (*development*). The exposed parts of the initial layer can then be etched selectively, then the resin is lifted away chemically before deposition of the following layer. This lithography step can take place over twenty times during the fabrication of an integrated circuit (Figure).

In the 1980s, the microelectronics industry used mercury lamps delivering near-UV (g, h and i lines) through quartz optics, with an emission line of 436 nanometres (nm). This system was able to etch structures to a feature-size of 3 microns (μm). This system was used through to the mid-90s, when it was replaced by excimer lasers emitting **far-UV** light (KrF, krypton fluoride at 248 nm, then ArF, argon fluoride at 193 nm, with the photons thus created generating several electronvolts) that were able to reach a resolution of 110 nm, pushed to under 90 nm with new processes.

In the 1980s, the CEA's Electronics and Information Technology Laboratory (Leti) pioneered the application of lasers in lithography and the fabrication of integrated circuits using excimer lasers, and even the most advanced integrated circuit production still uses these sources.

The next step for high-volume production was expected to be the $F_2$ laser (λ = 157 nm), but this lithography technology has to all intents and purposes been abandoned due to complications involved in producing optics in $CaF_2$, which is transparent at this wavelength. While the shortening of wavelengths in exposure tools has been the driving factor behind the strong resolution gain already achieved, two other factors have nevertheless played key roles. The first was the development of polymer-lattice photoresists with low absorbance at the wavelengths used, implementing progressively more innovative input energy reflection/emission systems. The second was enhanced optics reducing diffraction interference (better surface quality, increase in numerical aperture).

Over the years, the increasing complexity of the optical systems has led to resolutions actually *below* the source wavelength. This development could not continue without a major technological breakthrough, a huge step forward in wavelength. For generations of integrated circuits with a lowest resolution of between 80 and 50 nm (the next "node" being at 65 nm), various different approaches are competing to offer particle projection at ever-shorter wavelengths. They use either "soft" X-rays at extreme ultraviolet wavelength (around 10 nm), "hard" X-rays at wavelengths below 1 nm, ions or electrons.

The step crossing below the 50 nm barrier will lead towards low-electron-energy (10 eV)-enabled nanolithography with technology solutions such as the scanning tunnelling microscope and molecular beam epitaxy (Box C) for producing "superlattices".

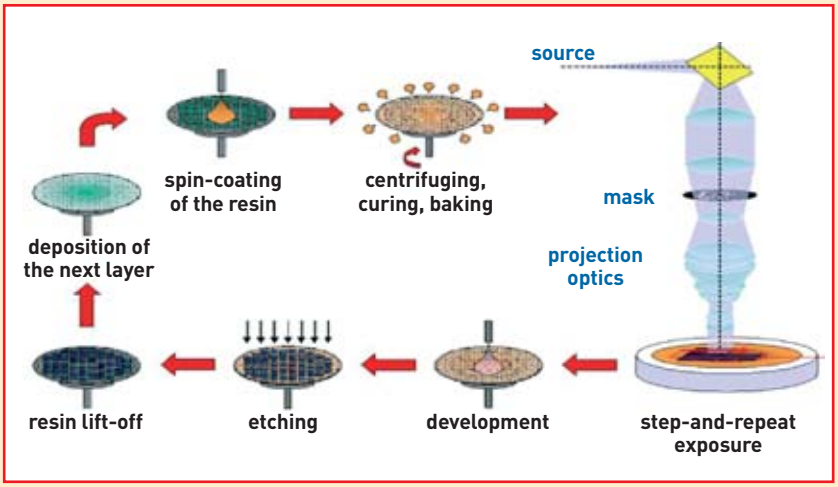



Figure. The various phases in the lithography process are designed to carve features out of the layers of conducting or insulating materials making up an integrated circuit. The sequences of the operation are laying of a photoresist, then projecting the pattern on a mask using a reduction optics system, which is followed by dissolution of the resin that is exposed to the light beam (development). The exposed parts of the initial layer can then be etched selectively, then the resin is lifted away before deposition of the following layer.

# A From the macroscopic to the nanoworld, and vice versa...

In order to gain a better idea of the size of microscopic and nanoscopic* objects, it is useful to make comparisons, usually by aligning different scales, *i.e.* matching the natural world, from molecules to man, to engineered or fabricated objects (Figure). Hence, comparing the "artificial" with the "natural" shows that artificially-produced **nanoparticles** are in fact smaller than red blood cells.

Another advantage of juxtaposing the two is that it provides a good illustration of the two main ways of developing nanoscale systems or objects: ***top-down*** and ***bottom-up***. In fact, there are two ways into the nanoworld: molecular manufacturing, involving the control of single **atoms** and the building from the ground up, and extreme miniaturization, generating progressively smaller systems.

Top-down technology is based on the artificial, using macroscopic materials that we chip away using our hands and our tools: for decades now, electronics has been applied using **silicon** as a substrate and what are called "**wafers**" as workpieces. In fact, microelectronics is also where the "top-down" synthesis approach gets its name from. However, we have reached a stage where, over and above simply adapting the miniaturization of silicon, we also have to take on or use certain physical phenomena, particularly from **quantum** physics, that operate when working at the nanoscale.

The bottom-up approach can get around these physical limits and also cut manufacturing costs, which it does by using component **self-assembly**. This is the approach that follows nature by assembling molecules to create **proteins**, which are a series of amino acids that the super-molecules, *i.e.* **nucleic acids** (**DNA**, **RNA**), are able to produce within cells to form functional structures that can reproduce in more complex patterns. Bottom-up synthesis aims at structuring the material using "building blocks", including atoms themselves, as is the case with living objects in nature. Nanoelectronics seeks to follow this assembly approach to make functional structures at lower manufacturing cost.

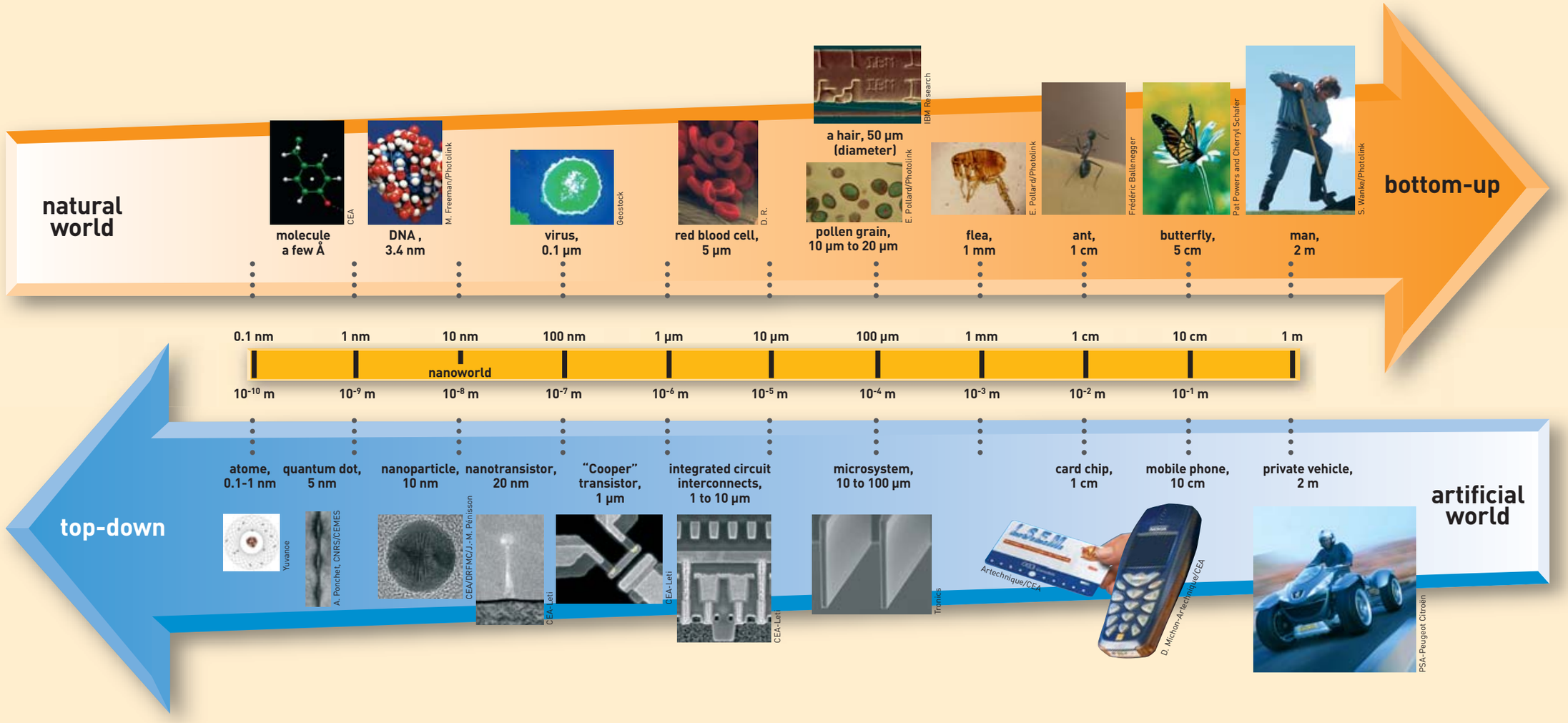
The **nanosciences** can be defined as the body of research into the physical, chemical or biological properties of nano-objects, how to manufacture them, and how they self-assemble by auto-organisazation.

**Nanotechnologies** cover all the methods that can be used to work at molecular scale to reorganize matter into objects and materials, even progressing to the macroscopic scale.


**300-mm silicon wafer produced by the Crolles2 Alliance, an illustration of current capabilities using top-down microelectronics.**

* From the Greek *nano meaning* "very small", which is also used as a prefix meaning a billionth ($10^{-9}$) of a unit. In fact, the **nanometre** (1 nm = $10^{-9}$ metres , or a billionth of a metre), is the master unit for nanosciences and nanotechnologies.

A (next)


natural world
bottom-up
molecule a few Å
CEA
DNA , 3.4 nm
M. Freeman/Photolink
virus, 0.1 µm
Geostock
red blood cell, 5 µm
D. R.
a hair, 50 µm (diameter)
IBM Research
pollen grain, 10 µm to 20 µm
E. Pollard/Photolink
flea, 1 mm
E. Pollard/Photolink
ant, 1 cm
Frédéric Ballenegger
butterfly, 5 cm
Pat Powers and Cheryl Schafer
man, 2 m
S. Wanke/Photolink
0.1 nm
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10 nm
100 nm
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10 cm
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nanoworld
10-10 m
10-9 m
10-8 m
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A. Ponchet, CNRS/CEMES
nanoparticle, 10 nm
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CEA-Leti
microsystem, 10 to 100 µm
Tronics
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Artechnique/CEA
mobile phone, 10 cm
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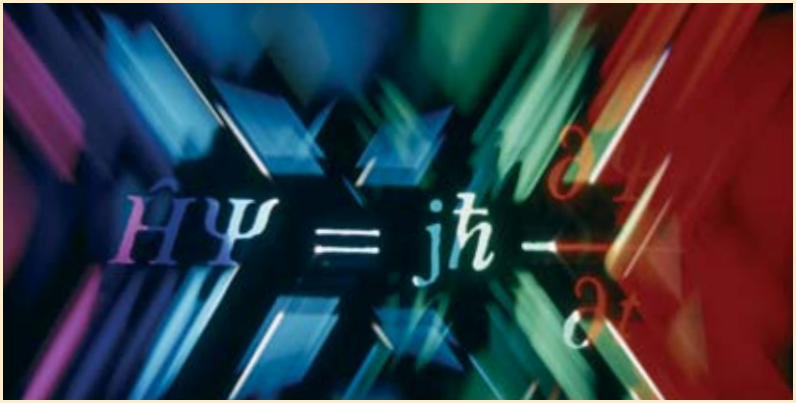
private vehicle, 2 m
PSA-Peugeot Citroën

# B A guide to quantum physics

**Quantum physics** (historically known as quantum mechanics) covers a set of physical laws that apply at microscopic scale. While fundamentally different from the majority of laws that appear to apply at our own scale, the laws of quantum physics nevertheless underpin the general basis of physics at all scales. That said, on the macroscopic scale, quantum physics in action appears to behave particularly strangely, except for a certain number of phenomena that were already curious, such as **superconductivity** or superfluidity, which in fact can only explained by the laws of quantum physics. Furthermore, the transition from the validating the paradoxes of quantum physics to the laws of classical physics, which we find easier to comprehend, can be explained in a very general way, as will be mentioned later.

Quantum physics gets its name from the fundamental characteristics of quantum objects: characteristics such as the angular momentum (**spin**) of **discrete** or discontinuous particles called **quanta**, which can only take values multiplied by an elementary *quantum*. There is also a **quantum of action** (product of a unit of energy multiplied by time) called **Planck's constant** (symbolized as h) which has a value of 6.626 x $10^{-34}$ joule·second.




D. Sarraute/CEA

**An "artist's impression" of the Schrödinger equation.**

While classical physics separates *waves* from *particles*, quantum physics somehow covers both these concepts in a third group, which goes beyond the simple wave-particle duality that Louis de Broglie imagined. When we attempt to comprehend it, it sometimes seems closer to waves, and sometimes to particles. A quantum object cannot be separated from how it is observed, and has no fixed attributes. This applies equally to a particle - which in no way can be likened to a tiny little bead following some kind of trajectory - of light (**photon**) or matter (**electron**, **proton**, **neutron**, **atom**, etc.).

This is the underlying feature behind the **Heisenberg uncertainty principle**, which is another cornerstone of quantum physics. According to this principle (which is more *indeterminacy* than *uncertainty*), the position and the velocity of a particle cannot be measured *simultaneously* at a given point in time. Measurement remains possible, but can never be more accurate than *h*, Planck's constant. Given that these approximations have no intrinsically real value outside the observation process, this simultaneous determination of both position and velocity becomes simply impossible.

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At any moment in time, the quantum object presents the characteristic of *superposing* several states, in the same way that one wave can be the *sum* of several others. In quantum theory, the amplitude of a wave (like the peak, for example) is equal to a **probability amplitude** (or probability wave), a complex number-valued function associated with each of the possible sates of a system thus described as quantum. Mathematically speaking, a physical state in this kind of system is represented by a **state vector**, a function that can be added to others *via* superposition. In other words, the sum of two possible state vectors of a system is *also* a possible state vector of that system. Also, the product of two vector spaces is also the sum of the vector products, which indicates **entanglement**: as a state vector is generally spread through space, the notion of local objects no longer holds true. For a pair of entangled particles, *i.e.* particles created together or having already interacted, that is, described by the *product* and not the *sum* of the two individual state vectors, the fate of each particle is linked - entangled - with the other, regardless of the distance between the two. This characteristic, also called *quantum state entanglement*, has staggering consequences, even before considering the potential applications, such as quantum cryptography or - why not? - teleportation. From this point on, the ability to predict the behaviour of a quantum system is reduced to probabilistic or statistical predictability. It is as if the quantum object is some kind of "juxtaposition of possibilities". Until it has been measured, the measurable size that supposedly quantifies the physical property under study is not strictly defined. Yet as soon as this measurement process is launched, it destroys the **quantum superposition** through the "collapse of the wave-packet" described by Werner Heisenberg in 1927. All the properties of a quantum system can be deduced from the equation that Erwin Schrödinger put forward the previous year. Solving the **Schrödinger equation** made it possible to determine the energy of a system as well as the **wave function**, a notion that tends to be replaced by the probability amplitude.

According to another cornerstone principle of quantum physics, the **Pauli exclusion principle**, two identical half-spin ions (**fermions**, particularly electrons) cannot simultaneously share the same position, spin and velocity (within the limits imposed by the uncertainty principle), *i.e.* share the same *quantum state*. **Bosons** (especially photons) do not follow this principle, and can exist in the same quantum state.

The coexistence of **superposition states** is what lends **coherence** to a quantum system. This means that the theory of **quantum decoherence** is able to explain why macroscopic objects, atoms and other particles, present "classical" behaviour whereas microscopic objects show quantum behaviour. Far more influence is exerted by the "environment" (air, background radiation, etc.) than an advanced measurement device, as the environment radically removes all *superposition of states* at this scale. The larger the system considered, the more it is coupled to a large number of degrees of freedom in the environment, which means the less "chance" (to stick with a probabilistic logic) it has of maintaining any degree of quantum coherence.

**TO FIND OUT MORE:**

Étienne Klein, *Petit voyage dans le monde des quanta*, Champs, Flammarion, 2004.

# C Molecular beam epitaxy

**Quantum wells** are grown using Molecular Beam Epitaxy (from the Greek *taxi*, meaning order, and *epi*, meaning over), or MBE. The principle of this physical deposition technique, which was first developed for growing III-V **semiconductor crystals**, is based on the evaporation of ultra-pure elements of the component to be grown, in a furnace under ultra-high vacuum (where the pressure can be as low as $5 \cdot 10^{-11}$ mbar) in order to create a pure, pollution-free surface. One or more thermal beams of **atoms** or **molecules** react on the surface of a single-crystal wafer placed on a substrate kept at high temperature (several hundred °C), which serves as a lattice for the formation of a film called epitaxial film. It thus becomes possible to stack ultra-thin layers that measure a millionth of a millimetre each, *i.e.* composed of only a few atom planes.

The elements are evaporated or sublimated from an ultra-pure source placed in an **effusion cell** (or Knudsen cell; an enclosure where a molecular flux moves from a region with a given pressure to another region of lower pressure) heated by the **Joule effect**. A range of structural and analytical probes can monitor film growth *in situ* in real time, particularly using surface quality analysis and grazing angle phase transitions by LEED (*Low energy electron diffraction*) or RHEED (*Reflection high-energy electron diffraction*). Various **spectroscopic** methods are also used, including Auger **electron** spectroscopy, secondary **ion** mass spectrometry (SIMS), **X-ray** photoelectron spectrometry (XPS) or **ultraviolet** photoelectron spectrometry (UPS).

As *ultra-high-vacuum* technology has progressed, molecular beam epitaxy has branched out to be applied beyond III-V semiconductors to embrace metals and insulators. In fact, the vacuum in the growth chamber, whose design changes depending on the properties of the matter intended to be deposited, has to be better than $10^{-11}$ mbar in order to grow an ultra-pure film of exceptional crystal quality at relatively low substrate temperatures. This value corresponds to the vacuum quality when the growth chamber is at rest. Arsenides, for example, grow at a residual vacuum of around $10^{-8}$ mbar as soon as the arsenic cell has reached its set growth temperature.

The pumping necessary to achieve these performance levels draws on several techniques using ion pumps, cryopumping, titanium sublimation pumping, diffusion pumps or turbomolecular pumps. The main impurities ($H_2$, $H_2O$, CO and $CO_2$) can present partial pressures of lower than $10^{-13}$ mbar.

# D The transistor, fundamental component of integrated circuits

The first transistor was made in germanium by John Bardeen and Walter H. Brattain, in December 1947. The year after, along with William B. Shockley at **Bell Laboratories**, they developed the bipolar transistor and the associated theory. During the 1950s, transistors were made with **silicon** (Si), which to this day remains the most widely-used **semiconductor** due to the exceptional quality of the interface created by silicon and silicon oxide ($SiO_2$), which serves as an insulator. In 1958, Jack Kilby invented the **integrated circuit** by manufacturing 5 components on the same **substrate**. The 1970s saw the advent of the first microprocessor, produced by Intel and incorporating 2,250 transistors, and the first memory. The complexity of integrated circuits has grown exponentially (doubling every 2 to 3 years according to "Moore's law") as transistors continue to become increasingly miniaturized.

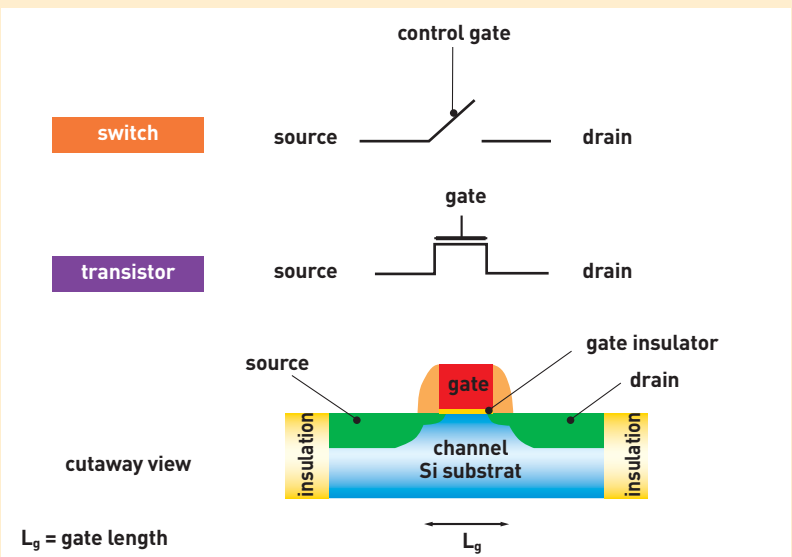


Figure.
A MOS transistor is a switching device for controlling the passage of an electric current from the source (S) to the drain (D) via a gate (G) that is electrically insulated from the conducting channel. The silicon substrate is marked B for Bulk.

The transistor, a name derived from *trans*fer and res*istor*, is a fundamental component of microelectronic integrated circuits, and is set to remain so with the necessary changes at the nanoelectronics scale: also well-suited to amplification, among other functions, it performs one essential basic function which is to open or close a current as required, like a switching device (Figure). Its basic working principle therefore applies directly to processing binary code (0, the current is blocked, 1 it goes through) in logic circuits (inverters, gates, adders, and memory cells).

The transistor, which is based on the transport of **electrons** in a solid and not in a vacuum, as in the electron tubes of the old **triodes**, comprises three **electrodes** (*anode, cathode* and *gate*), two of which serve as an electron *reservoir*: the **source**, which acts as the emitter filament of an electron tube, the **drain**, which acts as the collector plate, with the gate as "controller". These elements work differently in the two main types of transistor used today: *bipolar junction transistors*, which came first, and *field effect transistors* (**FET**).

Bipolar transistors use two types of **charge carriers**, electrons (negative charge) and **holes** (positive charge), and are comprised of identically **doped** (p or n) semiconductor substrate parts

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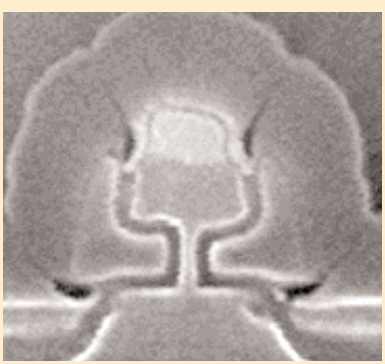
separated by a thin layer of inversely-doped semiconductor. By assembling two semiconductors of opposite types (a p-n junction), the current can be made to pass through in only one direction. Bipolar transistors, whether n-p-n type or p-n-p type, are all basically current amplifier controlled by a gate current[1]: thus, in an n-p-n transistor, the voltage applied to the p part controls the flow of current between the two n regions. Logic circuits that use bipolar transistors, which are called TTL (for transistor-transistor logic), consume more energy than field effect transistors which present a zero gate current in off-state and are voltage-controlled.

Field effect transistors, most commonly of **MOS** (metal oxide semiconductor) type, are used in the majority of today's **CMOS** (C for complementary) logic circuits[2]. Two n-type regions are created on a p-type silicon crystal by doping the surface. These two regions, also called drain and source, are thus separated by a very narrow p-type space called the **channel**. The effect of a positive current on the control electrode, naturally called the **gate**, positioned over the semiconductor forces the holes to the surface, where they attract the few mobile electrons of the semiconductor. This forms a conducting channel between source and drain (Figure). When a negative voltage is applied to the gate, which is electrically insulated by an oxide layer, the electrons are forced out of the channel. As the positive voltage increases, the channel resistance decreases, letting progressively more current through.

In an integrated circuit, transistors together with the other components (**diodes**, condensers, resistances) are initially incorporated into a "chip" with more or less complex functions. The circuit is built by "sandwiching" layer upon layer of conducting materials and insulators formed by **lithography** (Box E, ***Lithography, the key to miniaturization***). By far the most classic application of this is the microprocessor at the heart of our computers, which contains several hundred million transistors (whose size has been reduced 10,000-fold since the 1960s), soon a billion. This has led to industrial manufacturers splitting the core of the processors into several subunits working in parallel!

Lucent Technologies Inc./Bell Labs

The very first transistor.



STMicroelectronics

8 nanometre transistor developed by the Crolles2 Alliance bringing together STMicroelectronics, Philips and Freescale Semiconductor.

(1) This category includes **Schottky transistors** or **Schottky barrier transistors** which are field effect transistors with a metal/semiconductor control gate that, while more complex, gives improved charge-carrier mobility and response times.

(2) Giving **MOSFET** transistor (for Metal Oxide Semiconductor Field Effect Transistor).

# G The tunnel effect, a quantum phenomenon

Quantum physics predicts unexpected behaviour that defies ordinary intuition. The tunnel effect is an example. Take the case of a marble that rolls over a bump. Classical physics predicts that unless the marble has enough kinetic energy it will not reach the top of the bump, and will roll back towards its starting point. In quantum physics, a particle (proton, electron) can get past the bump even if its initial energy is insufficient, by "tunnelling" through. The tunnel effect makes it possible for two protons to overcome their mutual electrical repulsion at lower relative velocities than those predicted by classical calculations.

Tunnel effect microscopy is based on the fact that there is a finite probability that a particle with energy lower than the height of a potential barrier (the bump) can still jump over it. The particles are electrons travelling through the space between two electrodes. These electrodes are a fine metal tip terminating in a single atom, and the metal or semiconductor surface of the sample. In classical physics a solid surface is considered as a well-defined boundary with electrons confined inside the solid. By contrast, in quantum physics each electron has wave properties that make its location uncertain. It can be visualized as an electron cloud located close to the surface. The density of this cloud falls off exponentially with increasing distance from the solid surface. There is thus a certain probability that an electron will be located "outside" the solid at a given time. When the fine metal tip is brought near the surface at a distance of less than a nanometre, the wave function associated with the electron is non-null on the other side of the potential barrier and so electrons can travel from the surface to the tip, and *vice versa*, by the tunnel effect. The potential barrier crossed by the electron is called the tunnel barrier. When a low potential is applied between the tip and the surface, a tunnel current can be detected. The tip and the surface being studied together form a local tunnel junction. The tunnel effect is also at work in Josephson junctions where a direct current can flow through a narrow discontinuity between two superconductors.

In a transistor, an unwanted tunnel effect can appear when the insulator or grid is very thin (nanometre scale). Conversely, the effect is put to use in novel devices such as Schottky barrier tunnel transistors and carbon nanotube assemblies.