Nanotubes, multipurpose **electron guns**

Carbon nanotubes are particularly well adapted to extracting electrons at room temperature. This property stems directly from their shape, and can be used in two main applications: in the production of flat-screen displays, and as tiny electron guns for fabricating the electronic microcircuits of the future. These two examples highlight how the contribution of nanotechnology engineering can be applied in regular, everyday objects as much as cutting-edge high technology.

It is possible to emit **electrons** from a conductor material, at room temperature, when this material is subjected to an electrical field of above one billion volts per metre (in other words, a thousand volts per micron). The colossal values involved generate major technical problems in obtaining this effect (called field effect or cold emission) when electrons are to be extracted from a flat surface. This technical hurdle can be bypassed by using tips with a very low bend radius placed in front of a **polarized anode**. The local field at the peak of the tip is in fact the result of an applied field multiplied by an amplification coefficient that essentially depends on the geometry of the tip. This coefficient, typically in the 10 to 100 bracket, brings the electrical field voltage required for emission to within reasonably manageable values. This field voltage becomes stronger with higher aspect ratios between tip height and bend radius. This is where carbon nanotubes come into play (see *Carbon nanotubes*).

Nanotubes boast exceptional dimensions: a diametre ranging from 1 to a few tens of nanometres (nm) for a length that can easily reach several microns (µm), without mentioning records on the millimetre, or even centimetre scale. They thus represent very promising objects for use in field emission as their aspect ratio (which, for a nanotube, is the ratio between height and radius) can easily go into the thousands. This exceptional geometry means electrons can be easily extracted from

CEA

Image taken from the first 15-cm viewing-angle video screen based on carbon nanotubes produced at the Leti. This demonstration monochrome display has 320 x 240 pixels at pitch 350 µm.

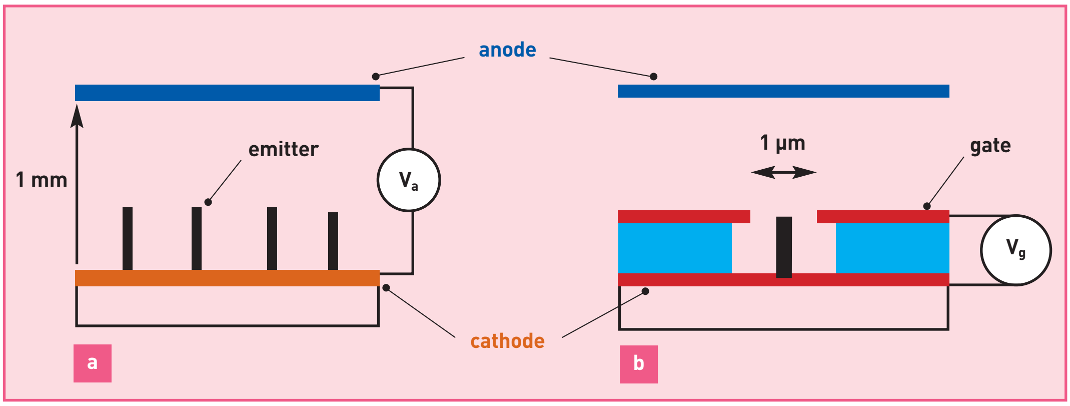


Figure 1.
Working principle behind the structures used to extract electrons by cold emission.
Diode structure (a): the electrical field applied between anode and cathode is amplified by the tip effect of the emitters, which can, for example, be nanotubes. Given the field strength required, voltage Va is around a handful of kilovolts, since the distances between anode and cathode are of the order of a millimetre.
Triode structure (b): the most universally used system. In this set-up, the extraction field is obtained by the gate placed at within a few microns of the emitter. Under these conditions, the gate voltage Vg required to extract the electrons is only around a few tens of volts, and the whole system is "integratable".

the materials by applying weak fields of just a few volts per micron.

High-performance electron emitters

In contrast with molecular electronics applications that require highly crystallized nanotubes with a set metallic or **semiconductor** state, field-effect nanotube applications are far less demanding. They can work with much lower quality tubes, which makes it possible to use multi-walled nanotubes fabricated at relatively low temperatures, which are therefore compatible with deposits on glass substrates or on functional **silicon integrated circuits**.

Classical structures for electron extraction are **triodes** (figure 1b) where the field is applied through a **gate** close to the emitter. Having the gate so close means that only relatively low voltages (typically 40-odd volts) are needed to obtain an emission current. Once extracted from the material, the electrons are accelerated in a vacuum by a second electrical field applied between the **cathode** and an **anode** placed at around 1 mm distance. The electrons interact at the anode with a either a phosphore (or luminophore) to emit light (the flat-screen display application) or with a resin to illuminate it (**lithography** application). The following gives a brief illustration of these two applications.

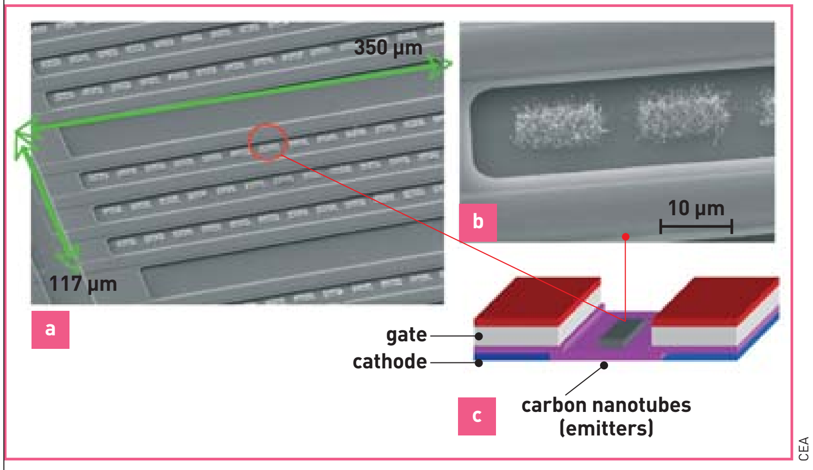


Figure 2.
Cathode structure for a flat-screen display using carbon nanotubes acting as emitters.
(a), scanning electron microscope view of a the structure of a single pixel (350 µm by 117 µm) made of four metal strips (gates) between which the nanotubes have grown o n catalyst templates located in the trenches.
(b), close-up of the nanotube carpets obtained between the gates.
Each carpet measures 10 µm x 6 µm, and the visible nanotubes are diametre 30 nm.
(c), schematic cross-section representation of the cathode structure.

The next generation of TV screens

This new screen technology is mainly targeted at a TV market where screens can reach a viewable area of up to 1 metre. The CEA's Electronics and Information Technology Laboratory (Leti) has introduced nanotubes to develop new screen structures that have no patterns below 10 µm, making them easy to produce on a large surface (Figure 2). The first generation of flat displays using cold emission was developed in the 1990s. Despite the technical success, this technology was difficult to marketed due to its prohibitive manufacturing costs. The electron emitters used were molybdenum microtips set into gate holes around a micron wide. This geometry, which was a necessity due to the low amplification coefficient of the tip, is difficult to produce profitably on a large surface area. Major industry players like Samsung are also developing this new nanotube-based technology, which may hit the consumer market before the end of decade. These displays would be brighter and less expensive that current plasma displays, which would therefore be phased out after market release of the new technology.

Once the triode-based screen structure is built using conventional techniques such as thin-layer deposition and etching, the nanotubes can be deposited during a growth phase at 600°C. Nanotube growth is localized solely on **catalyst** templates (figure 3) that are far larger (at 10 µm x 6 µm) than the nanotubes to be produced, but only 10 nm thick. When the whole structure is heated at 600°C, the layer breaks up into an array of droplets whose diametre becomes that of the nanotubes. These droplets become nanotube **growth seeds** that will self-organize into a carpet on the zone that was originally covered by the catalyst template.

This technology is potentially very useful, as it enables both the diametre and the density of the nanotubes to be controlled without having to go through costly lithography steps. The nanotube carpets are used "as is" for emission, with the longer tubes statistically acting as electron emitters. Current performance capabilities with this technology are approaching the levels required to build a finished product. The brightness, life-span and production costs achieved are all very promising. Only the uniformity of emission between pixels still needs working on.

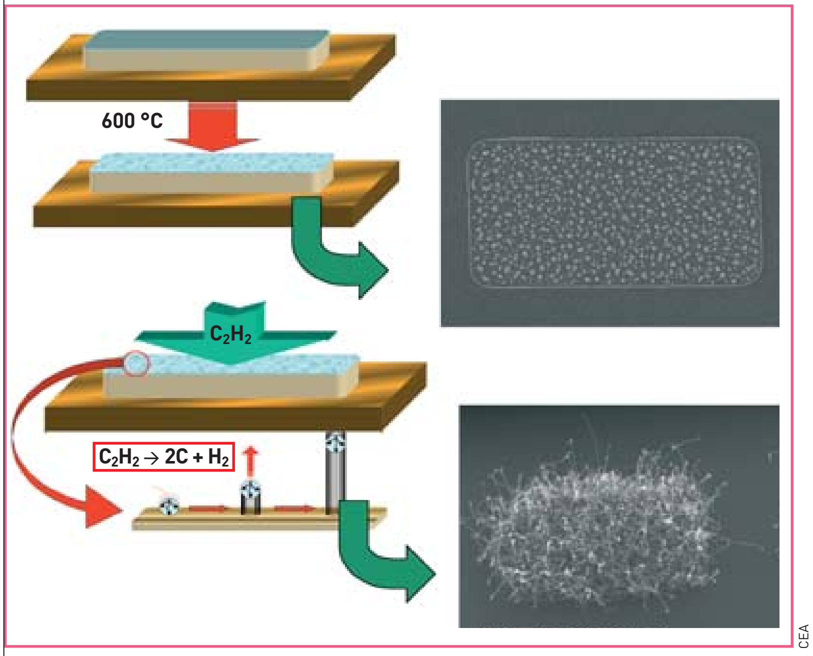


Figure 3.
Process for growing the nanotubes used in flat-screen displays. In step 1 (top left), the catalyst template fragments under the effect of the high temperature.
The droplet catalyst particles are clearly visible in the scanning electron microscope image (top right) of a catalyst template following fragmentation.
Step 2 (bottom left) is the growth of the nanotubes on the catalyst droplets. The reactive gas (in this case, acetylene) breaks down on each of the droplets, and the carbon diffuses through it, thus building the nanotube under the droplet which is at the top of the tube.
The image of the catalyst template after growth (bottom right) shows the nanotube carpet.

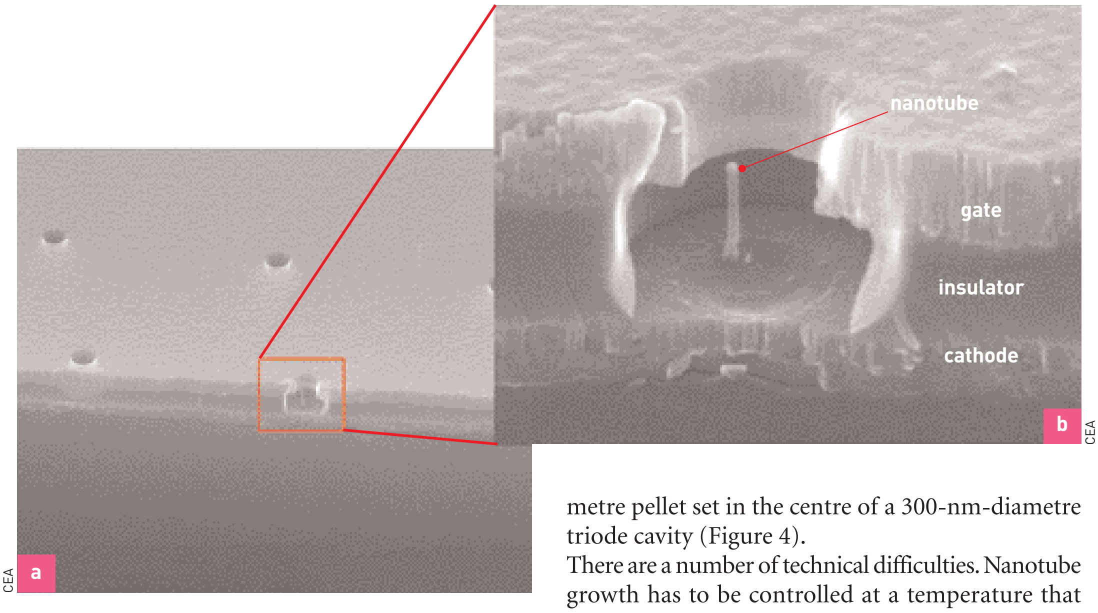


Figure 4.
Scanning microscope images of an array of electron guns produced on a 200-mm silicon wafer. (a); view of a network of triode cavities.
The gate holes have a diameter of 300 nm.
(b); cross-section close-up showing the vertical carbon nanotube in its cavity, and the stacking of the materials making up the nanodevice. Both gate and cathode are metals insulated by a silicon insulating layer.

Taking advanced lithography forward

There is a huge need for **lithography** (a technology step whereby a pattern initially present in a mask is reproduced at smaller scale in a material), driven towards ever higher **resolutions** by the need to integrate micro- and nanoelectronic components. In a few years time (around 2010), the huge resolutions required to fabricate the integrated circuits of the future will have exceeded the possibilities achievable by optics since the wavelength of the useable light (**ultra-violet**) will have become too wide for the patterns that will need creating (dimensions below 50 nm).

Maskless lithography

The solution for increasing resolution is to replace the use of an optics-based light beam to reproduce a mask carrying the patterns to be etched, by an electron beam to carve these patterns directly into a resin. The resolution gain is essentially equivalent to the resolution gain between a classical optical microscope and an electron microscope. This solution does, however, generate a whole new problem: the time for writing patterns into a resin, which is done locally with a single electronic paintbrush, point by point, becomes prohibitive and increasingly long as resolution increases to reach the target values, which are below 5 nm. To reduce the write-time, since an image cannot be made, the idea is to use not one electron beam but a vast array (typically around 10,000) all working in parallel. Each beam has to be individually piloted by a silicon integrated circuit. An array of micro electron guns thus has to be built above the control circuit.
To achieve this, research engineers naturally thought of carbon nanotubes, whose low threshold electronic emission field strength can be used to make ultra-small control circuits that can easily be integrated. In contrast with the flat display application, the objective here is to engineer individual vertical nanotubes with ultra-high-precision localization (to below 50 nm) within the assembly. The catalyst is still used to initiate growth. Here, it is made of a 50-nm-diametre pellet set in the centre of a 300-nm-diametre triode cavity (Figure 4).
There are a number of technical difficulties. Nanotube growth has to be controlled at a temperature that can guarantee that the electronics works correctly (typically 400°C), whereas the tube growth temperatures are generally above 600°C. The images obtained by the Leti during project development so far bear witness to the progress made in this domain.

The first electronic macro-componentthat functions via nano-objects

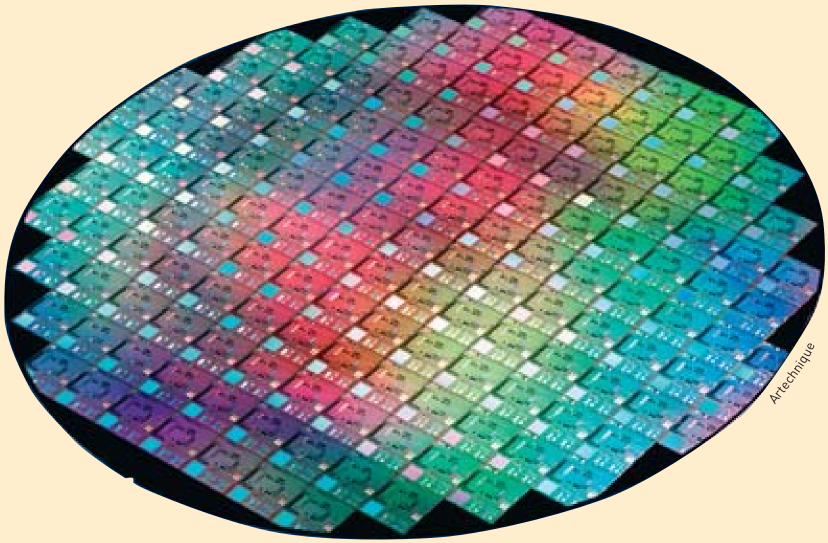
Flat-screen displays are almost certainly the first type of macro-component to function via nano-objects currently operational at the CEA. This application provides a good illustration of the technical revolution about to introduce these objects into electronic components, which nanotechnologies have already made cheaper while maintaining the required levels of performance. In micro-guns developed for use in lithography, the exceptional intrinsic qualities of these same nano-objects are expected to significantly boost the overall performance of the system. We are only just starting to get to grips with nanotube technology, but already it is clear that a wide range of consumer and high-tech objects will have integrated nanotubes in a few years time.

> **Jean Dijon**
Technological Research Division
CEA Grenoble Centre

A From the macroscopic to the nanoworld, and vice versa...

In order to gain a better idea of the size of microscopic and nanoscopic* objects, it is useful to make comparisons, usually by aligning different scales, *i.e.* matching the natural world, from molecules to man, to engineered or fabricated objects (Figure). Hence, comparing the "artificial" with the "natural" shows that artificially-produced **nanoparticles** are in fact smaller than red blood cells.
Another advantage of juxtaposing the two is that it provides a good illustration of the two main ways of developing nanoscale systems or objects: ***top-down*** and ***bottom-up***. In fact, there are two ways into the nanoworld: molecular manufacturing, involving the control of single **atoms** and the building from the ground up, and extreme miniaturization, generating progressively smaller systems.
Top-down technology is based on the artificial, using macroscopic materials that we chip away using our hands and our tools: for decades now, electronics has been applied using **silicon** as a substrate and what are called "**wafers**" as workpieces. In fact, microelectronics is also where the "top-down" synthesis approach gets its name from. However, we have reached a stage where, over and above simply adapting the miniaturization of silicon, we also have to take on or use certain physical phenomena, particularly from **quantum** physics, that operate when working at the nanoscale.
The bottom-up approach can get around these physical limits and also cut manufacturing costs, which it does by using component **self-assembly**. This is the approach that follows nature by assembling molecules to create **proteins**, which are a series of amino acids that the super-molecules, *i.e.* **nucleic acids** (**DNA**, **RNA**), are able to produce within cells to form functional structures that can reproduce in more complex patterns. Bottom-up synthesis aims at structuring the material using "building blocks", including atoms themselves, as is the case with living objects in nature. Nanoelectronics seeks to follow this assembly approach to make functional structures at lower manufacturing cost.
The **nanosciences** can be defined as the body of research into the physical, chemical or biological properties of nano-objects, how to manufacture them, and how they self-assemble by auto-organisazation.
Nanotechnologies cover all the methods that can be used to work at molecular scale to reorganize matter into objects and materials, even progressing to the macroscopic scale.

* From the Greek *nano meaning* "very small", which is also used as a prefix meaning a billionth (10^{-9}) of a unit.
In fact, the **nanometre** (1 nm = 10^{-9} metres , or a billionth of a metre), is the master unit for nanosciences and nanotechnologies.



300-mm silicon wafer produced by the Crolles2 Alliance, an illustration of current capabilities using top-down microelectronics.

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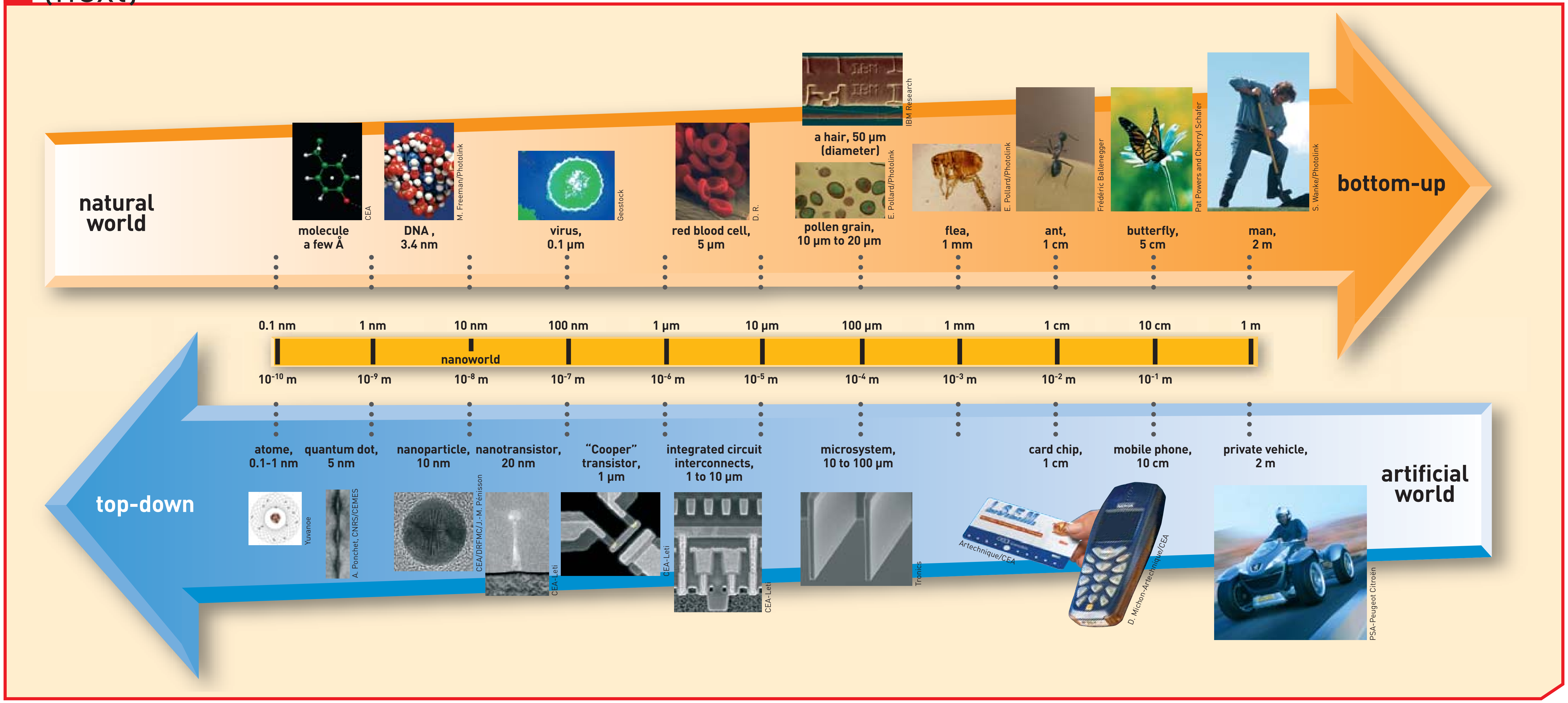
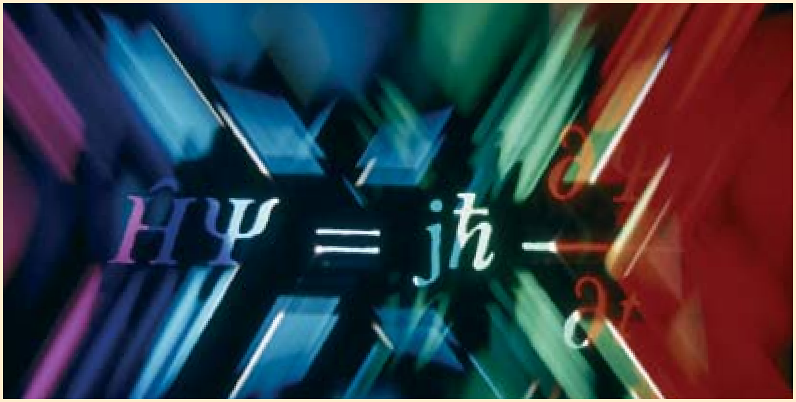

natural world
molecule a few Å
DNA, 3.4 nm
virus, 0.1 µm
red blood cell, 5 µm
a hair, 50 µm (diameter)
pollen grain, 10 µm to 20 µm
flea, 1 mm
ant, 1 cm
butterfly, 5 cm
man, 2 m
bottom-up
0.1 nm
1 nm
10 nm
100 nm
1 µm
10 µm
100 µm
1 mm
1 cm
10 cm
1 m
nanoworld
10^{-10} m
10^{-9} m
10^{-8} m
10^{-7} m
10^{-6} m
10^{-5} m
10^{-4} m
10^{-3} m
10^{-2} m
10^{-1} m
top-down
atome, 0.1-1 nm
quantum dot, 5 nm
nanoparticle, 10 nm
nanotransistor, 20 nm
"Cooper" transistor, 1 µm
integrated circuit interconnects, 1 to 10 µm
microsystem, 10 to 100 µm
card chip, 1 cm
mobile phone, 10 cm
private vehicle, 2 m
artificial world
CEA
M. Freeman/Photolink
Geostock
D. R.
IBM Research
E. Pollard/Photolink
Frédéric Ballenegger
Pat Powers and Cherryl Schafer
S. Wanke/Photolink
Yuvanoe
A. Ponchet, CNRS/CEMES
CEA/DRFMC/J.-M. Pénisson
CEA-Leti
Tronics
Artechnique/CEA
D. Michon-Artechnique/CEA
PSA-Peugeot Citroën

B A guide to quantum physics

Quantum physics (historically known as quantum mechanics) covers a set of physical laws that apply at microscopic scale. While fundamentally different from the majority of laws that appear to apply at our own scale, the laws of quantum physics nevertheless underpin the general basis of physics at all scales. That said, on the macroscopic scale, quantum physics in action appears to behave particularly strangely, except for a certain number of phenomena that were already curious, such as superconductivity or superfluidity, which in fact can only explained by the laws of quantum physics. Furthermore, the transition from the validating the paradoxes of quantum physics to the laws of classical physics, which we find easier to comprehend, can be explained in a very general way, as will be mentioned later.

Quantum physics gets its name from the fundamental characteristics of quantum objects: characteristics such as the angular momentum (spin) of discrete or discontinuous particles called quanta, which can only take values multiplied by an elementary *quantum*. There is also a quantum of action (product of a unit of energy multiplied by time) called Planck's constant (symbolized as h) which has a value of 6.626 x 10^{-34} joule·second.



An "artist's impression" of the Schrödinger equation.

While classical physics separates *waves* from *particles*, quantum physics somehow covers both these concepts in a third group, which goes beyond the simple wave-particle duality that Louis de Broglie imagined. When we attempt to comprehend it, it sometimes seems closer to waves, and sometimes to particles. A quantum object cannot be separated from how it is observed, and has no fixed attributes. This applies equally to a particle - which in no way can be likened to a tiny little bead following some kind of trajectory - of light (photon) or matter (electron, proton, neutron, atom, etc.).

This is the underlying feature behind the Heisenberg uncertainty principle, which is another cornerstone of quantum physics. According to this principle (which is more *indeterminacy* than *uncertainty*), the position and the velocity of a particle cannot be measured *simultaneously* at a given point in time. Measurement remains possible, but can never be more accurate than *h*, Planck's constant. Given that these approximations have no intrinsically real value outside the observation process, this simultaneous determination of both position and velocity becomes simply impossible.

B (next)

At any moment in time, the quantum object presents the characteristic of *superposing* several states, in the same way that one wave can be the *sum* of several others. In quantum theory, the amplitude of a wave (like the peak, for example) is equal to a **probability amplitude** (or probability wave), a complex number-valued function associated with each of the possible sates of a system thus described as quantum. Mathematically speaking, a physical state in this kind of system is represented by a **state vector**, a function that can be added to others *via* superposition. In other words, the sum of two possible state vectors of a system is *also* a possible state vector of that system. Also, the product of two vector spaces is also the sum of the vector products, which indicates **entanglement**: as a state vector is generally spread through space, the notion of local objects no longer holds true. For a pair of entangled particles, *i.e.* particles created together or having already interacted, that is, described by the *product* and not the *sum* of the two individual state vectors, the fate of each particle is linked - entangled - with the other, regardless of the distance between the two. This characteristic, also called *quantum state entanglement*, has staggering consequences, even before considering the potential applications, such as quantum cryptography or - why not? - teleportation. From this point on, the ability to predict the behaviour of a quantum system is reduced to probabilistic or statistical predictability. It is as if the quantum object is some kind of "juxtaposition of possibilities". Until it has been measured, the measurable size that supposedly quantifies the physical property under study is not strictly defined. Yet as soon as this measurement process is launched, it destroys the **quantum superposition** through the "collapse of the wave-packet" described by Werner Heisenberg in 1927. All the properties of a quantum system can be deduced from the equation that Erwin Schrödinger put forward the previous year. Solving the **Schrödinger equation** made it possible to determine the energy of a system as well as the **wave function**, a notion that tends to be replaced by the probability amplitude.

According to another cornerstone principle of quantum physics, the **Pauli exclusion principle**, two identical half-spin ions (**fermions**, particularly electrons) cannot simultaneously share the same position, spin and velocity (within the limits imposed by the uncertainty principle), *i.e.* share the same *quantum state*. **Bosons** (especially photons) do not follow this principle, and can exist in the same quantum state.

The coexistence of **superposition states** is what lends **coherence** to a quantum system. This means that the theory of **quantum decoherence** is able to explain why macroscopic objects, atoms and other particles, present "classical" behaviour whereas microscopic objects show quantum behaviour. Far more influence is exerted by the "environment" (air, background radiation, etc.) than an advanced measurement device, as the environment radically removes all *superposition of states* at this scale. The larger the system considered, the more it is coupled to a large number of degrees of freedom in the environment, which means the less "chance" (to stick with a probabilistic logic) it has of maintaining any degree of quantum coherence.

TO FIND OUT MORE:

Étienne Klein, *Petit voyage dans le monde des quanta*, Champs, Flammarion, 2004.

C Molecular beam epitaxy

Quantum wells are grown using Molecular Beam Epitaxy (from the Greek *taxi*, meaning order, and *epi*, meaning over), or MBE. The principle of this physical deposition technique, which was first developed for growing III-V semiconductor crystals, is based on the evaporation of ultra-pure elements of the component to be grown, in a furnace under ultra-high vacuum (where the pressure can be as low as $5 \cdot 10^{-11}$ mbar) in order to create a pure, pollution-free surface. One or more thermal beams of atoms or molecules react on the surface of a single-crystal wafer placed on a substrate kept at high temperature (several hundred °C), which serves as a lattice for the formation of a film called epitaxial film. It thus becomes possible to stack ultra-thin layers that measure a millionth of a millimetre each, *i.e.* composed of only a few atom planes.

The elements are evaporated or sublimated from an ultra-pure source placed in an effusion cell (or Knudsen cell; an enclosure where a molecular flux moves from a region with a given pressure to another region of lower pressure) heated by the Joule effect.
A range of structural and analytical probes can monitor film growth *in situ* in real time, particularly using surface quality analysis and grazing angle phase transitions by LEED (*Low energy electron diffraction*) or RHEED (*Reflection high-energy electron diffraction*). Various spectroscopic methods are also used, including Auger electron spectroscopy, secondary ion mass spectrometry (SIMS), X-ray photoelectron spectrometry (XPS) or ultraviolet photoelectron spectrometry (UPS).
As *ultra-high-vacuum* technology has progressed, molecular beam epitaxy has branched out to be applied beyond III-V semiconductors to embrace metals and insulators. In fact, the vacuum in the growth chamber, whose design changes depending on the properties of the matter intended to be deposited, has to be better than 10^{-11} mbar in order to grow an ultra-pure film of exceptional crystal quality at relatively low substrate temperatures. This value corresponds to the vacuum quality when the growth chamber is at rest. Arsenides, for example, grow at a residual vacuum of around 10^{-8} mbar as soon as the arsenic cell has reached its set growth temperature.
The pumping necessary to achieve these performance levels draws on several techniques using ion pumps, cryopumping, titanium sublimation pumping, diffusion pumps or turbomolecular pumps. The main impurities (H_2, H_2O, CO and CO_2) can present partial pressures of lower than 10^{-13} mbar.

D The transistor, fundamental component of integrated circuits

The first transistor was made in germanium by John Bardeen and Walter H. Brattain, in December 1947. The year after, along with William B. Shockley at Bell Laboratories, they developed the bipolar transistor and the associated theory. During the 1950s, transistors were made with silicon (Si), which to this day remains the most widely-used semiconductor due to the exceptional quality of the interface created by silicon and silicon oxide (SiO_2), which serves as an insulator. In 1958, Jack Kilby invented the integrated circuit by manufacturing 5 components on the same substrate. The 1970s saw the advent of the first microprocessor, produced by Intel and incorporating 2,250 transistors, and the first memory. The complexity of integrated circuits has grown exponentially (doubling every 2 to 3 years according to "Moore's law") as transistors continue to become increasingly miniaturized.

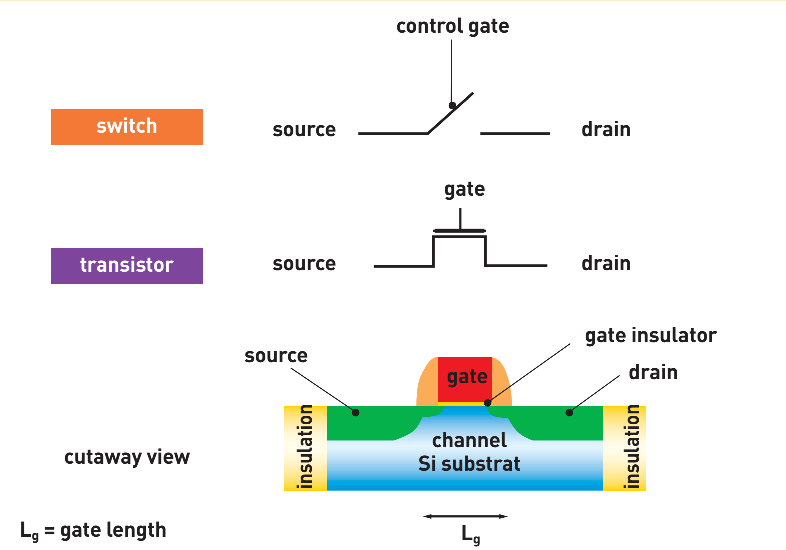


Figure.
A MOS transistor is a switching device for controlling the passage of an electric current from the source (S) to the drain (D) via a gate (G) that is electrically insulated from the conducting channel. The silicon substrate is marked B for Bulk.

The transistor, a name derived from *trans*fer and res*istor*, is a fundamental component of microelectronic integrated circuits, and is set to remain so with the necessary changes at the nanoelectronics scale: also well-suited to amplification, among other functions, it performs one essential basic function which is to open or close a current as required, like a switching device (Figure). Its basic working principle therefore applies directly to processing binary code (0, the current is blocked, 1 it goes through) in logic circuits (inverters, gates, adders, and memory cells).

The transistor, which is based on the transport of electrons in a solid and not in a vacuum, as in the electron tubes of the old triodes, comprises three electrodes (*anode, cathode* and *gate*), two of which serve as an electron *reservoir*: the source, which acts as the emitter filament of an electron tube, the drain, which acts as the collector plate, with the gate as "controller". These elements work differently in the two main types of transistor used today: *bipolar junction transistors*, which came first, and *field effect transistors* (FET).

Bipolar transistors use two types of charge carriers, electrons (negative charge) and holes (positive charge), and are comprised of identically doped (p or n) semiconductor substrate parts

D (next)

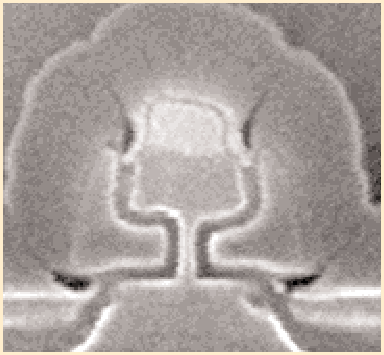
separated by a thin layer of inversely-doped semiconductor. By assembling two semiconductors of opposite types (a p-n junction), the current can be made to pass through in only one direction. Bipolar transistors, whether n-p-n type or p-n-p type, are all basically current amplifier controlled by a gate current[1]: thus, in an n-p-n transistor, the voltage applied to the p part controls the flow of current between the two n regions. Logic circuits that use bipolar transistors, which are called TTL (for transistor-transistor logic), consume more energy than field effect transistors which present a zero gate current in off-state and are voltage-controlled.

Field effect transistors, most commonly of **MOS** (metal oxide semiconductor) type, are used in the majority of today's **CMOS** (C for complementary) logic circuits[2]. Two n-type regions are created on a p-type silicon crystal by doping the surface. These two regions, also called drain and source, are thus separated by a very narrow p-type space called the **channel**. The effect of a positive current on the control electrode, naturally called the **gate**, positioned over the semiconductor forces the holes to the surface, where they attract the few mobile electrons of the semiconductor. This forms a conducting channel between source and drain (Figure). When a negative voltage is applied to the gate, which is electrically insulated by an oxide layer, the electrons are forced out of the channel. As the positive voltage increases, the channel resistance decreases, letting progressively more current through.

In an integrated circuit, transistors together with the other components (**diodes**, condensers, resistances) are initially incorporated into a "chip" with more or less complex functions. The circuit is built by "sandwiching" layer upon layer of conducting materials and insulators formed by **lithography** (Box E, ***Lithography, the key to miniaturization***). By far the most classic application of this is the microprocessor at the heart of our computers, which contains several hundred million transistors (whose size has been reduced 10,000-fold since the 1960s), soon a billion. This has led to industrial manufacturers splitting the core of the processors into several subunits working in parallel!

Lucent Technologies Inc./Bell Labs

The very first transistor.



STMicroelectronics

8 nanometre transistor developed by the Crolles2 Alliance bringing together STMicroelectronics, Philips and Freescale Semiconductor.

(1) This category includes **Schottky transistors** or **Schottky barrier transistors** which are field effect transistors with a metal/semiconductor control gate that, while more complex, gives improved charge-carrier mobility and response times.

(2) Giving **MOSFET** transistor (for Metal Oxide Semiconductor Field Effect Transistor).

E Lithography, the key to miniaturization

Optical lithography (photolithography) is a major application in the particle-matter interaction, and constitutes the classical process for fabricating integrated circuits. It is a key step in defining circuit patterns, and remains a barrier to any future development. Since resolution, at the outset, appears to be directly proportional to wavelength, feature-size first progressed by a step-wise shortening of the wavelength λ of the radiation used.

The operation works via a reduction lens system, by the *exposure* of a photoresist film to energy particles, from the ultraviolet (UV) photons currently used through to X photons, ions, and finally electrons, all through a mask template carrying a pattern of the desired circuit. The aim of all this is to transfer this pattern onto a stack of insulating or conducting layers that make up the mask. These layers will have been deposited previously (the *layering* stage) on a wafer of semiconductor material, generally silicon. After this process, the resin dissolves under exposure to the air (*development*). The exposed parts of the initial layer can then be etched selectively, then the resin is lifted away chemically before deposition of the following layer. This lithography step can take place over twenty times during the fabrication of an integrated circuit (Figure).

In the 1980s, the microelectronics industry used mercury lamps delivering near-UV (g, h and i lines) through quartz optics, with an emission line of 436 nanometres (nm). This system was able to etch structures to a feature-size of 3 microns (µm). This system was used through to the mid-90s, when it was replaced by excimer lasers emitting **far-UV** light (KrF, krypton fluoride at 248 nm, then ArF, argon fluoride at 193 nm, with the photons thus created generating several electronvolts) that were able to reach a resolution of 110 nm, pushed to under 90 nm with new processes.

In the 1980s, the CEA's Electronics and Information Technology Laboratory (Leti) pioneered the application of lasers in lithography and the fabrication of integrated circuits using excimer lasers, and even the most advanced integrated circuit production still uses these sources.

Artechnique

Photolithography section in ultra-clean facilities at the STMicroelectronics unit in Crolles (Isère).

The next step for high-volume production was expected to be the F_2 laser (λ = 157 nm), but this lithography technology has to all intents and purposes been abandoned due to complications involved in producing optics in CaF_2, which is transparent at this wavelength. While the shortening of wavelengths in exposure tools has been the driving factor behind the strong resolution gain already achieved, two other factors have nevertheless played key roles. The first was the development of polymer-lattice photoresists with low absorbance at the wavelengths used, implementing progressively more innovative input energy reflection/emission systems. The second was enhanced optics reducing diffraction interference (better surface quality, increase in numerical aperture).

Over the years, the increasing complexity of the optical systems has led to resolutions actually *below* the source wavelength. This development could not continue without a major technological breakthrough, a huge step forward in wavelength. For generations of integrated circuits with a lowest resolution of between 80 and 50 nm (the next "node" being at 65 nm), various different approaches are competing to offer particle projection at ever-shorter wavelengths. They use either "soft" X-rays at extreme ultraviolet wavelength (around 10 nm), "hard" X-rays at wavelengths below 1 nm, ions or electrons.

The step crossing below the 50 nm barrier will lead towards low-electron-energy (10 eV)-enabled nanolithography with technology solutions such as the scanning tunnelling microscope and molecular beam epitaxy (Box C) for producing "superlattices".

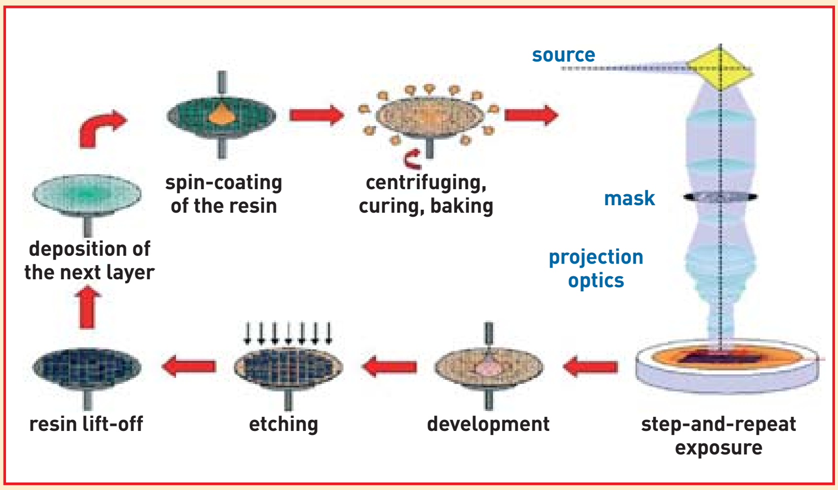


Figure. The various phases in the lithography process are designed to carve features out of the layers of conducting or insulating materials making up an integrated circuit. The sequences of the operation are laying of a photoresist, then projecting the pattern on a mask using a reduction optics system, which is followed by dissolution of the resin that is exposed to the light beam (development). The exposed parts of the initial layer can then be etched selectively, then the resin is lifted away before deposition of the following layer.

G The tunnel effect, a quantum phenomenon

Quantum physics predicts unexpected behaviour that defies ordinary intuition. The tunnel effect is an example. Take the case of a marble that rolls over a bump. Classical physics predicts that unless the marble has enough kinetic energy it will not reach the top of the bump, and will roll back towards its starting point. In quantum physics, a particle (proton, electron) can get past the bump even if its initial energy is insufficient, by "tunnelling" through. The tunnel effect makes it possible for two protons to overcome their mutual electrical repulsion at lower relative velocities than those predicted by classical calculations.

Tunnel effect microscopy is based on the fact that there is a finite probability that a particle with energy lower than the height of a potential barrier (the bump) can still jump over it. The particles are electrons travelling through the space between two electrodes. These electrodes are a fine metal tip terminating in a single atom, and the metal or semiconductor surface of the sample. In classical physics a solid surface is considered as a well-defined boundary with electrons confined inside the solid. By contrast, in quantum physics each electron has wave properties that make its location uncertain. It can be visualized as an electron cloud located close to the surface. The density of this cloud falls off exponentially with increasing distance from the solid surface. There is thus a certain probability that an electron will be located "outside" the solid at a given time. When the fine metal tip is brought near the surface at a distance of less than a nanometre, the wave function associated with the electron is non-null on the other side of the potential barrier and so electrons can travel from the surface to the tip, and *vice versa*, by the tunnel effect. The potential barrier crossed by the electron is called the tunnel barrier. When a low potential is applied between the tip and the surface, a tunnel current can be detected. The tip and the surface being studied together form a local tunnel junction. The tunnel effect is also at work in Josephson junctions where a direct current can flow through a narrow discontinuity between two superconductors.

In a transistor, an unwanted tunnel effect can appear when the insulator or grid is very thin (nanometre scale). Conversely, the effect is put to use in novel devices such as Schottky barrier tunnel transistors and carbon nanotube assemblies.